1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0011175308	ENGINEERING RELEASED	2018-02-05

D32/D33 Top MLB: EVT (D32 Build)

LAST_MODIFICATION=Wed Jan 31 16:37:18 2018

BOM:639-03991 (Ultimate)
BOM:639-03992 (Extreme)
BOM:639-03990 (Max)
MCO:056-05750

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-02545	1	SCH,MLB_TOP,D32	SCH	CRITICAL	?
820-00997	1	PCB,MLB_TOP,D32	PCB	CRITICAL	?

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DRAWING TITLE: SCH,MLB,TOP,D32

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Display CMC's

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00415	155S00391	ALT_PARTS	ALL	CMC,350SM,7HGz,MUR

NAND

Ultimate

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00340	1	HYNIX, 3DV4. ULTIMATE	U2600	CRITICAL	ULTIMATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00359	335S00340	ALT_PARTS	U2600	TOSHIBA, BICS3, ULT
335S00286	335S00340	ALT_PARTS	U2600	SANDISK, BICS3, ULT
335S00288	335S00340	ALT_PARTS	U2600	SAMSUNG, 3DV4, ULT

Extreme

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00342	1	HYNIX, 3DV4, Extreme	U2600	CRITICAL	EXTREME

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00247	335S00342	ALT_PARTS	U2600	SANDISK, BISC3, SUPREME
335S00276	335S00342	ALT_PARTS	U2600	SAMSUNG, 3DV4, SUPREME
335S00358	335S00342	ALT_PARTS	U2600	TOSHIBA, 3DV4, SUPREME

Max

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00343	1	HYNIX, 3DV4, MAX	U2600	CRITICAL	MAX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00339	335S00343	ALT_PARTS	U2600	SAMSUNG, 3DV4, MAX

Global R/C Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0648	138S0652	ALT_PARTS	ALL	CAP,X5R,4.7UF,6.3V,0.65MM,0402,TAIYO
138S0739	138S0706	ALT_PARTS	ALL	CAP,CER,X5R,0.22UF,20%,6.3V,20%
138S00049	138S0831	ALT_PARTS	ALL	CAP,CER,X5R,2.2UF,20%,6.3V,0201

Yangtze Inductors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00872	152S00918	ALT_PARTS	ALL	IND,MLD,0.47UH,TDK
152S00847	152S00918	ALT_PARTS	ALL	IND,MLD,0.47UH,CYN

CRITICAL PART#	COMMENT
152S00918	IND,MLD,0.22UH,20%,5.8A,40MOHM,H=.65,1608

Denali Inductors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00878	152S00831	ALT_PARTS	ALL	IND,MLD,0.22UH,20%,5.9A,38MOHM,H=.65,1608
152S00818	152S00831	ALT_PARTS	ALL	IND,MLD,0.22UH,20%,5.9A,38MOHM,H=.65,1608,CYN
152S00835	152S00822	ALT_PARTS	ALL	IND,MLD,0.47UH,20%,4.5A,49MOHM,H=.80,2012
152S00827	152S00822	ALT_PARTS	ALL	IND,MLD,0.47UH,20%,4.5A,50MOHM,H=.80,2012
152S00877	152S00817	ALT_PARTS	ALL	IND,MLD,0.1UH,20%,9A,20MOHM,H=0.8,2012
152S00829	152S00817	ALT_PARTS	ALL	IND,MLD,0.1UH,20%,9.0A,22MOHM,H=0.8,2012
152S00825	152S00823	ALT_PARTS	ALL	IND,MLD,1UH,20%,3A,69MO,H=.65,2016
152S00833	152S00819	ALT_PARTS	ALL	IND,MLD,1UH,20%,2.1A,42MO,H=.65,2012
152S00824	152S00819	ALT_PARTS	ALL	IND,MLD,1UH,20%,2A,69MO,H=.65,2012
152S00834	152S00820	ALT_PARTS	ALL	IND,MLD,0.47UH,20%,3.0A,270MO,H=.80,2012
152S00828	152S00820	ALT_PARTS	ALL	IND,MLD,0.47UH,20%,3.2A,460MO,H=.80,2012
152S00826	152S00821	ALT_PARTS	ALL	IND,MLD,1UH,20%,2.1A,52MO,H=.80,2012
152S00866	152S00821	ALT_PARTS	ALL	IND,MLD,1UH,20%,2.1A,52MO,H=.80,2012

CRITICAL PART#	COMMENT
152S00831	IND,MLD,0.22UH,20%,5.8A,40MOHM,H=.65,1608
152S00822	IND,MLD,0.47UH,20%,4.5A,47MOHM,H=.8,2012
152S00817	IND,MLD,0.1UH,20%,9.4A,22MOHM,H=0.65,1608
152S00823	IND,MLD,1UH,20%,3.0A,60MO,H=.65,2016
152S00819	IND,MLD,1UH,20%,1.7A,69MO,H=.65,2012
152S00820	IND,MLD,0.47UH,20%,3.2A,42MO,H=.80,2012
152S00821	IND,MLD,1UH,20%,2.2A,60MO,H=.80,2012

XTAL Alternate

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0612	197S00118	ALT_PARTS	Y1000	XTAL, 24M, 1612
197S00120	197S00118	ALT_PARTS	Y1000	XTAL, 24M, 1612

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00148	138S00149	ALT_PARTS	ALL	0402-3T,10.5uF@1V, Kyocera
138S00150	138S00149	ALT_PARTS	ALL	0402-3T,10.5uF@1V, SEMCO
138S00151	138S00149	ALT_PARTS	ALL	0402-3T,10.5uF@1V, TY

CRITICAL PART#	COMMENT
138S00149	0402-3T,10.5uF@1V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00143	138S00144	ALT_PARTS	ALL	0402,16uF@1V, Kyocera
138S00163	138S00144	ALT_PARTS	ALL	0402,16uF@1V, TY

CRITICAL PART#	COMMENT
138S00144	0402,16uF@1V

NEON Alternate

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00721	152S00876	ALT_PARTS	L4100, L4120	TY, IND

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	ALT_PARTS	ALL	0201,3uF@1V, Kyocera
138S00164	138S00139	ALT_PARTS	ALL	0201,3uF@1V, TY

CRITICAL PART#	COMMENT
138S00139	0201,3uF@1V

ANSEL Alternate

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00716	152S00875	ALT_PARTS	L3700	TY, IND

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00221	138S00146	ALT_PARTS	ALL	0402,5.1uF@3V, Kyocera

CRITICAL PART#	COMMENT
138S00146	0402,5.1uF@3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00140	138S00141	ALT_PARTS	ALL	0201,1.1uF@3V, Kyocera
138S00142	138S00141	ALT_PARTS	ALL	0201,1.1uF@3V, SEMCO
138S00166	138S00141	ALT_PARTS	ALL	0201,1.1uF@3V, Taiyo

CRITICAL PART#	COMMENT
138S00141	0201,1.1uF@3V

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EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR (MLB_TOP,639-03991,ULTIMATE)	EEEE_HWV1	CRITICAL	ULTIMATE
825-7691	1	EEEE FOR (MLB_TOP,639-03992,EXTREME)	EEEE_HWV2	CRITICAL	EXTREME
825-7691	1	EEEE FOR (MLB_TOP,639-03990,MAX)	EEEE_HWV0	CRITICAL	MAX

Cyprus OMIT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00510	1	CYPRUS 4GB Micron	U1000	CRITICAL	SOC

Cyprus ALTs

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00511	339S00510	ALT_PARTS	U1000	CYPRUS 4GB Hynix
339S00512	339S00510	ALT_PARTS	U1000	CYPRUS 4GB Samsung

Combo Stiffener

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
604-19651	1	Combo Stiffener	ST0401	CRITICAL	ALL

SYNC_MASTER=

SYNC_DATE=08/09/2017

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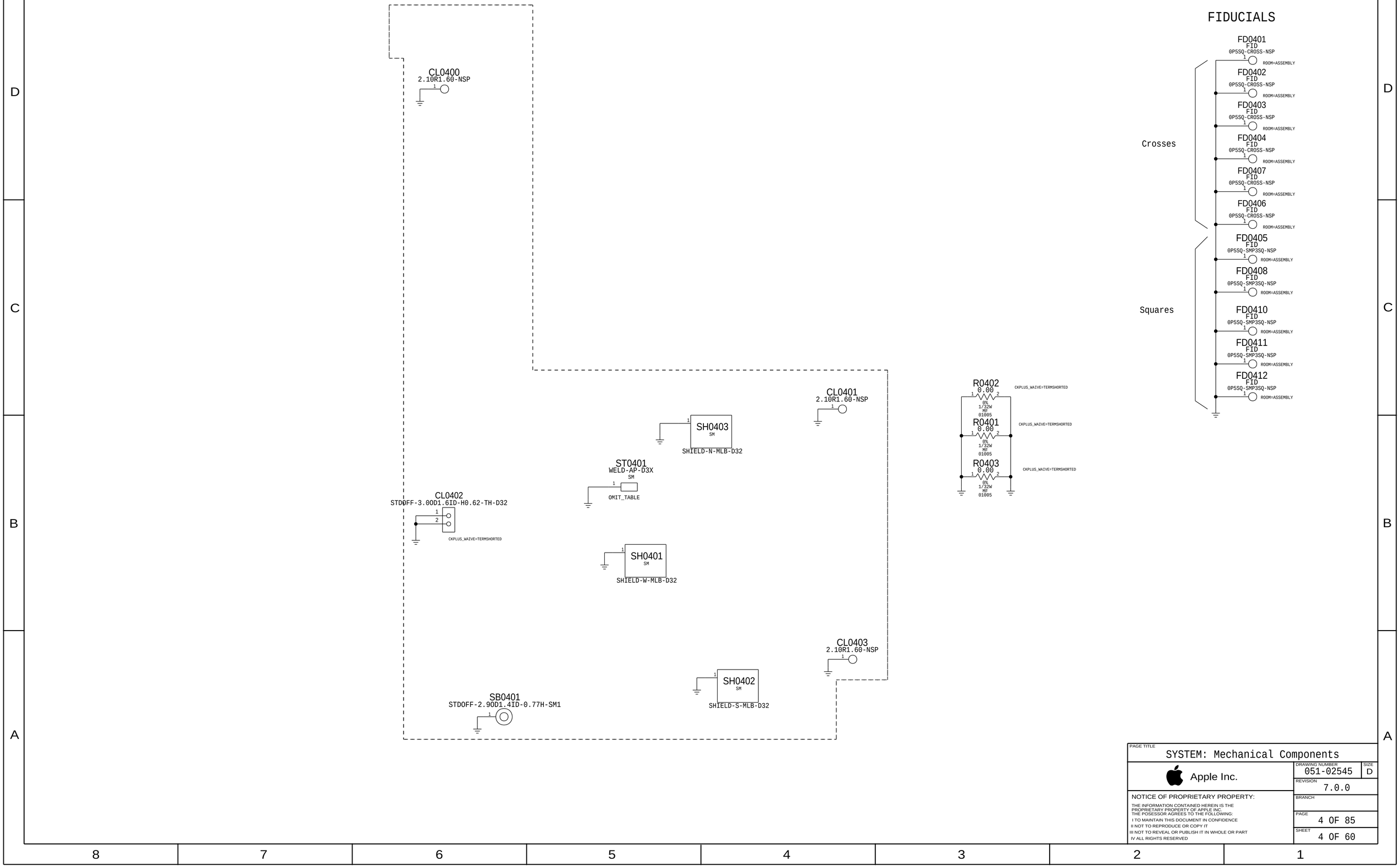

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SYSTEM: Mechanical Components

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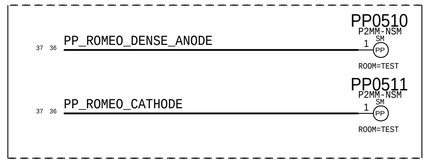
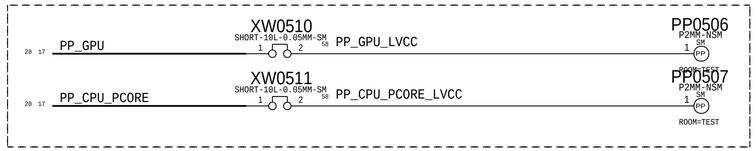
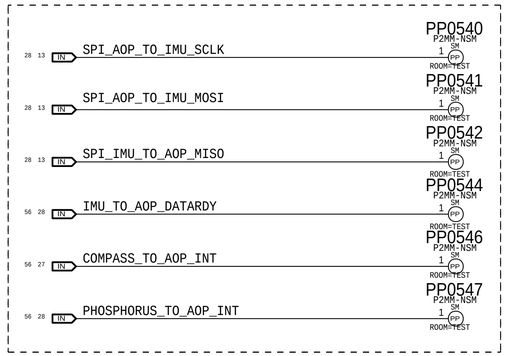
PEARL



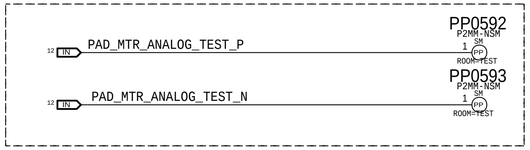
LVCC



Sensors



METROLOGY



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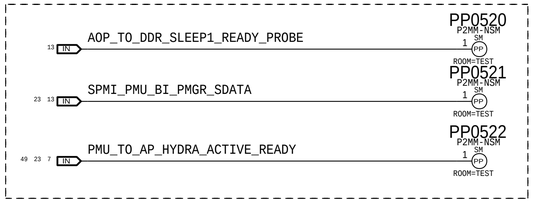
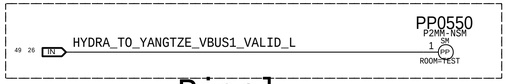
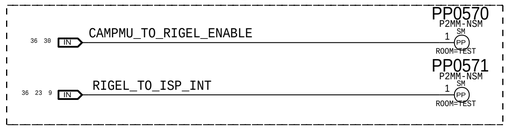


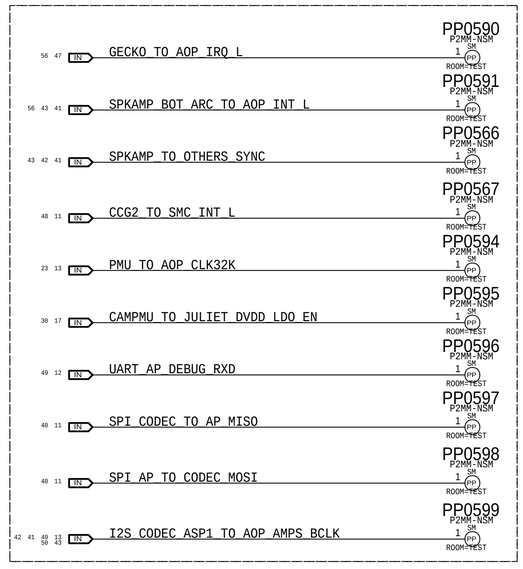
Hydra VBUS



Rigel



VALIDATION PP's



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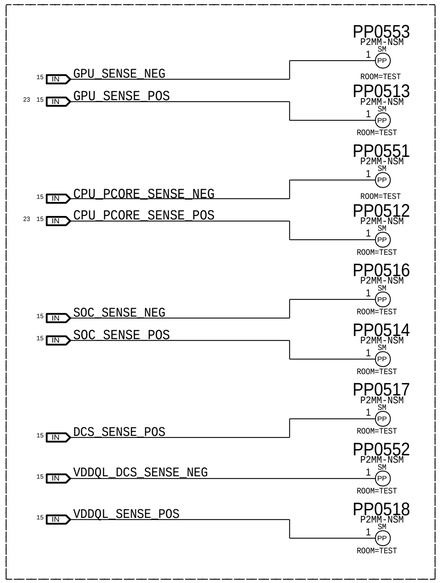
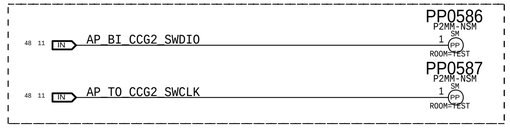
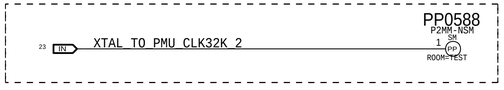


NAND

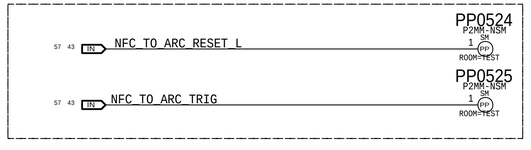
CCG SWD



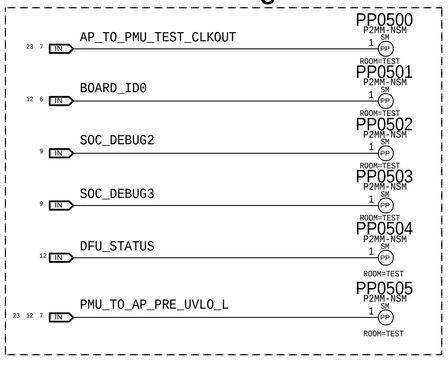
PMU XTAL



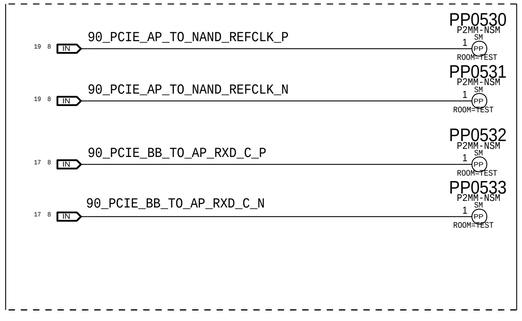
WALLET MODE



SOC Debug



PCIE Refclk



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SYSTEM: Testpoints (Top)

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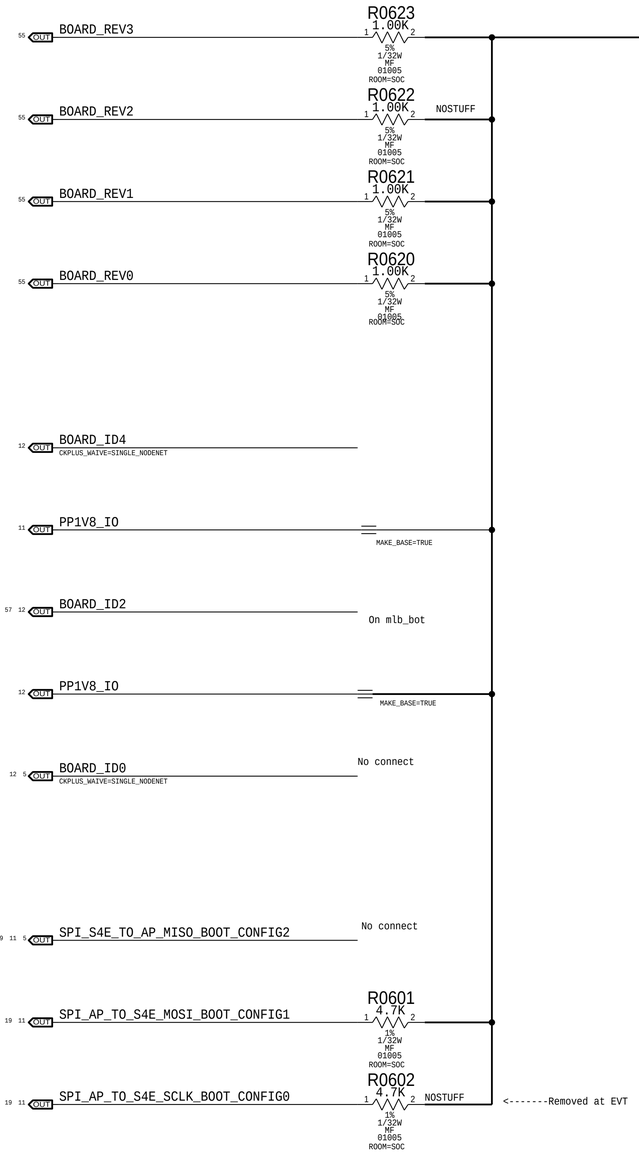
TOP BOARD ONLY CONFIGURATION IS D33 MLB MAV
BOTTOM BOARD SELECTS ICE/MAV and D32/D33

BOOTSTRAPPING:BOARD REV
BOARD ID
BOOT CONFIG



SELECTED -->

Board Rev[3:0] Float = Low PU = High	3	2	1	0
	Build Major		Build Minor	
Proto 1	**1**	**1**	**1**	**1**
(Spare)	**1**	**1**	**1**	0
Proto 2	**1**	**1**	0	**1**
(Spare)	**1**	**1**	0	0
EVT	**1**	0	**1**	**1**
(Spare)	**1**	0	**1**	0
Carrier	0	**1**	**1**	**1**
(Spare)	0	**1**	**1**	0
DVT	0	0	**1**	**1**
(Spare)	0	0	**1**	0
(Spare)	0	0	0	**1**
PVT	0	0	0	0

DEFAULT -->

Board ID[4:0] Float = Low PU = High	4	3	2	1	0
	Denali = 0, Imola = 1	Mav = 0, Ice = 1	00=Open 01=D33 10=N84 11=D32		MLB = 0, Dev = 1
D32 MLB	0	0	**1**	**1**	0
D32p MLB	**1**	0	**1**	**1**	0
D32 Dev	0	0	**1**	**1**	**1**
D32p Dev	**1**	0	**1**	**1**	**1**
D321 MLB	0	**1**	**1**	**1**	0
D321p MLB	**1**	**1**	**1**	**1**	0
D321 Dev	0	**1**	**1**	**1**	**1**
D321p Dev	**1**	**1**	**1**	**1**	**1**
D33 MLB	0	0	0	**1**	0
D33p MLB	**1**	0	0	**1**	0
D33 Dev	0	0	0	**1**	**1**
D33p Dev	**1**	0	0	**1**	**1**
D331 MLB	0	**1**	0	**1**	0
D331p MLB	**1**	**1**	0	**1**	0
D331 Dev	0	**1**	0	**1**	**1**
D331p Dev	**1**	**1**	0	**1**	**1**

POR -->

Boot Config [2:0] Float = Low PU = High	2	1	0
SPI NOR on SPI0 12 MHz	0	0	0
SPI NOR on SPI0 12 MHz Test	0	0	**1**
SPI NAND on SPI0 12 MHz	0	**1**	0
SPI NAND on SPI0 12 MHz Test	0	**1**	**1**
SPI NOR on SPI0 40 MHz	**1**	0	0
SPI NOR on SPI0 40 MHz Test	**1**	0	**1**
SPI NOR on SPI0 6 MHz	**1**	**1**	0
SPI NOR on SPI0 6 MHz Test	**1**	**1**	**1**

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BOOTSTRAPPING

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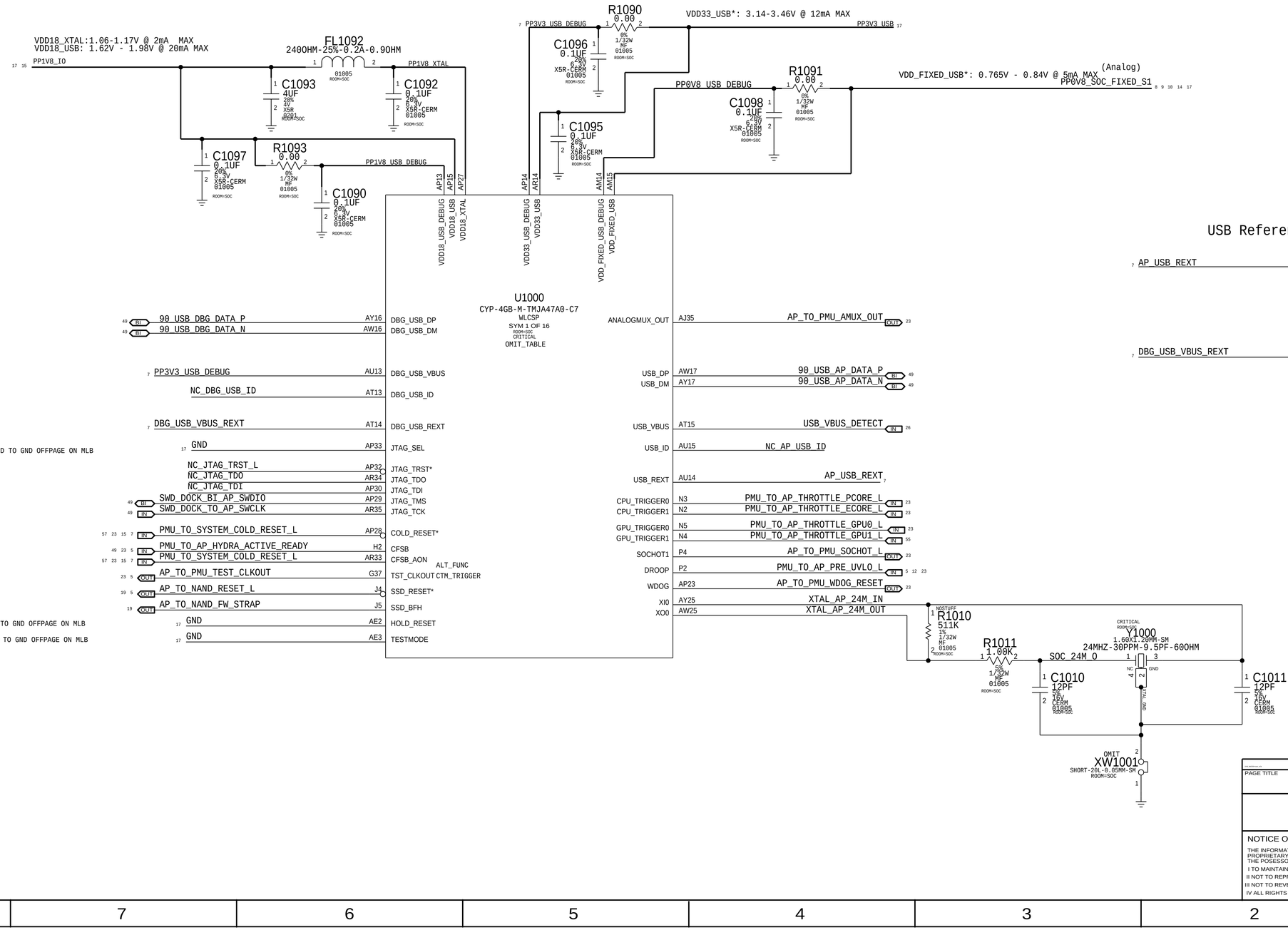
SOC - USB, JTAG, XTAL



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SOC: JTAG,USB,XTAL

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SOC - PCIE

VDD12_PCIE:1.14V - 1.26V @ 130mA MAX
VDD12_PCIE_REFBUF:1.14V - 1.26V @ 30mA MAX

17 19 PP1V2_SOC
C1199 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
OMIT XW1101 SHORT-20L-0.05MM-SM ROOM=SOC
R1195 0.00 0% 1/32W MF 01005 ROOM=SOC
PP1V2_SOC_PCIE_REFBUF
C1198 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

VDD_FIXED_PCIE:0.769V - 0.85V @ 105mA MAX
VDD_FIXED_PCIE_REFBUF:0.769V - 0.85V @ 65mA MAX
PP0V8_SOC_FIXED_S1 7 9 10 14 17
R1194 0.00 0% 1/32W MF 01005 ROOM=SOC
OMIT XW1100 SHORT-20L-0.05MM-SM ROOM=SOC
C1193 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C1191 2.2UF 20% 6.3V X5R-CERM 0201
PP0V8_SOC_FIXED_PCIE_REFBUF
C1194 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

AM29 AM31 VDD12_PCIE
AL26 AK27 VDD12_PCIE_REFBUF VDD12_PCIE_REFBUF
AL28 AL30 VDD_FIXED_PCIE0 VDD_FIXED_PCIE1
AL27 VDD_FIXED_PCIE_REFBUF

U1000
CYP-4GB-M-TMJA47A0-C7
WLCSP
SYM 2 OF 16

19 8 BI	PCIE_NAND_BI_AP_CLKREQ_L	U37	PCIE_CLKREQ0*	PCIE_CLKREQ3*	U34	PCIE_WLAN_BI_AP_CLKREQ_L	BI 8 58
19 8 OUT	90_PCIE_AP_TO_NAND_REFCLK_P	AW19	PCIE_REF_CLK0_P	PCIE_REF_CLK3_P	AY22	90_PCIE_AP_TO_WLAN_REFCLK_P	OUT 58
19 8 OUT	90_PCIE_AP_TO_NAND_REFCLK_N	AY19	PCIE_REF_CLK0_N	PCIE_REF_CLK3_N	AW22	90_PCIE_AP_TO_WLAN_REFCLK_N	OUT 58
17 IN	90_PCIE_NAND_TO_AP_RXD_C_P	AY27	PCIE_RX0_P	PCIE_RX3_P	AY33	90_PCIE_WLAN_TO_AP_RXD_C_P	IN 17
17 IN	90_PCIE_NAND_TO_AP_RXD_C_N	AW27	PCIE_RX0_N	PCIE_RX3_N	AW33	90_PCIE_WLAN_TO_AP_RXD_C_N	IN 17
17 OUT	90_PCIE_AP_TO_NAND_TXD_C_P	AU26	PCIE_TX0_P	PCIE_TX3_P	AU32	90_PCIE_AP_TO_WLAN_TXD_C_P	OUT 17
17 OUT	90_PCIE_AP_TO_NAND_TXD_C_N	AV26	PCIE_TX0_N	PCIE_TX3_N	AV32	90_PCIE_AP_TO_WLAN_TXD_C_N	OUT 17
19 8 OUT	PCIE_AP_TO_NAND_PERST_L	T36	PCIE_PERST0*	PCIE_PERST3*	R37	PCIE_AP_TO_WLAN_PERST_L	OUT 8 57

NAND LINK | LINK3

NC_PCIE1_CLKREQ1_L	U36	PCIE_CLKREQ1* Hardwired as Input	PCIE_CLKREQ2*	U35	NC_PCIE2_CLKREQ1_L		
NC_PCIE1_REF_CLK_P	AW20	PCIE_REF_CLK1_P	PCIE_REF_CLK2_P	AW21	NC_PCIE2_REF_CLK_P		
NC_PCIE1_REF_CLK_N	AY20	PCIE_REF_CLK1_N	PCIE_REF_CLK2_N	AY21	NC_PCIE2_REF_CLK_N		
NC_PCIE1_RX1_P	AY29	PCIE_RX1_P	PCIE_RX2_P	AY31	NC_PCIE2_RX1_P		
NC_PCIE1_RX1_N	AW29	PCIE_RX1_N	PCIE_RX2_N	AW31	NC_PCIE2_RX1_N		
NC_PCIE1_TX1_P	AU28	PCIE_TX1_P	PCIE_TX2_P	AU30	NC_PCIE2_TX1_P		
NC_PCIE1_TX1_N	AV28	PCIE_TX1_N	PCIE_TX2_N	AV30	NC_PCIE2_TX1_N		
NC_PCIE1_PERST_L	T35	PCIE_PERST1*	PCIE_PERST2*	T34	NC_PCIE2_PERST_L		

LINK1 | LINK2

PCIE_RCAL_POS	AT31	PCIE_RCAL_P					
	AR31	PCIE_RCAL_N					
PCIE_CLKREQ4*	T37					PCIE_BB_BI_AP_CLKREQ_L	BI 57
PCIE_REF_CLK4_P	AY23					90_PCIE_AP_TO_BB_REFCLK_P	OUT 57
PCIE_REF_CLK4_N	AW23					90_PCIE_AP_TO_BB_REFCLK_N	OUT 57
PCIE_RX4_P	AY35					90_PCIE_BB_TO_AP_RXD_C_P	IN 5 17
PCIE_RX4_N	AW35					90_PCIE_BB_TO_AP_RXD_C_N	IN 5 17
PCIE_TX4_P	AU34					90_PCIE_AP_TO_BB_TXD_C_P	OUT 17
PCIE_TX4_N	AV34					90_PCIE_AP_TO_BB_TXD_C_N	OUT 17
LINK4 PCIE_PERST4*	R35					PCIE_AP_TO_BB_PERST_L	OUT 8 57

R1140 200 1% 1/32W MF 01005 ROOM=SOC
C1140 10PF 5% 16V CERM 01005 ROOM=SOC

PCIE LINK 0
PCIE LINK 3
PCIE LINK 4

PCIe BB CLKREQ PU on BB domain

PCIe Clock Request Pull-Ups

17 PP1V8_IO
R1100 100K 5% 1/32W MF 01005 ROOM=SOC
R1130 100K 5% 1/32W MF 01005 ROOM=SOC
19 8 PCIE_NAND_BI_AP_CLKREQ_L
58 8 PCIE_WLAN_BI_AP_CLKREQ_L

PCIe Reset Pull-Downs

57 8 PCIE_AP_TO_WLAN_PERST_L
57 8 PCIE_AP_TO_BB_PERST_L
19 8 PCIE_AP_TO_NAND_PERST_L
R1101 100K 5% 1/32W MF 01005 ROOM=SOC
R1121 100K 5% 1/32W MF 01005 ROOM=SOC
R1131 100K 5% 1/32W MF 01005 ROOM=SOC

SYNC_DATE=04/07/2017

PAGE TITLE
SOC: PCIE

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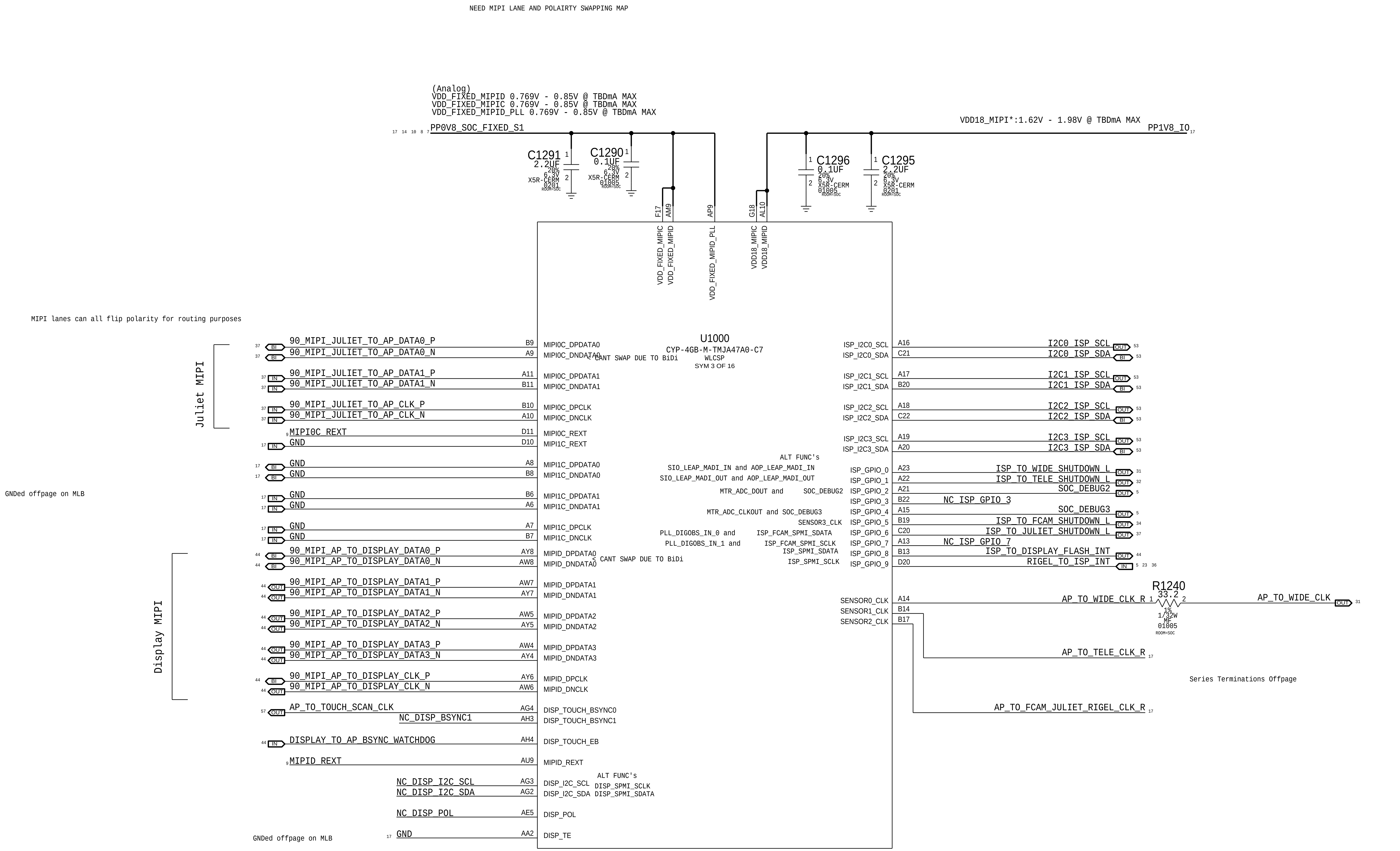
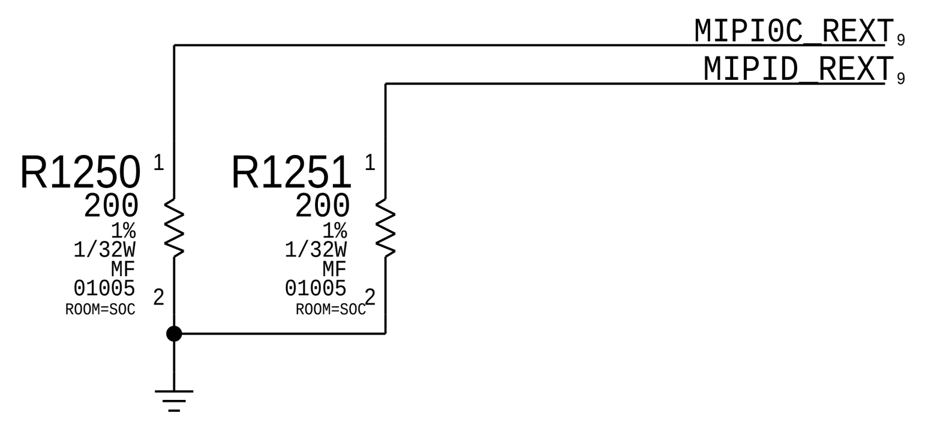
SOC - MIPI



NEED MIPI LANE AND POLAIRTY SWAPPING MAP
(Analog)
VDD_FIXED_MIPID 0.769V - 0.85V @ TBDmA MAX
VDD_FIXED_MIPIC 0.769V - 0.85V @ TBDmA MAX
VDD_FIXED_MIPID_PLL 0.769V - 0.85V @ TBDmA MAX
PP0V8_SOC_FIXED_S1
C1291 2.2UF 20% 6.3V X5R-CERM 0201
C1290 0.1UF 20% 6.3V X5R-CERM 01005
VDD18_MIPI*:1.62V - 1.98V @ TBDmA MAX
PP1V8_IO
C1296 0.1UF 20% 6.3V X5R-CERM 01005
C1295 2.2UF 20% 6.3V X5R-CERM 0201
F17 AM9 AP9 G18 AL10
VDD_FIXED_MIPIC
VDD_FIXED_MIPID
VDD_FIXED_MIPID_PLL
VDD18_MIPIC
VDD18_MIPID
MIPI lanes can all flip polarity for routing purposes
Juliet MIPI
Display MIPI
GNDed offpage on MLB
U1000
CYP-4GB-M-TMJA47A0-C7
WLCSP
SYM 3 OF 16
CANT SWAP DUE TO BiDi
90_MIPI_JULIET_TO_AP_DATA0_P B9 MIPI0C_DPDATA0
90_MIPI_JULIET_TO_AP_DATA0_N A9 MIPI0C_DNDATA0
90_MIPI_JULIET_TO_AP_DATA1_P A11 MIPI0C_DPDATA1
90_MIPI_JULIET_TO_AP_DATA1_N B11 MIPI0C_DNDATA1
90_MIPI_JULIET_TO_AP_CLK_P B10 MIPI0C_DPCLK
90_MIPI_JULIET_TO_AP_CLK_N A10 MIPI0C_DNCLK
MIPI0C_REXT D11 MIPI0C_REXT
GND D10 MIPI1C_REXT
GND A8 MIPI1C_DPDATA0
GND B8 MIPI1C_DNDATA0
GND B6 MIPI1C_DPDATA1
GND A6 MIPI1C_DNDATA1
GND A7 MIPI1C_DPCLK
GND B7 MIPI1C_DNCLK
90_MIPI_AP_TO_DISPLAY_DATA0_P AY8 MIPID_DPDATA0
90_MIPI_AP_TO_DISPLAY_DATA0_N AW8 MIPID_DNDATA0
90_MIPI_AP_TO_DISPLAY_DATA1_P AW7 MIPID_DPDATA1
90_MIPI_AP_TO_DISPLAY_DATA1_N AY7 MIPID_DNDATA1
90_MIPI_AP_TO_DISPLAY_DATA2_P AW5 MIPID_DPDATA2
90_MIPI_AP_TO_DISPLAY_DATA2_N AY5 MIPID_DNDATA2
90_MIPI_AP_TO_DISPLAY_DATA3_P AW4 MIPID_DPDATA3
90_MIPI_AP_TO_DISPLAY_DATA3_N AY4 MIPID_DNDATA3
90_MIPI_AP_TO_DISPLAY_CLK_P AY6 MIPID_DPCLK
90_MIPI_AP_TO_DISPLAY_CLK_N AW6 MIPID_DNCLK
AP_TO_TOUCH_SCAN_CLK AG4 DISP_TOUCH_BSYNC0
NC_DISP_BSYNC1 AH3 DISP_TOUCH_BSYNC1
DISPLAY_TO_AP_BSYNC_WATCHDOG AH4 DISP_TOUCH_EB
MIPID_REXT AU9 MIPID_REXT
NC_DISP_I2C_SCL AG3 DISP_I2C_SCL
NC_DISP_I2C_SDA AG2 DISP_I2C_SDA
NC_DISP_POL AE5 DISP_POL
GND AA2 DISP_TE
ALT FUNC's
DISP_SPMI_SCLK
DISP_SPMI_SDATA
ALT FUNC's
SIO_LEAP_MADI_IN and AOP_LEAP_MADI_IN
SIO_LEAP_MADI_OUT and AOP_LEAP_MADI_OUT
MTR_ADC_DOUT and SOC_DEBUG2
MTR_ADC_CLKOUT and SOC_DEBUG3
SENSOR3_CLK
PLL_DIGOBS_IN_0 and ISP_FCAM_SPMI_SDATA
PLL_DIGOBS_IN_1 and ISP_FCAM_SPMI_SCLK
ISP_SPMI_SDATA
ISP_SPMI_SCLK
ISP_I2C0_SCL A16 I2C0_ISP_SCL
ISP_I2C0_SDA C21 I2C0_ISP_SDA
ISP_I2C1_SCL A17 I2C1_ISP_SCL
ISP_I2C1_SDA B20 I2C1_ISP_SDA
ISP_I2C2_SCL A18 I2C2_ISP_SCL
ISP_I2C2_SDA C22 I2C2_ISP_SDA
ISP_I2C3_SCL A19 I2C3_ISP_SCL
ISP_I2C3_SDA A20 I2C3_ISP_SDA
ISP_GPIO_0 A23 ISP_TO_WIDE_SHUTDOWN_L
ISP_GPIO_1 A22 ISP_TO_TELE_SHUTDOWN_L
ISP_GPIO_2 A21 SOC_DEBUG2
ISP_GPIO_3 B22 NC_ISP_GPIO_3
ISP_GPIO_4 A15 SOC_DEBUG3
ISP_GPIO_5 B19 ISP_TO_FCAM_SHUTDOWN_L
ISP_GPIO_6 C20 ISP_TO_JULIET_SHUTDOWN_L
ISP_GPIO_7 A13 NC_ISP_GPIO_7
ISP_GPIO_8 B13 ISP_TO_DISPLAY_FLASH_INT
ISP_GPIO_9 D20 RIGEL_TO_ISP_INT
SENSOR0_CLK A14 AP_TO_WIDE_CLK_R
SENSOR1_CLK B14
SENSOR2_CLK B17
R1240 33.2 1% 1/32W MF 01005
AP_TO_WIDE_CLK
AP_TO_TELE_CLK_R
AP_TO_FCAM_JULIET_RIGEL_CLK_R
Series Terminations Offpage

MIPI Reference



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SOC - LPDP

VDD12_PLL_LPDP 1.14V - 1.26V @ 8mA MAX
VDD12_LPDP_RX 1.14V - 1.26V @ 60mA MAX
PP1V2_SOC

C1390 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1391 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1392 0.1UF 10% 6.3V X5R-CERM 01005 ROOM=SOC
C1393 0.01UF 10% 6.3V X5R 01005 ROOM=SOC
C1394 15PF 5% 16V NP0-C0G-CERM 01005 ROOM=SOC
Desense for Wifi frequencies

GND'd offpage
GND'd offpage
GND
GND

(Analog)
VDD_FIXED_PLL_LPDP 0.769V - 0.85V @ 4mA MAX
VDD_FIXED_LPDP_RX 0.769V - 0.85V @ 50mA MAX
PP0V8_SOC_FIXED_S1

C1395 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1396 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

Dan LPDP Lane Assignment
Wide: 0-2
Tele: 3-5
Fcam: 6-7

Justin LPDP Lane Assignment
Wide: 2-4
Tele: 5-7
Fcam: 0-1

LPD Assigned off page

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		AM10	VDD12_LPDP_TX			
		F27	VDD12_LPDP_RX			
		F29				
		AM13	VDD12_PLL_LPDP			
		AM12	VDD_FIXED_PLL_LPDP			
		AM11	VDD_FIXED_LPDP_TX			
		F31	VDD_FIXED_LPDP_RX			
		G28				
90_LPDP_WIDE_TO_AP_D0_P	A25	LPDPRX_RX_D0_P		LPDP_TX0P	AY14	NC_LPDP_TX0_P
90_LPDP_WIDE_TO_AP_D0_N	B25	LPDPRX_RX_D0_N		LPDP_TX0N	AW14	NC_LPDP_TX0_N
90_LPDP_WIDE_TO_AP_D1_P	B26	LPDPRX_RX_D1_P		LPDP_TX1P	AY13	NC_LPDP_TX1_P
90_LPDP_WIDE_TO_AP_D1_N	C26	LPDPRX_RX_D1_N		LPDP_TX1N	AW13	NC_LPDP_TX1_N
90_LPDP_WIDE_TO_AP_D2_P	A27	LPDPRX_RX_D2_P		LPDP_TX2P	AY12	NC_LPDP_TX2_P
90_LPDP_WIDE_TO_AP_D2_N	B27	LPDPRX_RX_D2_N		LPDP_TX2N	AW12	NC_LPDP_TX2_N
90_LPDP_TELE_TO_AP_D0_P	B28	LPDPRX_RX_D3_P		LPDP_TX3P	AY11	NC_LPDP_TX3_P
90_LPDP_TELE_TO_AP_D0_N	C28	LPDPRX_RX_D3_N		LPDP_TX3N	AW11	NC_LPDP_TX3_N
90_LPDP_TELE_TO_AP_D1_P	B30	LPDPRX_RX_D4_P				
90_LPDP_TELE_TO_AP_D1_N	C30	LPDPRX_RX_D4_N				
90_LPDP_TELE_TO_AP_D2_P	A31	LPDPRX_RX_D5_P		LPDP_AUX_P	AY10	NC_LPDP_AUX_P
90_LPDP_TELE_TO_AP_D2_N	B31	LPDPRX_RX_D5_N		LPDP_AUX_N	AW10	NC_LPDP_AUX_N
90_LPDP_FCAM_TO_AP_D0_P	B32	LPDPRX_RX_D6_P				
90_LPDP_FCAM_TO_AP_D0_N	C32	LPDPRX_RX_D6_N		EDP_HPD	AF2	NC_EPD_HPD
				DP_WAKEUP	AF4	NC_DP_WAKEUP
90_LPDP_FCAM_TO_AP_D1_P	A33	LPDPRX_RX_D7_P				
90_LPDP_FCAM_TO_AP_D1_N	B33	LPDPRX_RX_D7_N				
LPDP_WIDE_BI_AP_AUX	D23	LPDPRX_AUX_D0_P				
LPDP_TELE_BI_AP_AUX	D24	LPDPRX_AUX_D1_P				
NC_LPDP_D2_AUX	C24	LPDPRX_AUX_D2_P				
NC_LPDP_D3_AUX	D25	LPDPRX_AUX_D3_P				
NC_LPDP_D4_AUX	D27	LPDPRX_AUX_D4_P				
NC_LPDP_D5_AUX	D29	LPDPRX_AUX_D5_P				
NC_LPDP_D6_AUX	D31	LPDPRX_AUX_D6_P				
LPDP_FCAM_BI_AP_AUX	D33	LPDPRX_AUX_D7_P				
LPDPRX_RCAL_POS	A29	LPDPRX_RCAL_P		LPDP_RCAL_P	AU10	NC_LPDP_RCAL_P
	B29	LPDPRX_RCAL_N		LPDP_RCAL_N	AT10	NC_LPDP_RCAL_N

R1300 200 1% 1/32W MF 01005 ROOM=SOC
LPDPRX_RCAL_NEG
C1301 10PF 5% 16V CERM 01005 ROOM=SOC

PAGE TITLE
SOC: LPDP

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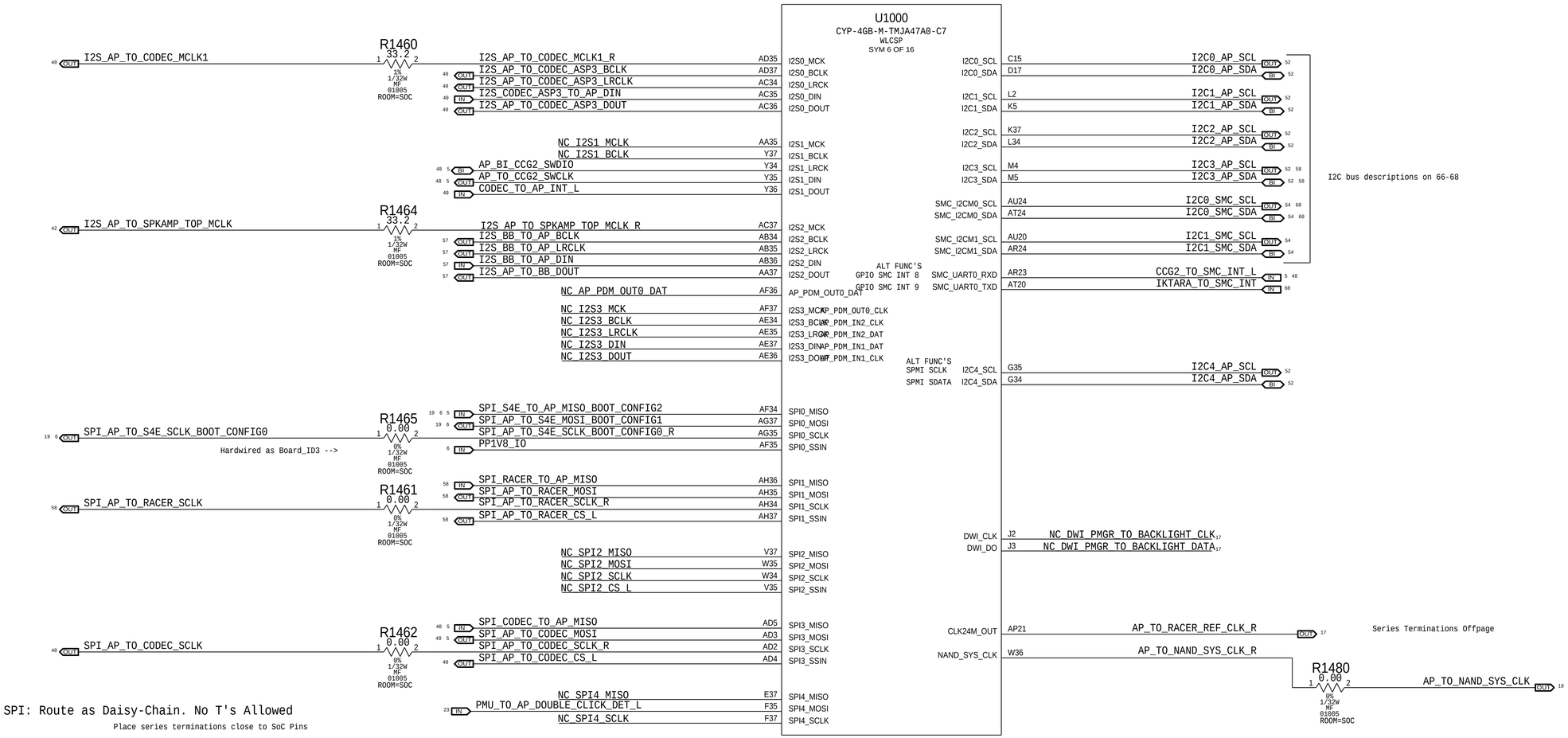
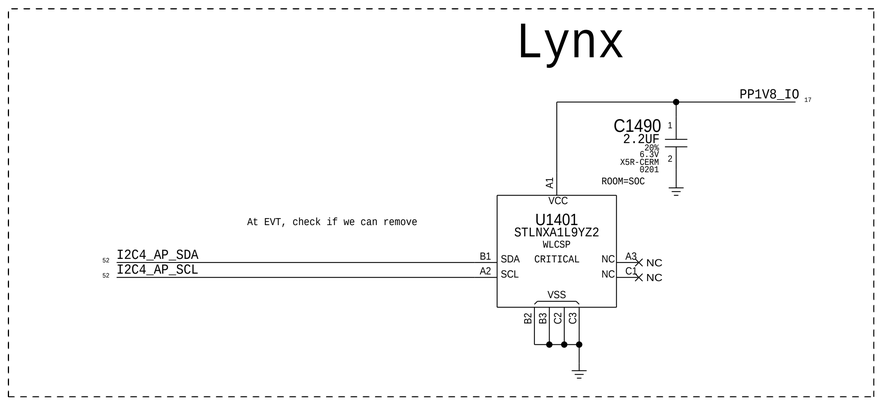
SOC - SERIAL INTERFACES





PAGE TITLE	SOC: SERIAL
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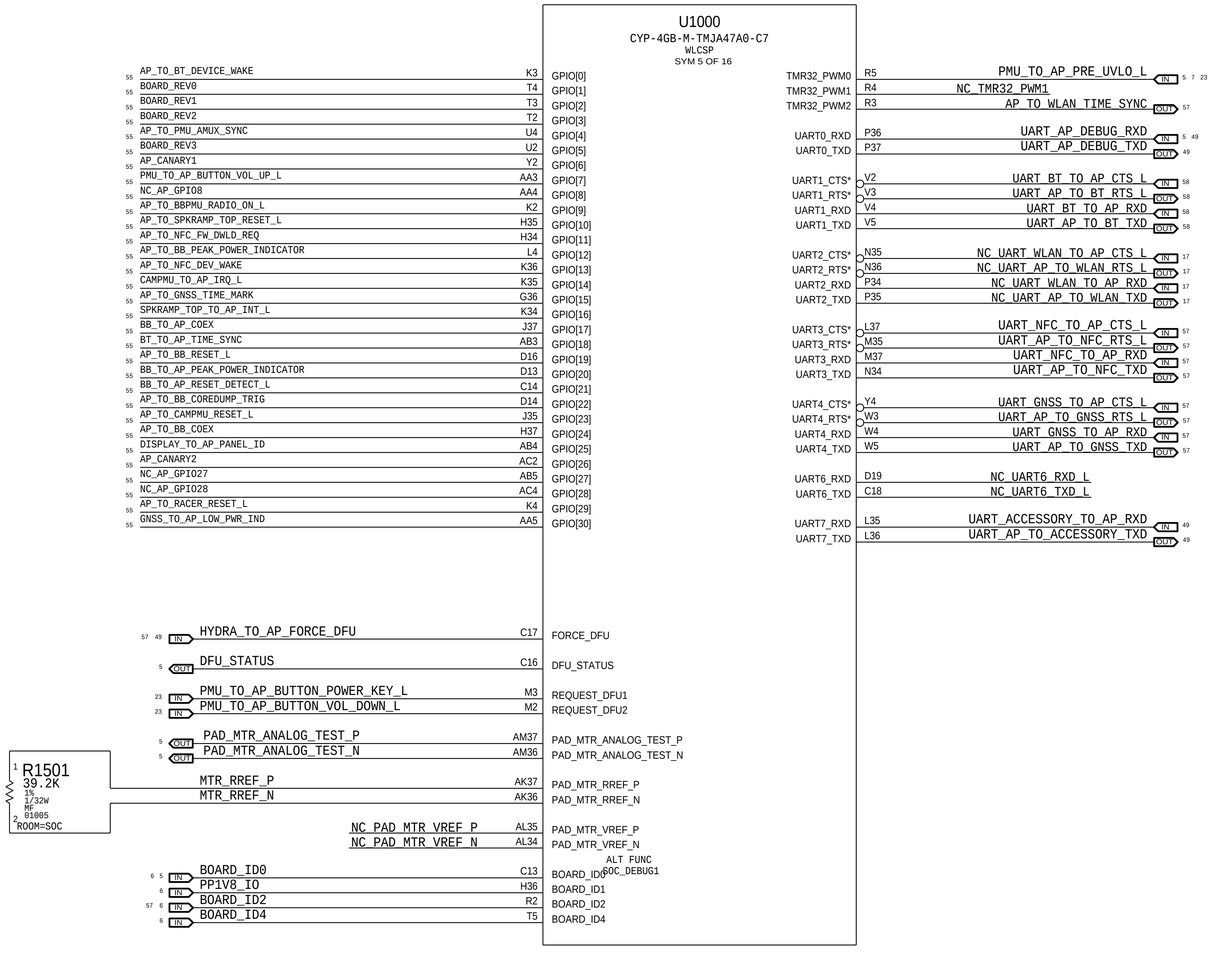
SOC - GPIO INTERFACES

GPIOs are wired on page 70



PAGE TITLE

SOC: GPIO & UART

Apple Inc.

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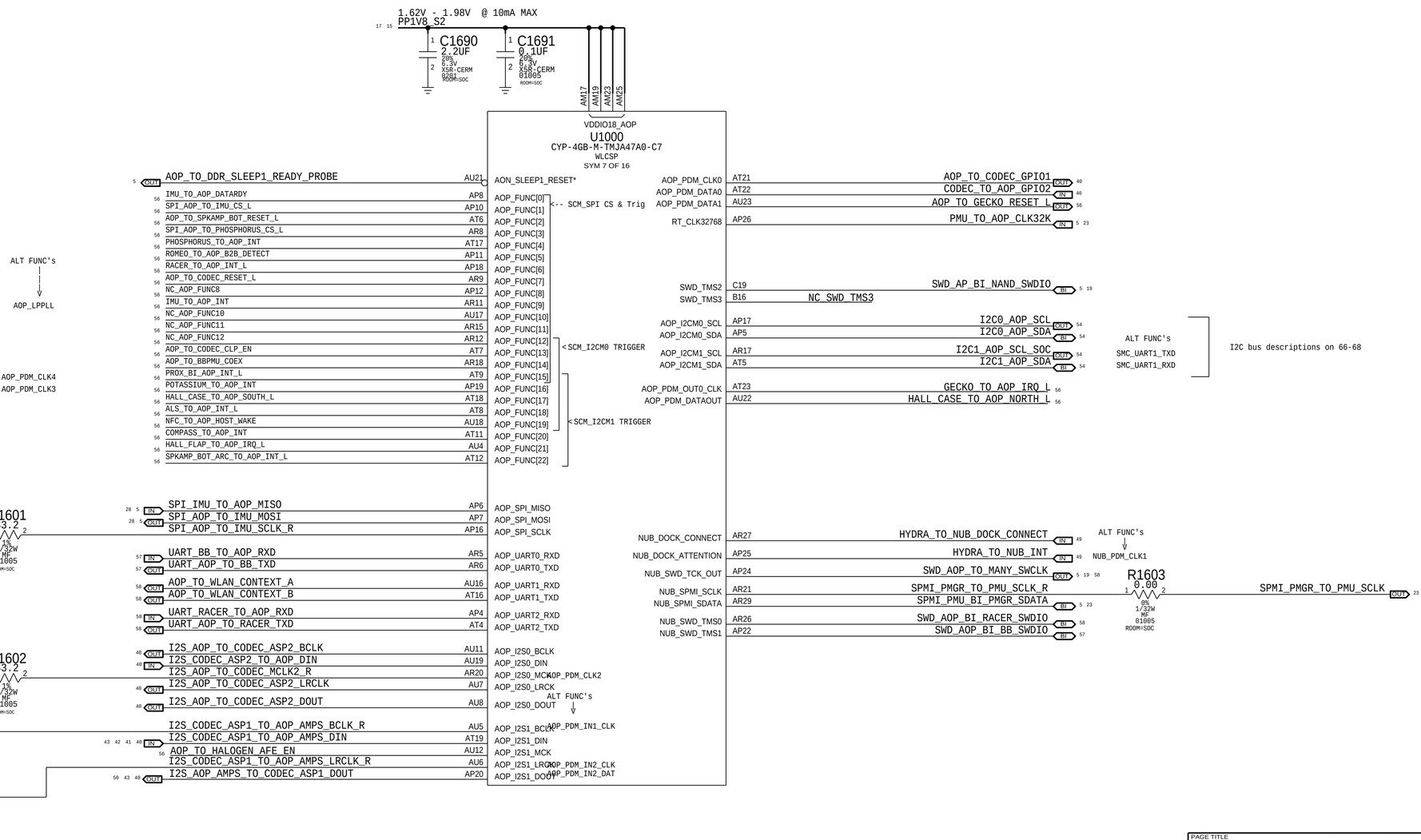
SOC - AOP



PAGE TITLE

SOC: AOP

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SOC - CPU, GPU & SOC RAILS

1.06V @ 13.8A MAX
0.905V @ 12.9A MAX
0.527V @ 2.4A MAX

17 PP_CPU_PCORE

C1702 4UF 20% 4V X5R 0201 ROOM=SOC
C1703 4UF 20% 4V X5R 0201 ROOM=SOC

C1704 14UF 20% 4V X5R 0402-D2X-1
C1705 14UF 20% 4V X5R 0402-D2X-1
C1706 14UF 20% 4V X5R 0402-D2X-1
C1707 14UF 20% 4V X5R 0402-D2X-1

C1708 14UF 20% 4V X5R 0402-D2X-1
C1709 14UF 20% 4V X5R 0402-D2X-1
C1710 14UF 20% 4V X5R 0402-D2X-1
C1711 14UF 20% 4V X5R 0402-D2X-1
C1712 14UF 20% 4V X5R 0402-D2X-1
C1713 14UF 20% 4V X5R 0402-D2X-1

VDD_LOW: 0.691V - 0.756V @ 75mA MAX
VDD_LOW_ULPPLL: 0.691V - 0.756V @ 0.3mA MAX
17 PP0V7_VDD_LOW_S2

C1751 4UF 20% 4V X5R 0201 ROOM=SOC
C1750 4UF 20% 4V X5R 0201 ROOM=SOC

R1702 100 5% 1/32W NF 01005 ROOM=SOC
PP0V7_VDD_LOW_ULPPLL_R
C1742 4UF 20% 4V X5R 0201 ROOM=SOC

R1701 10 5% 1/32W NF 01005 ROOM=SOC
PP0V7_VDD_LOW_FLPPLL_R
C1743 0.47UF 20% 6.3V X5R 01005 ROOM=SOC

1.02V @ 2.1A MAX
0.975V @ 1.4A MAX
0.765V @ 0.33A MAX
17 PP_CPU_SRAM

C1772 14UF 20% 4V X5R 0402-D2X-1
C1773 14UF 20% 4V X5R 0402-D2X-1

1.06V @ 0.6A MAX
0.725V @ 0.41A MAX
0.685V @ 0.39A MAX
17 PP_GPU_SRAM

C1781 14UF 20% 4V X5R 0402-D2X-1
C1782 14UF 20% 4V X5R 0402-D2X-1

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AD9, AD17, AE10, AE12, AE16, AF13, AF15, AG10, AJ10, AK13, AK15, V11, V13, W10, W14, W16, Y9, Y17 → VDD_PCPU
AL16, AL18, AL22, AL24 → VDD_LOW
AM21 → VDD_LOW_ULPPLL
AL20 → VDD_LOW_FLPPLL
AB9, AB17, AE14, AF11, AH15, AK11, N12, U10, W12 → VDD_CPU_SRAM
F13, H11, H15, H19, J24, K13, K21, G22, M15, M19, M23 → VDD_GPU_SRAM

1.06V @ 14.5A MAX
0.725V @ 6.3A MAX
0.570V @ 3.1A MAX
PP_GPU 17

C1730 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1731 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

C1732 14UF 20% 4V X5R 0402-D2X-1
C1733 14UF 20% 4V X5R 0402-D2X-1
C1734 14UF 20% 4V X5R 0402-D2X-1
C1735 14UF 20% 4V X5R 0402-D2X-1
C1736 14UF 20% 4V X5R 0402-D2X-1

C1737 14UF 20% 4V X5R 0402-D2X-1
C1738 14UF 20% 4V X5R 0402-D2X-1
C1739 14UF 20% 4V X5R 0402-D2X-1

VDD_GPU: F11, F15, G10, G12, G14, G16, K25, G20, G24, G26, H13, H17, H21, H25, J12, J14, J20, J22, H23, J26, K11, K15, K23, L10, L12, L14, L20, L22, L24, L26, M13, M17, M21, M25, N20, N22, N24, N26

0.945V @ 2.9A MAX
0.626V @ 1.2A MAX
0.517V @ 0.62A MAX
PP_CPU_ECORE 17

C1791 14UF 20% 4V X5R 0402-D2X-1
C1792 14UF 20% 4V X5R 0402-D2X-1
C1793 14UF 20% 4V X5R 0402-D2X-1
C1794 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

VDD_ECPU: N10, P9, P13, T9, T13, V9, U11

VDD_FIXED_PCPU: 0.81V @ 5mA
VDD_FIXED_MTR 0.769V - 0.85V @ TBDmA
VDD_FIXED_ECPU: 0.769V - 0.85V @ 5mA
VDD_FIXED_ECPU: M11 → PP0V8_SOC_FIXED_S1 14 17
VDD_FIXED_MTR: AD31 → PP0V8_SOC_FIXED_S1 7 8 9 10 17
VDD_FIXED_PCPU: U12 → PP0V8_SOC_FIXED_S1 14 17

VDD_FIXED_PLL_SOC: AE24
VDD_FIXED_PLL_GPU: AE22
VDD_FIXED_PLL_ANE: AD23
VDD_FIXED_PLL_DDR3: 0.81V @ 8mA
VDD_FIXED_PLL_DDR2: 0.91V @ 8mA
PP0V8_SOC_FIXED_S1 14 17
VDD_FIXED_PLL_DDR0: AH5
VDD_FIXED_PLL_DDR1: AJ29
VDD_FIXED_PLL_DDR2: D7
VDD_FIXED_PLL_DDR3: N29
VDD_FIXED_PLL_SOC: 0.81V @ 9mA
VDD_FIXED_PLL_GPU: 0.81V @ 5mA
VDD_FIXED_PLL_ANE: 0.81V @ 5mA
VDD_FIXED_PLL_DDR0: 0.81V @ 8mA
VDD_FIXED_PLL_DDR1: 0.81V @ 8mA
VDD_FIXED_PLL_LPDP: 0.81V @ 2mA

VDD12_PLL_SOC: AE23
VDD12_PLL_ANE: AD24
VDD12_PLL_PCPU: U13
VDD12_PLL_ECPU: M12
VDD12_PLL_GPU: AD22
VDD12_PLL_SOC: 1.14 - 1.26V @ 9mA MAX
VDD12_PLL_ANE: 1.14 - 1.26V @ 7mA MAX
VDD12_PLL_PCPU: 1.14 - 1.26V @ 7mA MAX
VDD12_PLL_ECPU: 1.14 - 1.26V @ 7mA MAX
VDD12_PLL_GPU: 1.14 - 1.26V @ 7mA MAX
PP1V2_SOC 17

C1720 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C1721 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C1722 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C1723 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

Remote sense XW's for Buck0 Buck1 and Buck11 live off page for dev board compapability

0.783V @ 4.2A MAX
0.661V @ 2.6A MAX
0.595V @ 2.1A MAX
PP_SOC_S1 17

C1760 4UF 20% 4V X5R 0201 ROOM=SOC
C1761 4UF 20% 4V X5R 0201 ROOM=SOC
C1765 4UF 20% 4V X5R 0201 ROOM=SOC

C1762 14UF 20% 4V X5R 0402-D2X-1
C1763 14UF 20% 4V X5R 0402-D2X-1
C1764 14UF 20% 4V X5R 0402-D2X-1

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WLCSP
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VDD_SOC: AA8, AA18, AA22, AA24, AA28, AA30, AB19, AB21, AB25, AB27, AC18, AC22, AC24, AC28, AD19, AD21, AD25, AD27, AE18, AE28, AF19, AF21, AF25, AF27, AG18, AG22, AG24, AG28, AH10, AH19, AH25, AH27, AJ16, AJ18, AJ22, AJ24, AJ28, AK19, AK21, AK25, F22, G19, H27, J10, J28, K27, L28, M27, N16, N18, N28, P15, P19, P25, P27, R16, R18, R22, R24, R28, R30, T15, T19, T21, T25, T27, U8, U16, U18, U22, U24, U28, U30, V15, V19, V21, V25, V27, W18, W22, W24, W28, W30, Y19, Y21, Y25, Y27

PAGE TITLE	SOC: POWER (1/3)
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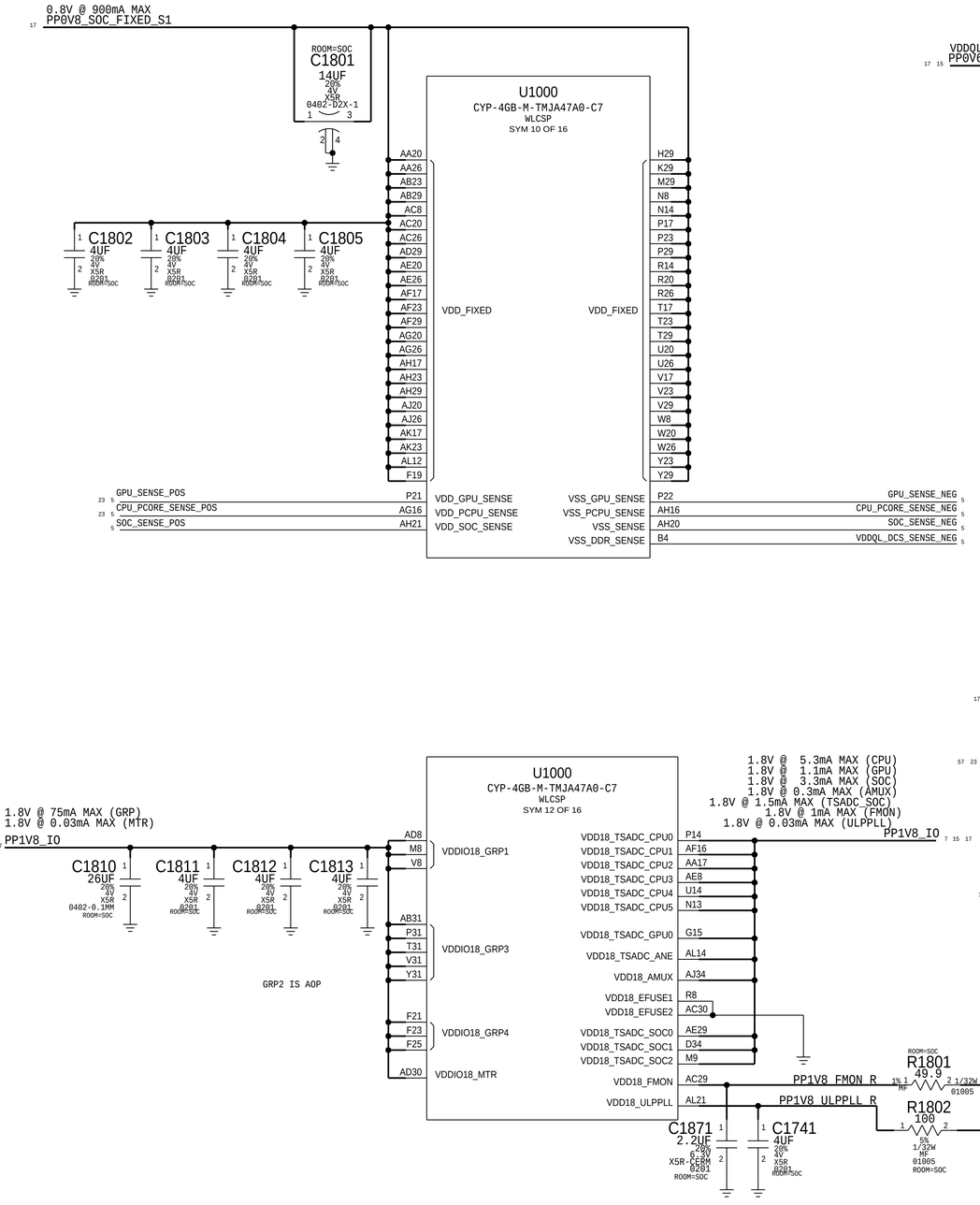
SOC - CPU, GPU & SOC RAILS



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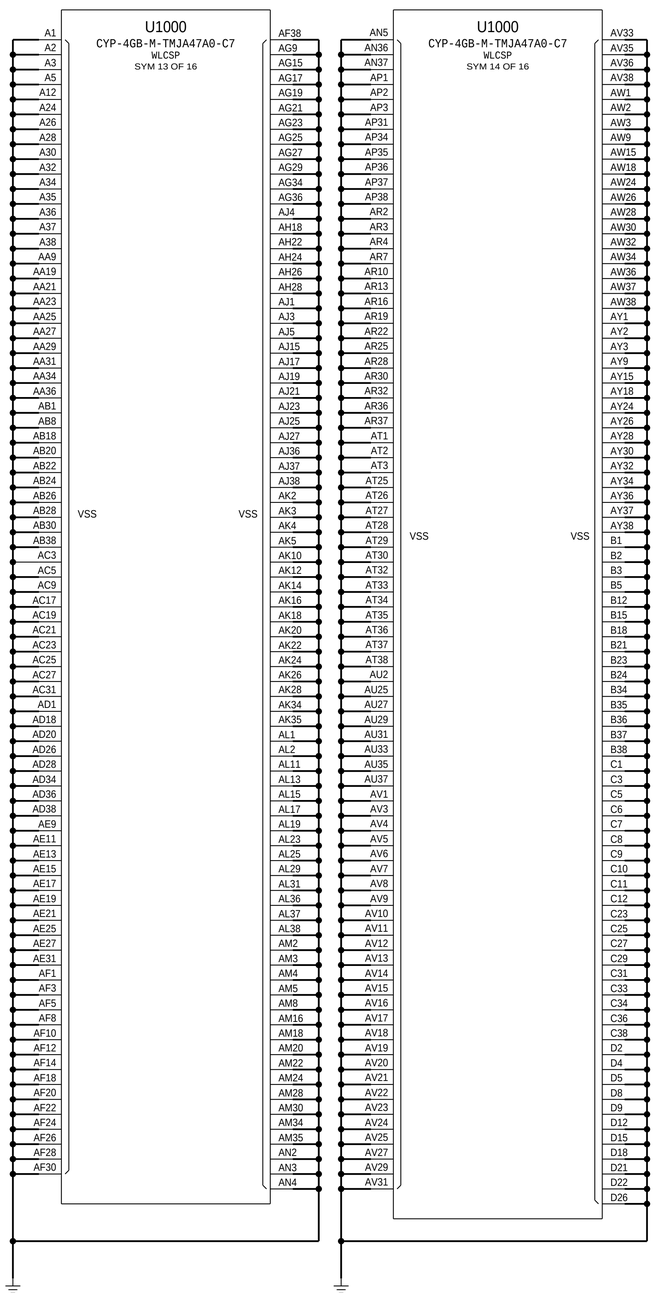
SOC - POWER SUPPLIES



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Medusa Compatibility

PP_VDD_MAIN (MAKE_BASE=TRUE) → PP_VDD_MAIN ×16
PP_VDD_BOOST (MAKE_BASE=TRUE) → PP_VDD_BOOST ×5
PP2V5_LDO0_S2 (MAKE_BASE=TRUE) → PP2V5_LDO0_S2
PP1V1_S2 (MAKE_BASE=TRUE) → PP1V1_S2 ×3
PP1V26_S2 (MAKE_BASE=TRUE) → PP1V26_S2
PP_CPU_PCORE (MAKE_BASE=TRUE) → PP_CPU_PCORE
PP_GPU (MAKE_BASE=TRUE) → PP_GPU
PP_SOC_S1 (MAKE_BASE=TRUE) → PP_SOC_S1
PP1V2_SOC (MAKE_BASE=TRUE) → PP1V2_SOC ×3
PP1V8_ALWAYS (MAKE_BASE=TRUE) → PP1V8_ALWAYS
PP1V8_S2 (MAKE_BASE=TRUE) → PP1V8_S2 ×3
PP1V8_IO (MAKE_BASE=TRUE) → PP1V8_IO ×5
PP_CPU_SRAM (MAKE_BASE=TRUE) → PP_CPU_SRAM
PP_GPU_SRAM (MAKE_BASE=TRUE) → PP_GPU_SRAM
PP_DCS_S1 (MAKE_BASE=TRUE) → PP_DCS_S1
PP0V6_VDDQL_S1 (MAKE_BASE=TRUE) → PP0V6_VDDQL_S1
PP_CPU_ECORE (MAKE_BASE=TRUE) → PP_CPU_ECORE
PP3V3_USB (MAKE_BASE=TRUE) → PP3V3_USB
PP0V7_VDD_LOW_S2 (MAKE_BASE=TRUE) → PP0V7_VDD_LOW_S2
PP0V8_SOC_FIXED_S1 (MAKE_BASE=TRUE) → PP0V8_SOC_FIXED_S1 ×3
GND (MAKE_BASE=TRUE)

PCIE Series Caps

90_PCIE_NAND_TO_AP_RXD_C_P	C1100 0.22UF	90_PCIE_NAND_TO_AP_RXD_P	IN
90_PCIE_NAND_TO_AP_RXD_C_N	C1101 0.22UF	90_PCIE_NAND_TO_AP_RXD_N	IN
90_PCIE_AP_TO_NAND_TXD_C_P	C1102 0.22UF	90_PCIE_AP_TO_NAND_TXD_P	OUT
90_PCIE_AP_TO_NAND_TXD_C_N	C1103 0.22UF	90_PCIE_AP_TO_NAND_TXD_N	OUT
90_PCIE_WLAN_TO_AP_RXD_C_P	C1130 0.1UF	90_PCIE_WLAN_TO_AP_RXD_P	IN
90_PCIE_WLAN_TO_AP_RXD_C_N	C1131 0.1UF	90_PCIE_WLAN_TO_AP_RXD_N	IN
90_PCIE_AP_TO_WLAN_TXD_C_P	C1132 0.1UF	90_PCIE_AP_TO_WLAN_TXD_P	OUT
90_PCIE_AP_TO_WLAN_TXD_C_N	C1133 0.1UF	90_PCIE_AP_TO_WLAN_TXD_N	OUT
90_PCIE_BB_TO_AP_RXD_C_P	C1120 0.1UF	90_PCIE_BB_TO_AP_RXD_P	IN
90_PCIE_BB_TO_AP_RXD_C_N	C1121 0.1UF	90_PCIE_BB_TO_AP_RXD_N	IN
90_PCIE_AP_TO_BB_TXD_C_P	C1122 0.1UF	90_PCIE_AP_TO_BB_TXD_P	OUT
90_PCIE_AP_TO_BB_TXD_C_N	C1123 0.1UF	90_PCIE_AP_TO_BB_TXD_N	OUT

All: GND_VOID, 20%, 6.3V, X5R, 01005-1, ROOM=SOC. C1123: CRITICAL, MAKE_TYPE=01005.

FF Specific CLK Series Terminations

AP_TO_TELE_CLK_R	R1241 33.2 1% 1/32W MF 01005 ROOM=SOC	AP_TO_TELE_CLK OUT
AP_TO_FCAM_JULIET_RIGEL_CLK_R	R1242 33.2 1% 1/32W MF 01005 ROOM=SOC	AP_TO_JULIET_CLK OUT
	R1243 33.2 1% 1/32W MF 01005 ROOM=SOC	AP_TO_RIGEL_CLK OUT
	R1244 33.2 1% 1/32W MF 01005 ROOM=SOC	AP_TO_FCAM_CLK OUT
AP_TO_RACER_REF_CLK_R	R1481 0.00 0% 1/32W MF 01005 ROOM=SOC	AP_TO_RACER_REF_CLK OUT

Dev Board Compatibility FB XW's

PP_GPU → OMIT XW1731 SHORT-20L-0.05MM-SM ROOM=SOC → BUCK1_FB OUT
NO_XNET_CONNECTION

Place near SOC Balls

PP_CPU_ECORE → OMIT XW1790 SHORT-20L-0.05MM-SM ROOM=SOC → BUCK11_FB OUT
PP_CPU_PCORE → OMIT XW1701 SHORT-20L-0.05MM-SM ROOM=SOC → BUCK0_FB OUT

PP1V26_S2 → U4002 SCY99224-1.20V WLCSP CRITICAL ROOM=B2B_PEARL (IN A1, EN B1, OUT A2, GND B2) → PP1V1_CAM_JULIET_DVDD
CAMPMU_TO_JULIET_DVDD_LDO_EN → EN
C4080 0.47UF 20% 6.3V X5R 01005 ROOM=B2B_PEARL
C4081 0.47UF 20% 6.3V X5R 01005 ROOM=B2B_PEARL
C4082 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=B2B_PEARL

FF Touch Compatibility Compatibility

PMU_TO_TOUCH_CLK32K → PMU_TO_TOUCH_CLK32K (MAKE_BASE=TRUE)
ACORN_GECKO_ANSEL_TO_PMU_ADC (MAKE_BASE=TRUE)
C3072 1000PF 10% 16V C0G 01005 ROOM=PMU — Place Near PMU

FF Display Compatibility

NC_DISPLAY_TO_CHESTNUT_PWR_EN → NC_DISPLAY_TO_CHESTNUT_PWR_EN (MAKE_BASE=TRUE)

Dev Board Power Compability

Should live on PMU LDO page by caps

PP_VDD_MAIN → OMIT XW2990 SHORT-20L-0.05MM-SM ROOM=PMU → VDD_MAIN_SNS OUT
GND (MAKE_BASE=TRUE)
BUCK11_FB → BUCK11_FB (MAKE_BASE=TRUE)

NC_UART_WLAN_TO_AP_CTS_L	NC_UART_WLAN_TO_AP_CTS_L IN
NC_UART_AP_TO_WLAN_RTS_L	NC_UART_AP_TO_WLAN_RTS_L OUT
NC_UART_WLAN_TO_AP_RXD	NC_UART_WLAN_TO_AP_RXD IN
NC_UART_AP_TO_WLAN_TXD	NC_UART_AP_TO_WLAN_TXD OUT

Dev Board Compatiblity GNDs

GND ×16 (MAKE_BASE=TRUE)

UF Dam Caps

PP0V6_VDDQL_S1 → C2000 220PF 5% 25V C0G 01005 ROOM=SOC

GND ×5
NC_DWI_PMGR_TO_BACKLIGHT_CLK → NC_DWI_PMGR_TO_BACKLIGHT_CLK (MAKE_BASE=TRUE)
NC_DWI_PMGR_TO_BACKLIGHT_DATA → NC_DWI_PMGR_TO_BACKLIGHT_DATA (MAKE_BASE=TRUE)

SYNC_MASTER
SYNC_DATE=04/17/2017

PAGE TITLE: SOC: DEV BOARD ALIASES

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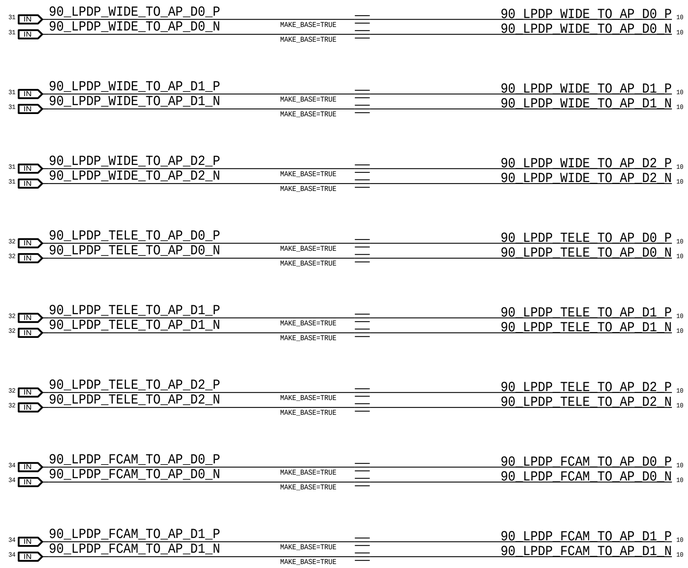

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SOC: LPDP ALIASES

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S4E NAND

391mA MAX
PP1V8_IO
C2626 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2610 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C2629 15UF 20% 6.3V CERM 0402-0.1MM ROOM=NAND
C2630 15UF 20% 6.3V CERM 0402-0.1MM ROOM=NAND
C2624 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2641 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2643 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2645 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2647 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2611 220PF 5% 25V C0G 01005 ROOM=NAND
C2612 220PF 5% 25V C0G 01005 ROOM=NAND
C2618 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2614 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2615 47PF 5% 16V CERM 01005 ROOM=NAND
C2617 22PF 5% 16V CERM 01005 ROOM=NAND
932mA MAX
PP0V9_NAND
C2602 26UF 20% 4V X5R 0402-0.1MM ROOM=NAND
C2605 26UF 20% 4V X5R 0402-0.1MM ROOM=NAND
C2600 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2601 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2622 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2627 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2640 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2642 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2644 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2646 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2603 220PF 5% 25V C0G 01005 ROOM=NAND
C2606 220PF 5% 25V C0G 01005 ROOM=NAND
C2609 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2607 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2608 47PF 5% 16V CERM 01005 ROOM=NAND
C2604 22PF 5% 16V CERM 01005 ROOM=NAND
XW2600 SHORT-26L-0.05MM-SM ROOM=NAND
OMIT
Place near C2629
1100mA MAX (1us peak power)
PP2V63_NAND
C2613 15UF 20% 6.3V CERM 0402-0.1MM ROOM=NAND
C2616 15UF 20% 6.3V CERM 0402-0.1MM ROOM=NAND
C2619 15UF 20% 6.3V CERM 0402-0.1MM ROOM=NAND
C2621 15UF 20% 6.3V CERM 0402-0.1MM ROOM=NAND
C2649 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2650 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2651 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2652 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2638 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2639 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2634 47PF 5% 16V CERM 01005 ROOM=NAND
C2635 22PF 5% 16V CERM 01005 ROOM=NAND
C2636 220PF 5% 25V C0G 01005 ROOM=NAND
C2637 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
R2604 3.01K 1% 1/32W MF 01005 ROOM=NAND
R2600 100 0.1% 1/32W MF 01005 ROOM=NAND
R2601 300 0.1% 1/32 MF 01005 ROOM=NAND
Board trace <= 0.2Ohm

NAND_ANI1_VREF
NAND_ANI0_VREF

U2600
H23Q2T8QK6MES-BC
LGA
ROOM=NAND
BOM OPTION/UNIT TABLE
CRITICAL

AP_TO_NAND_SYS_CLK	M3	CLK_IN
90_PCIE_AP_TO_NAND_REFCLK_P	K11	PCIE_REFCLK_P
90_PCIE_AP_TO_NAND_REFCLK_N	J12	PCIE_REFCLK_M
PCIE_NAND_BI_AP_CLKREQ_L	P5	PCIE_CLKREQ_N
PCIE_NAND_RESREF	H7	PCI_RESREF
90_PCIE_AP_TO_NAND_TXD_P	M11	PCIE_RX0_P
90_PCIE_AP_TO_NAND_TXD_N	N12	PCIE_RX0_M
90_PCIE_NAND_TO_AP_RXD_P	R12	PCIE_TX0_P
90_PCIE_NAND_TO_AP_RXD_N	T11	PCIE_TX0_M
AP_TO_NAND_RESET_L	L4	RESET*
	G10	TRST*
NAND_ZQ_ANI	K3	ZQ_C
NAND_ZQ_NAND	C10	ZQ_N

B3	EXT_D0/BOOT0	PMU_TO_NAND_LOW_BATT_BOOT_L
C4	EXT_D1/BOOT1	AP_TO_NAND_FW_STRAP
B5	EXT_D2/BOOT2/SPINAND_SCLK	SPI_AP_TO_S4E_SCLK_BOOT_CONFIG0
C6	EXT_D3/SWD_UID0/SPINAND_MISO	SPI_S4E_TO_AP_MISO_BOOT_CONFIG2
B7	EXT_D4/UART_RX	NC
C8	EXT_D5/SWD_UID1/SPINAND_MOSI	SPI_AP_TO_S4E_MOSI_BOOT_CONFIG1
B9	EXT_D6/UART_TX	NC
B11	EXT_D7/SPF	SYSTEM_ALIVE
E8	EXT_NCE/PERST*	PCIE_AP_TO_NAND_PERST_L
D7	EXT_NRE/JTAG_TMS	SWD_AP_BI_NAND_SWDIO
E6	EXT_NWE/JTAG_TCK	SWD_AOP_TO_MANY_SWCLK
E4	EXT_RNB/JTAG_TDO	
D5	EXT_CLE/JTAG_TDI	NC
D9	EXT_ALE/JTAG_SEL	
T3	DROOP_N	
G2	WP_N	PP1V8_IO

PCI_AVDD_CLK_1 N6, PCI_AVDD_CLK_2 M9, PCI_AVDD_H J6, PCI_VDD_1 N8, PCI_VDD_2 J8, AVDD18_PLL L2, ANI0_VREF G12, ANI1_VREF J4, VDD G6 G8 L6 L8 R6 R8, VDDIO E2 E10 J2 K9 N2 T5 P9, VCC D3 E12 G4 L12 R2, VDD_PLL R4, VPP F3 NC
VSS: A2 A4 A6 A8 A10 A12 B1 B13 C2 C12 D1 D11 D13 F1 F5 F7 F9 F11 F13 H1 H3 H5 H9 H11 H13 J10 K1 K5 K7 K13 L10 M1 M5 M7 M13 N4 N10 P1 P3 P7 P11 P13 R10 T1 T7 T9 T13 U2 U4 U6 U8 U10 U12

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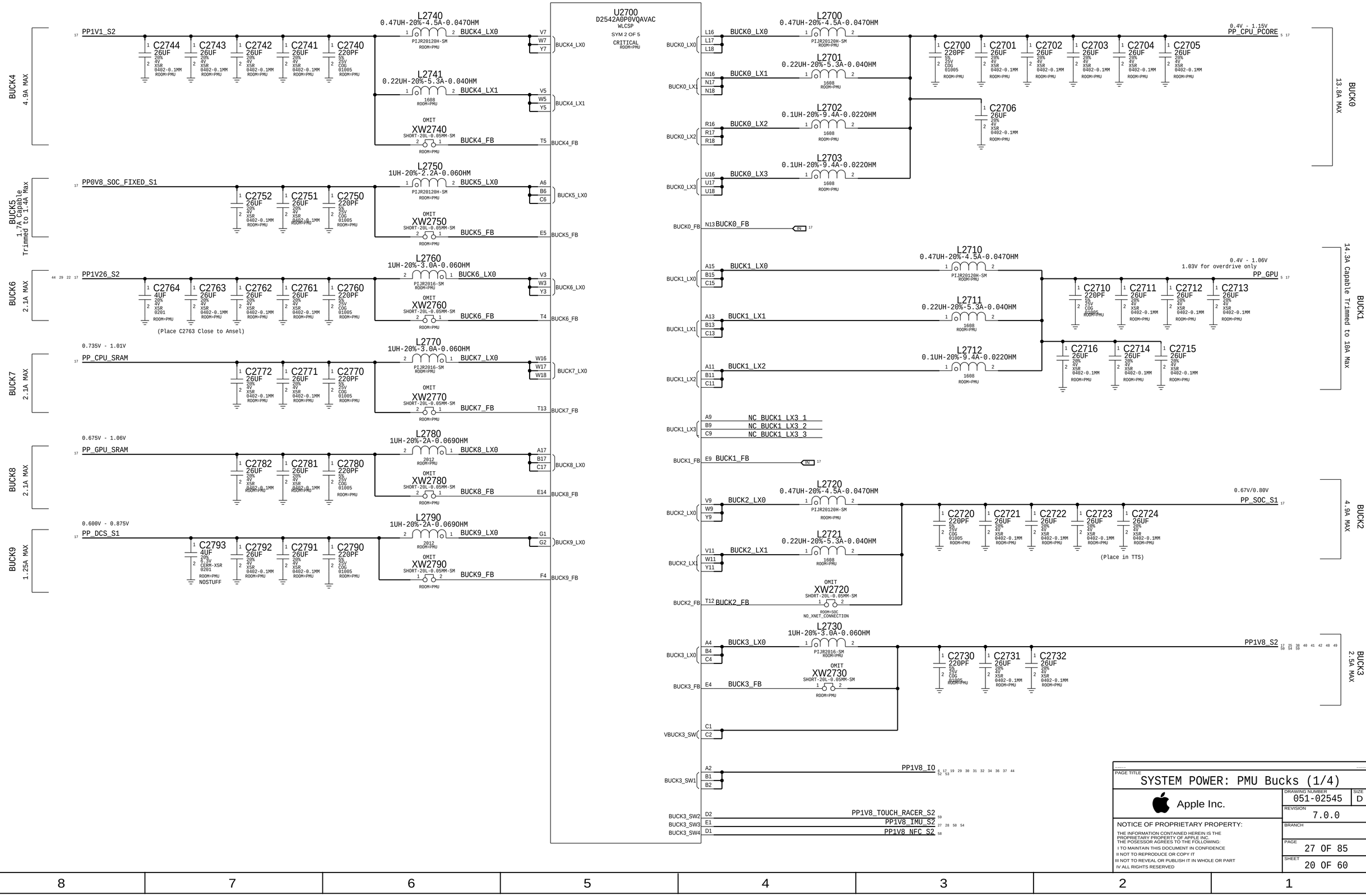

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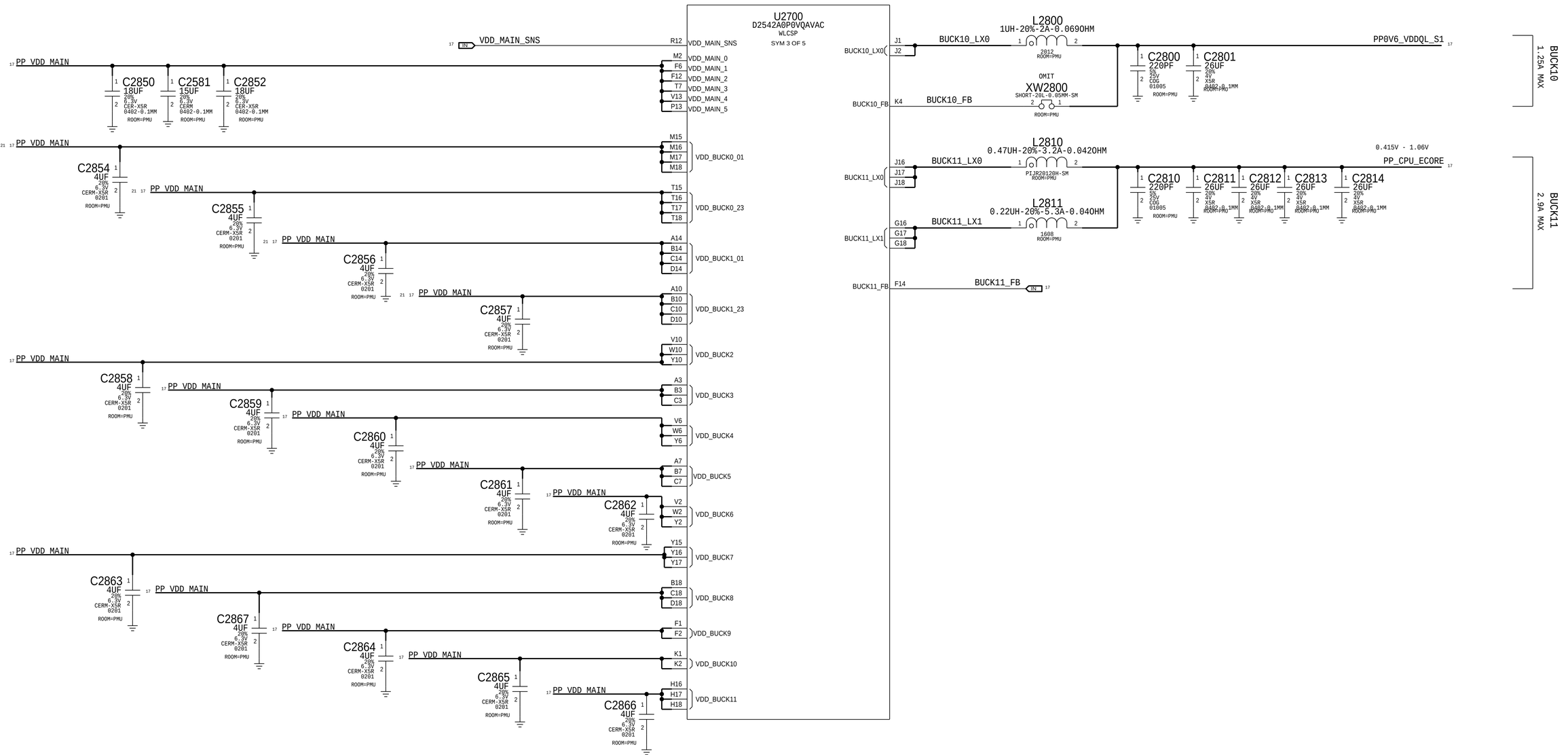
PMU - BUCKS



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PMU - LDOs

XW to VDD_MAIN_SNS lives on alias page

44 43 42 41 36 33 29 26 24 17 59 47 45 PP_VDD_MAIN

C2991 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=PMU

59 47 46 40 36 29 24 17 PP_VDD_BOOST

OMIT XW2995 SHORT-20L-0.05MM-SM ROOM=PMU

C2970 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU

C2971 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU

23 OUT PMU_LDO5_UVLO_DET

U2700 D2542A0P0VQAVAC WLCSP SYM 5 OF 5

A1 A18 D5 D7 D8 D11 D13 D15 D16 D17 E11 E16 E18 G3 G15 J3 J15 K3 K14 L15 M6 M8 N9 N10 N11 N14 N15 P8 P11 P14 R8 R9 R10 R11 R14 R15 T3 T6 T8 U4 U5 U6 U8 U9 U11 U12 U15 V15 Y1 Y18 — VSS

23 PMU_VSS_RTC P2 — VSS_XTAL

VSSA_BUCK0 T14
VSSA_BUCK1 D9
VSSA_BUCK2 U10
VSSA_BUCK3 D3
VSSA_BUCK4 U7
VSSA_BUCK5 D6
VSSA_BUCK6 U3
VSSA_BUCK7 W15
VSSA_BUCK8 E17
VSSA_BUCK9 D4
VSSA_BUCK10 H3
VSSA_BUCK11 H15

VSS_SW_BUCK_0 — P15 P16 P17 P18

VSS_SW_BUCK_0_11 — K15 K16 K17 K18

VSS_SW_BUCK0_7 — V16 V17 V18

VSS_SW_BUCK1 — A12 B12 C12 D12

VSS_SW_BUCK1_5 — A8 B8 C8

VSS_SW_BUCK2 — V12 W12 Y12

VSS_SW_BUCK2_4 — V8 W8 Y8

VSS_SW_BUCK4_6 — V4 W4 Y4

VSS_SW_BUCK5_3 — A5 B5 C5

VSS_SW_BUCK8_1 — A16 B16 C16

VSS_SW_BUCK9_10 — H1 H2

VSS_SW_BUCK11 — F16 F17 F18

U2700 D2542A0P0VQAVAC WLCSP SYM 1 OF 5

17 PP_VDD_MAIN — R6 VDD_LDO0
17 PP_VDD_BOOST — M4 VDD_LDO1_3
17 PP_VDD_MAIN — R5 VDD_LDO2
17 PP1V1_S2 — T1 VDD_LDO4
17 PP_VDD_BOOST — V1 VDD_LDO5
W1 VDD_LDO5
17 PP_VDD_BOOST — M1 VDD_LDO6
17 PP_VDD_BOOST — L1 VDD_BYPASS

C2980 4UF 20% 4V X5R 0201 ROOM=CAM_PMU

This cap also services LDO 14

L4 VDD_LDO7
R1 VDD_LDO8
L6 VDD_LDO9
17 PP_VDD_BOOST — R7 VDD_LDO10
17 PP1V26_S2 — N4 VDD_LDO11_13

SHORTED TO BOOST ON D3X

17 GND — R4 VDD_LDO12
17 PP1V1_S2 — R3 VDD_LDO14
17 PP2V5_LDO0_S2 — N6 VCC_LDOG
17 GND — E13 VPP_OTP

NC N12 TP_DET

VPUMP E2 — PMU_VPUMP

C2920 47NF 20% 6.3V X5R-CERM 01005 ROOM=PMU

C2901 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C2900 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C2903 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C2909 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=PMU

C2907 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C2911 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C2913 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C2916 0.47UF 20% 6.3V X5R 01005 ROOM=PMU

VPUMP: 10nF min. @4.6V

U2700 D2542A0P0VQAVAC WLCSP SYM 1 OF 5

VLDO0 P6 — 17 PP2V5_LDO0_S2 — LDO0 250 mA MAX
VLDO1 M5 — 17 PP3V3_USB — LDO1 50 mA MAX
VLDO2 P5 — 10 PP1V8_AUDIO_VA_S2 — LDO2 50 mA MAX
VLDO3 M3 — 25 PP3V0_PENROSE — LDO3 50 mA MAX
VLDO4 T2 — 17 PP0V7_VDD_LOW_S2 — LDO4 250 mA MAX
VLDO5 U1 — 19 PP2V63_NAND — LDO5 1.15 A MAX
VLDO6 L2 — NC_DENALI_LDO6 — LDO6 110 mA MAX

Job Taken by Gecko

LDO 2,4,8 and 5 all have STability caps off page

VLDO7 L3 — 18 48 48 49 58 PP3V0_S2 — LDO7 250 mA MAX
VLDO8 R2 — 19 PP0V9_NAND — LDO8 800 mA MAX
VLDO9 L5 — 17 23 26 57 PP1V8_ALWAYS — LDO9 10 mA MAX

D3X Cap Off page

VLDO10 P7 — 44 PP3V0_DISPLAY — LDO10 250 mA MAX
VLDO11 N5 — 17 PP1V2_SOC — LDO11 250 mA MAX
VLDO12 P4 — NC_DENALI_LDO12 — LDO12 50 mA MAX
VLDO13 N3 — 40 41 42 PP1V2_CODEC_S2 — LDO13 250 mA MAX
VLDO14 P3 — 44 PP1V0_DISPLAY_DVDD — LDO14 250 mA MAX

D3X Cap Off page

44 29 20 17 PP1V26_S2

U2900 SCY99224-1.10V WLCSP ROOM=PMU CRITICAL

A1 IN — OUT A2 — PP1V1_RACER_S2 59
B1 EN
GND
B2

C2917 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

PAGE TITLE: SYSTEM POWER: PMU LDOs (3/4)

Apple Inc.

DRAWING NUMBER: 051-02545 SIZE: D
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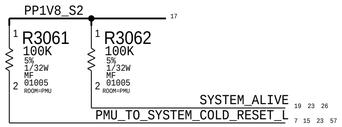
PMU - GPIOs

TODO: Update
CONTROL PIN NOTES:

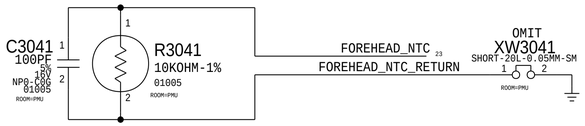
NOTE (1):INPUT PULL-DOWN 100-300k
NOTE (2):INPUT PULL-DOWN 1M
NOTE (3):INPUT PULL-UP OR DOWN 100k-300k
NOTE (4):OUTPUT OPEN-DRAIN, REQUIRES PULL-UP

COLD_RESET & SYSTEM_ALIVE

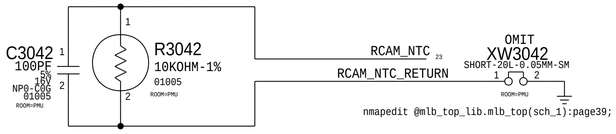


NTCs

FOREHEAD NTC



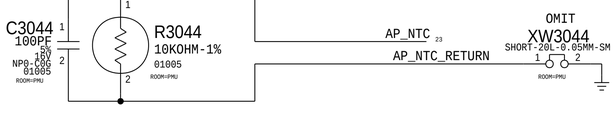
REAR CAMERA NTC



nmapedit @mlb_top_lib.mlb_top(sch_1):page39;

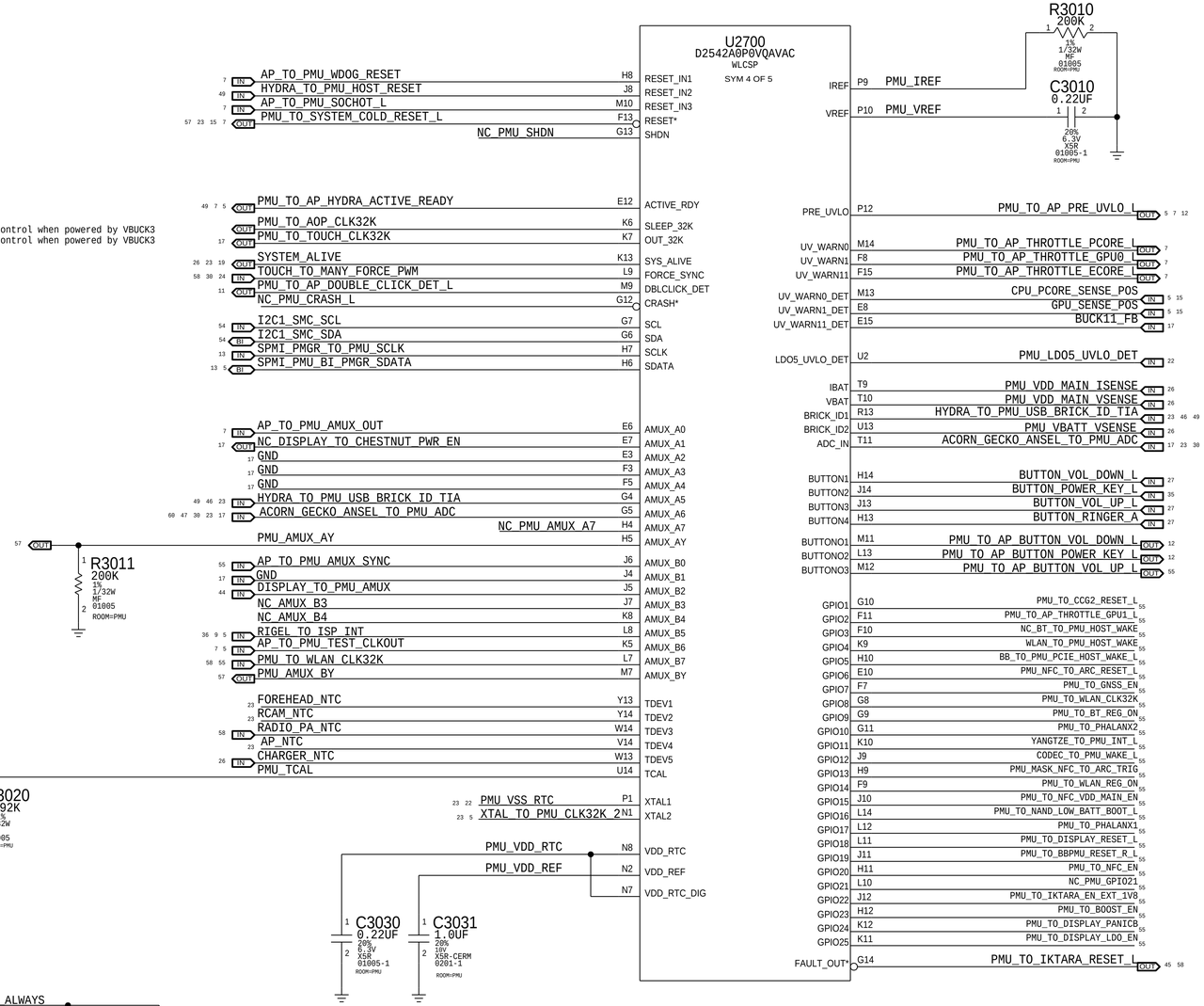
RADIO PA NTC on MLB Bottom

AP NTC



CHARGER NTC on Chrager Page

Only has DS control when powered by VBUCK3
Only has DS control when powered by VBUCK3



NOTE:100PF CAPS ARE THE SAMPLING CAPS FOR PMU ADC

PAGE TITLE
SYSTEM POWER: PMU (4/4)

Apple Inc.

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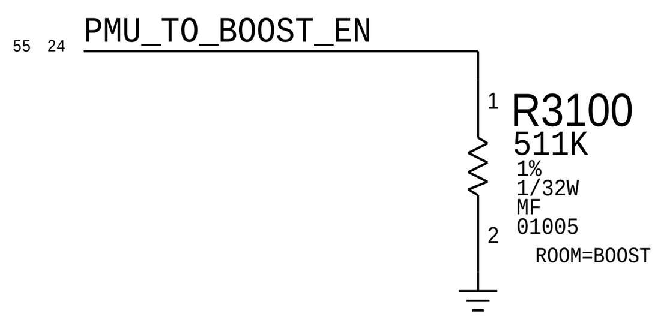
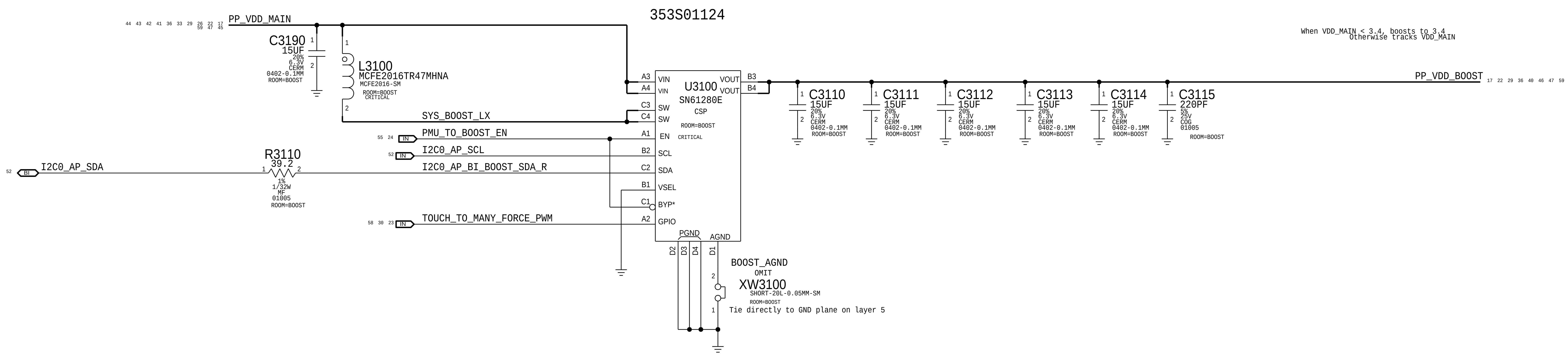
Boost Enable Pull



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00871	152S00869	ALT_PARTS	L3100	BOOST IND ALT, CYN
152S00873	152S00869	ALT_PARTS	L3100	BOOST IND ALT, TDK

BOOST

353S01124


PP_VDD_MAIN
C3190
15UF
20%
6.3V
CERM
0402-0.1MM
ROOM=BOOST
L3100
MCFE2016TR47MHNA
MCFE2016-SM
ROOM=BOOST
CRITICAL
SYS_BOOST_LX
PMU_TO_BOOST_EN
I2C0_AP_SCL
I2C0_AP_SDA
R3110
39.2
1%
1/32W
MF
01005
ROOM=BOOST
I2C0_AP_BI_BOOST_SDA_R
TOUCH_TO_MANY_FORCE_PWM
U3100
SN61280E
CSP
ROOM=BOOST
CRITICAL
VIN
VIN
SW
SW
EN
SCL
SDA
VSEL
BYP*
GPIO
VOUT
VOUT
PGND
AGND
BOOST_AGND
OMIT
XW3100
SHORT-20L-0.05MM-SM
ROOM=BOOST
Tie directly to GND plane on layer 5
C3110
C3111
C3112
C3113
C3114
15UF
20%
6.3V
CERM
0402-0.1MM
ROOM=BOOST
C3115
220PF
5%
25V
COG
01005
ROOM=BOOST
When VDD_MAIN < 3.4, boosts to 3.4
Otherwise tracks VDD_MAIN
PP_VDD_BOOST

PAGE TITLE
SYSTEM POWER: Boost

Apple Inc.

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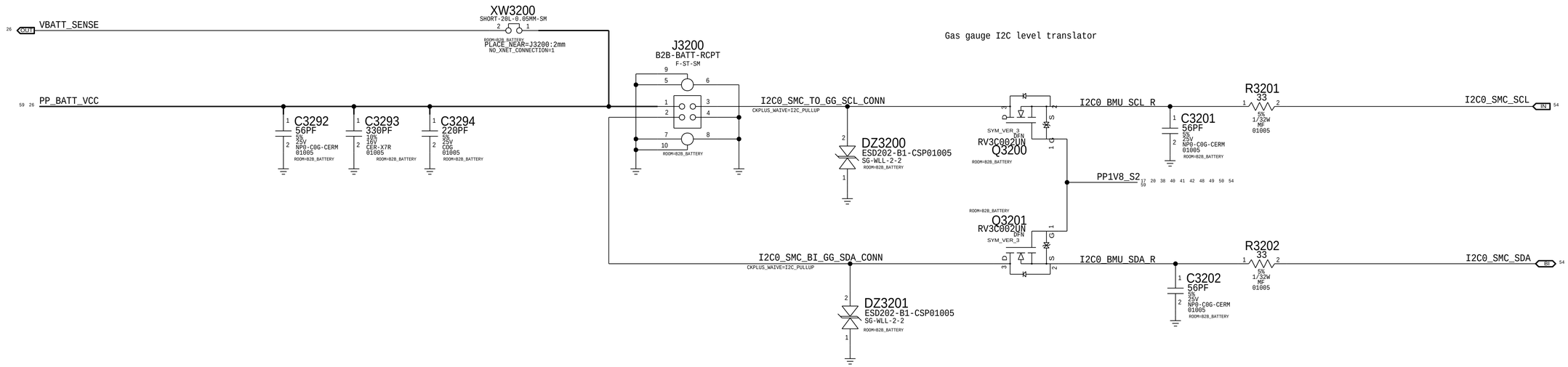
BATTERY CONNECTOR

Rcpt: 516S00232
Plug: 516S00233



PAGE TITLE
SYSTEM POWER: B2B Battery

Apple Inc.

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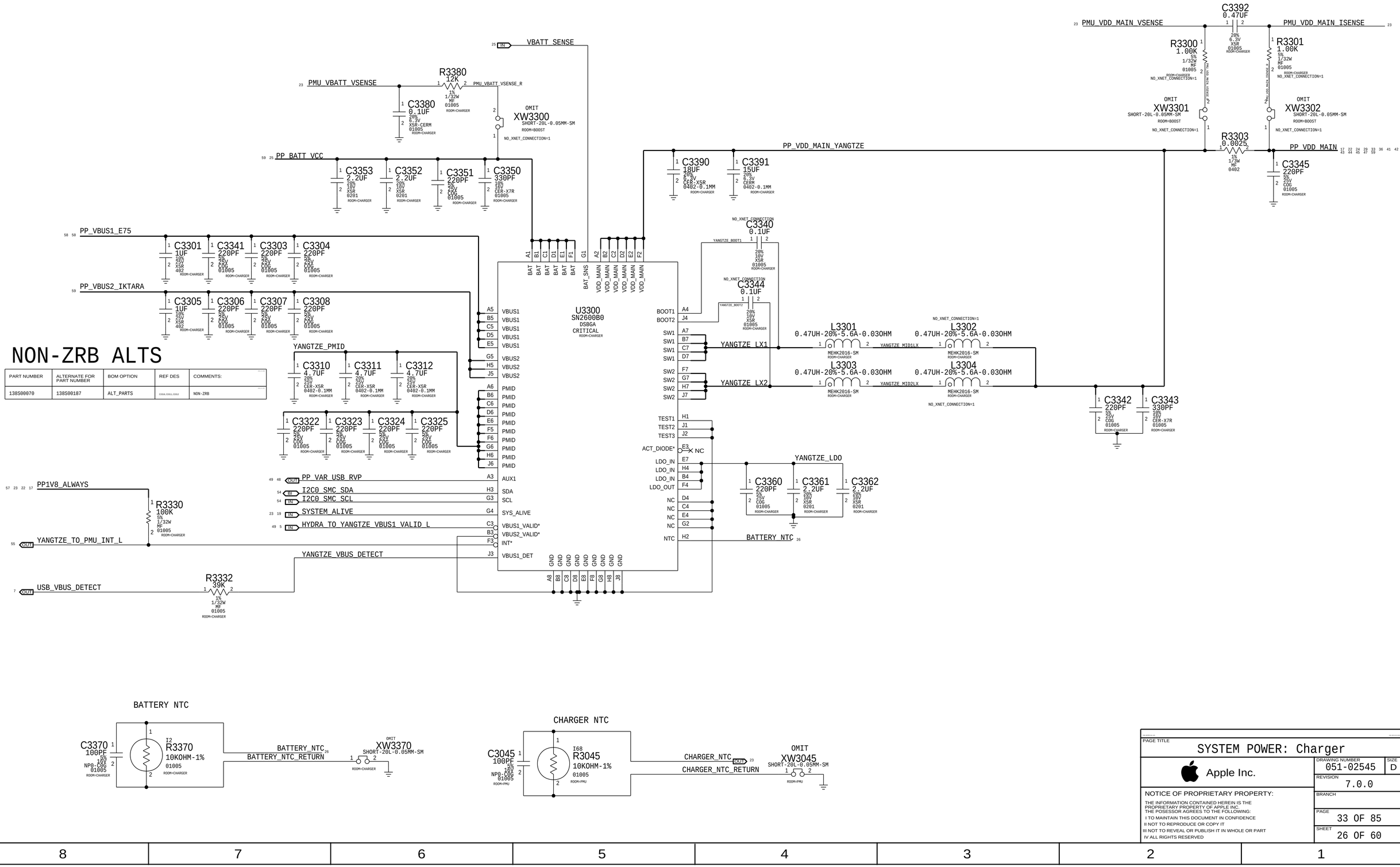
YANGTZE CHARGER

NON-ZRB ALTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00070	138S00187	ALT_PARTS	C3310,C3311,C3312	NON-ZRB



PAGE TITLE

SYSTEM POWER: Charger

Apple Inc.

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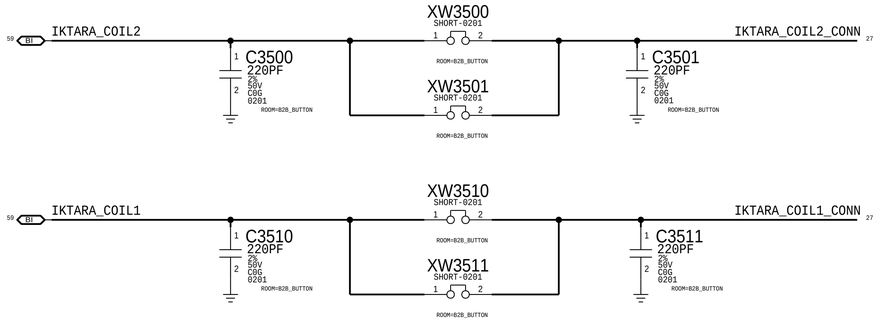
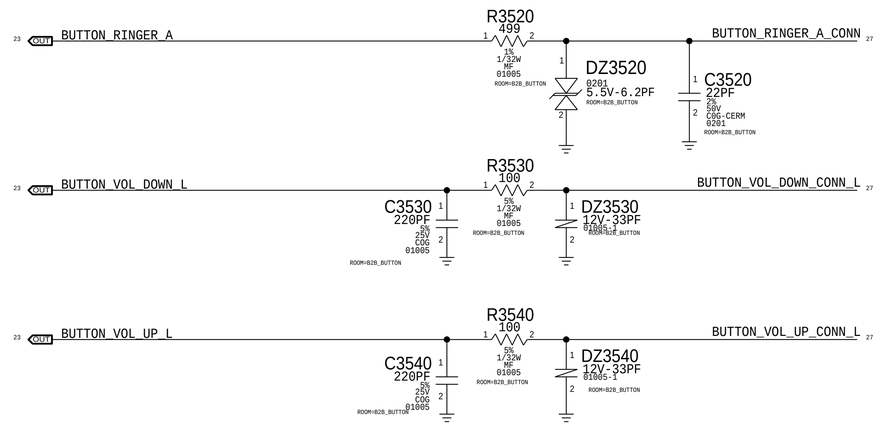
Cyclone Filtering

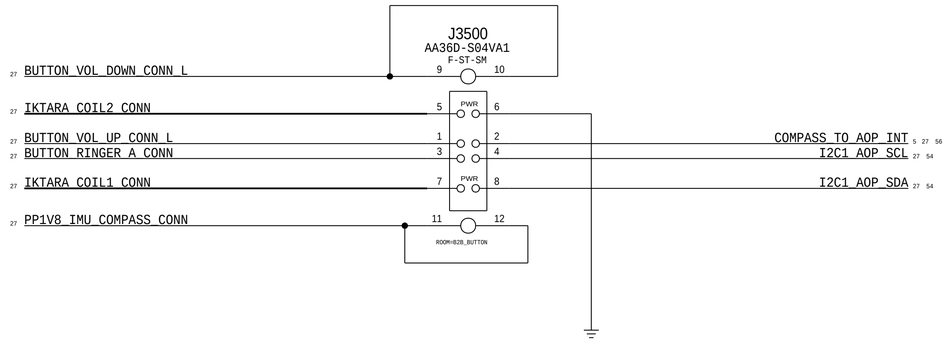


BUTTONS

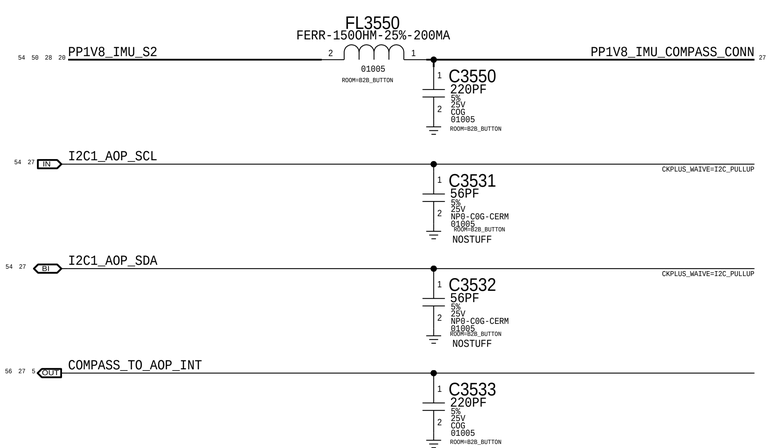


Cyclone + Button Connnector

Rcpt: 516S00289 <-- This one on MLB
Plug: 516S00290



Compass



PAGE TITLE

SYSTEM POWER: B2B Cyclone + Button

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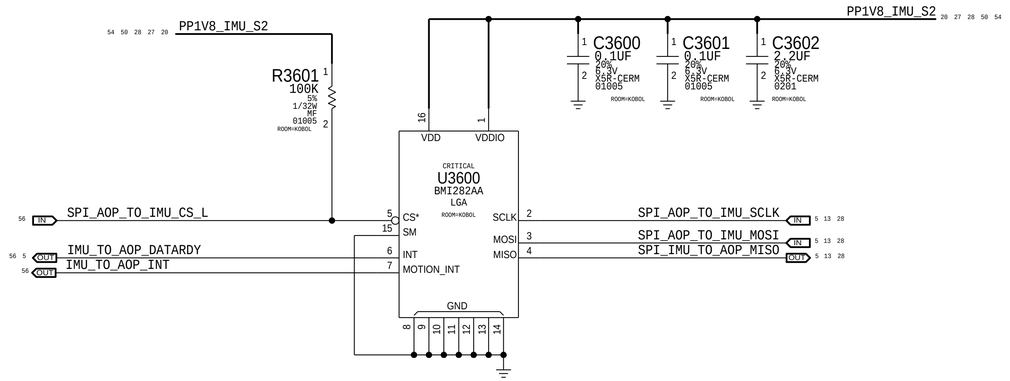
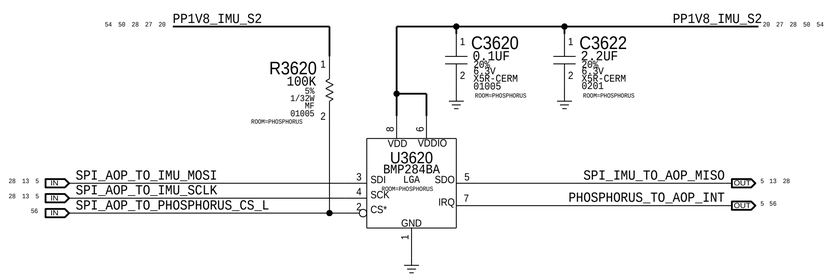
Kobol - Accel & Gyro

APN: 338S00367



Phosphorus

BOSCH (APN:338S00334)



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SENSORS

Apple Inc.

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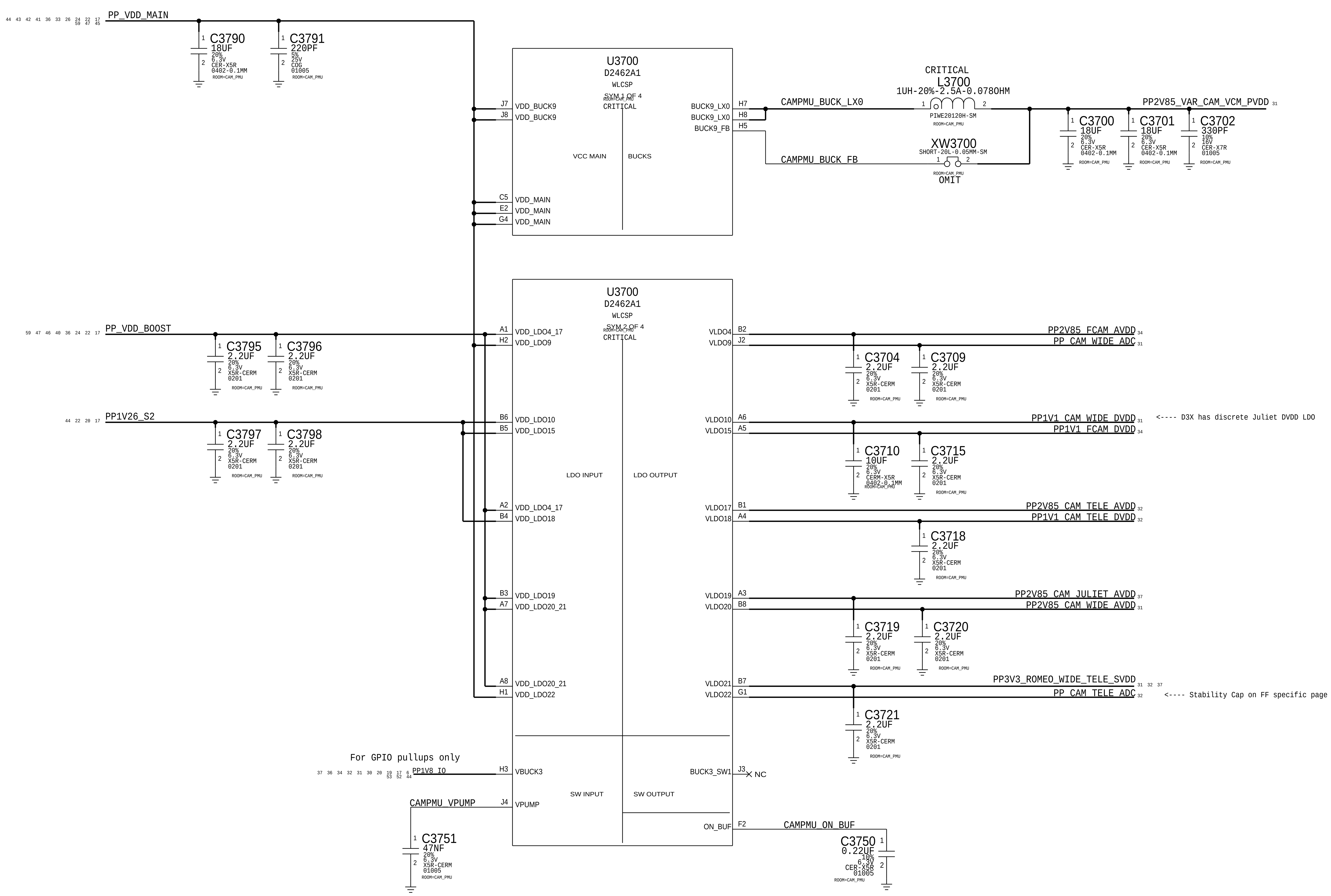
Camera PMU



PP_VDD_MAIN
C3790 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=CAM_PMU
C3791 220PF 5% 25V C0G 01005 ROOM=CAM_PMU
U3700 D2462A1 WLCSP SYM 1 OF 4 CRITICAL
VDD_BUCK9 J7
VDD_BUCK9 J8
VDD_MAIN C5
VDD_MAIN E2
VDD_MAIN G4
VCC MAIN
BUCKS
BUCK9_LX0 H7
BUCK9_LX0 H8
BUCK9_FB H5
CAMPMU_BUCK_LX0
CRITICAL
L3700 1UH-20%-2.5A-0.078OHM PIWE20120H-SM ROOM=CAM_PMU
CAMPMU_BUCK_FB
XW3700 SHORT-20L-0.05MM-SM ROOM=CAM_PMU OMIT
PP2V85_VAR_CAM_VCM_PVDD
C3700 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=CAM_PMU
C3701 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=CAM_PMU
C3702 330PF 10% 16V CER-X7R 01005 ROOM=CAM_PMU
U3700 D2462A1 WLCSP SYM 2 OF 4 CRITICAL
PP_VDD_BOOST
C3795 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
C3796 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
PP1V26_S2
C3797 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
C3798 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
A1 VDD_LDO4_17
H2 VDD_LDO9
B6 VDD_LDO10
B5 VDD_LDO15
A2 VDD_LDO4_17
B4 VDD_LDO18
B3 VDD_LDO19
A7 VDD_LDO20_21
A8 VDD_LDO20_21
H1 VDD_LDO22
LDO INPUT
LDO OUTPUT
VLDO4 B2 PP2V85_FCAM_AVDD
VLDO9 J2 PP_CAM_WIDE_ADC
C3704 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
C3709 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
VLDO10 A6 PP1V1_CAM_WIDE_DVDD
VLDO15 A5 PP1V1_FCAM_DVDD
<---- D3X has discrete Juliet DVDD LDO
C3710 10UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=CAM_PMU
C3715 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
VLDO17 B1 PP2V85_CAM_TELE_AVDD
VLDO18 A4 PP1V1_CAM_TELE_DVDD
C3718 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
VLDO19 A3 PP2V85_CAM_JULIET_AVDD
VLDO20 B8 PP2V85_CAM_WIDE_AVDD
C3719 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
C3720 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
VLDO21 B7 PP3V3_ROMEO_WIDE_TELE_SVDD
VLDO22 G1 PP_CAM_TELE_ADC
<---- Stability Cap on FF specific page
C3721 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU
For GPIO pullups only
PP1V8_IO
H3 VBUCK3
BUCK3_SW1 J3 NC
SW INPUT
SW OUTPUT
CAMPMU_VPUMP
J4 VPUMP
ON_BUF F2
CAMPMU_ON_BUF
C3751 47NF 20% 6.3V X5R-CERM 01005 ROOM=CAM_PMU
C3750 0.22UF 10% 6.3V CER-X5R 01005 ROOM=CAM_PMU

AVDD: Analog Supply (Pixels)
ADC: ADC Supply
DVDD: Digital Supply
SVDD: AF Sensor Supply
PVDD: AF Driver Supply

PAGE TITLE
CAMERA: PMU (1/2)

Apple Inc.

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Pull Downs

AP_TO_CAMPMU_RESET_L 30 55 57

R3801 100K 5% 1/32W MF 01005 ROOM=CAM_PMU

R3802 33.2 1% 1/32W MF 01005 ROOM=CAM_PMU

R3803 49.9 1% 1/32W MF 01005 ROOM=CAM_PMU

I2C3_ISP_SCL 53 IN

I2C3_ISP_SDA 53 BI

I2C3_ISP_SCL

I2C3_ISP_SDA_U3700

CAMPMU_TO_AP_IRQ_L 55 OUT

CAMPMU_TO_AP_IRQ_R_L

AP_TO_CAMPMU_RESET_L 30 55 57 IN

CAMPMU_VREF

CAMPMU_IREF

CAMPMU_VRTC

C3800 0.22UF 10% 6.3V CER-X5R 01005 ROOM=CAM_PMU

R3800 200K 1% 1/32W MF 01005 ROOM=CAM_PMU

C3810 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CAM_PMU

U3700 D2462A1 WLCSP SYM 3 OF 4 ROOM=CAM_PMU CRITICAL

I2C

SCL E8

SDA F8

IRQ* D8

CRASH* D6 NC

RESET_IN F5

RESET

VREF C1

IREF D1

VRTC E1

REFERENCE

TDEV1 J5 NC

TDEV2 G5 NC

TCAL C6 NC

TEMPERATURE

GPIO

GPIO1 F6 CAMPMU_TO_STROBE_DRIVER_HWEN OUT 33

GPIO2 E6 NC

GPIO3 D7 CAMPMU_TO_JULIET_DVDD_LDO_EN OUT 5 17

GPIO4 E4 NC

GPIO5 D4 NC

Alt Funcs GPIO6 D3 CAMPMU_TO_RIGEL_ENABLE OUT 5 36

LPM_IN GPIO9 F7 PP1V8_IO MAKE_BASE=TRUE PP1V8_IO 6 17 19 20 29 31 32 34 36 37 44 52 53

FORCE_SYNC GPIO10 F3 TOUCH_TO_MANY_FORCE_PWM

BUCK9_VSEL GPIO11 G3 YOGI_TO_RIGEL_STATUS_R IN 23 24 58

PRE-UVLO GPIO12 G2 NC

GPIO15 E3 MAMA_BEAR_BI_RIGEL_STATUS_R

R3811 10K 5% 1/32W MF 01005 ROOM=CAM_PMU

YOGI_TO_RIGEL_STATUS IN 36 38

R3810 10K 5% 1/32W MF 01005 ROOM=CAM_PMU

MAMA_BEAR_BI_RIGEL_STATUS BI 36 37

AMUX_AY C8 ACORN_GECKO_ANSEL_TO_PMU_ADC OUT 17 23 47 60

ATM E7

Advanced Test Mode (OTP rewrite)

U3700 D2462A1 WLCSP SYM 4 OF 4 ROOM=CAM_PMU CRITICAL

VSS C2 VSS C3 VSS C4 VSS C7 VSS D2 VSS D5 VSS E5 VSS F1

VSS G6 VSS G7 VSS G8 VSS H4 VSS H6 VSS J1 VSS J6 VSS F4

PAGE TITLE

CAMERA: PMU (2/2)

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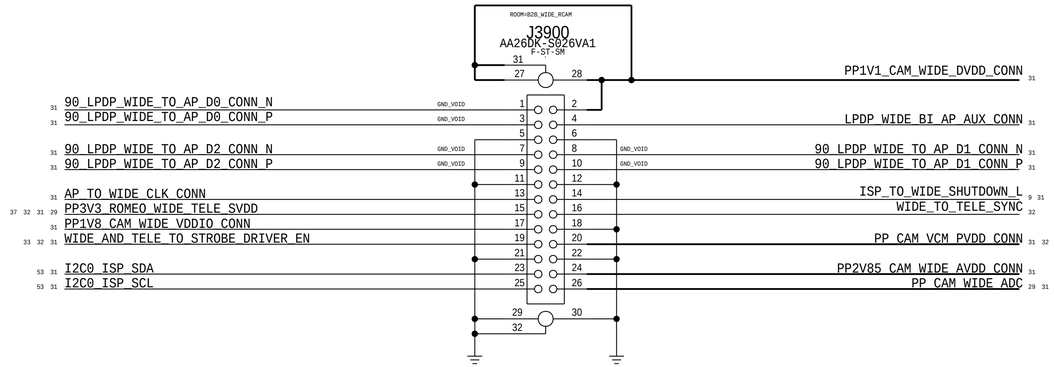
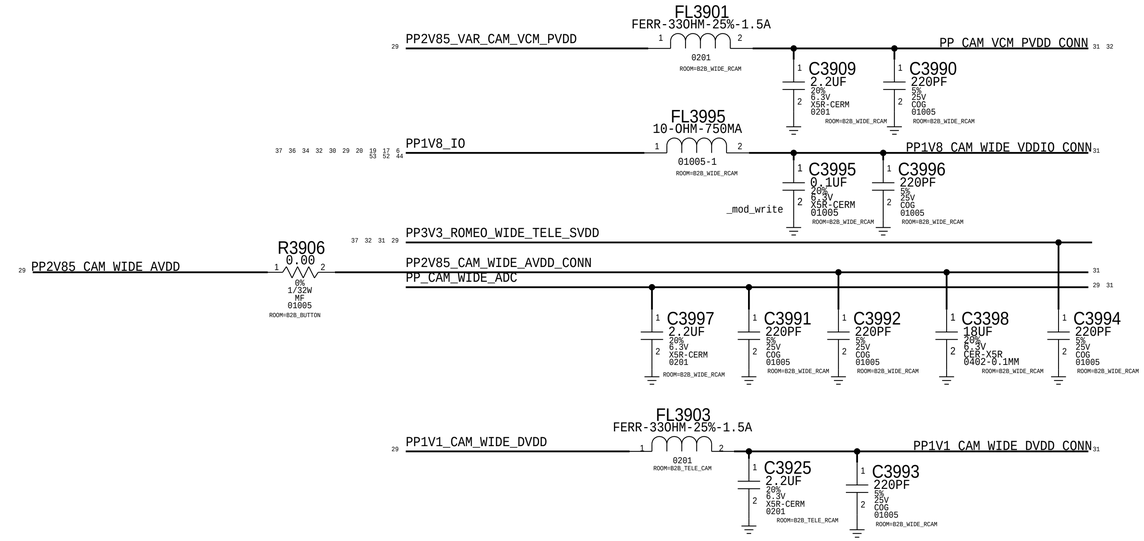
Wide Camera Connector

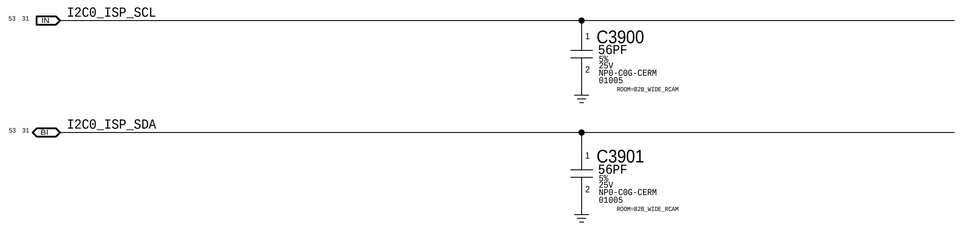
Rcpt: 516S00313 <-- This one on MLB
Plug: 516S00314



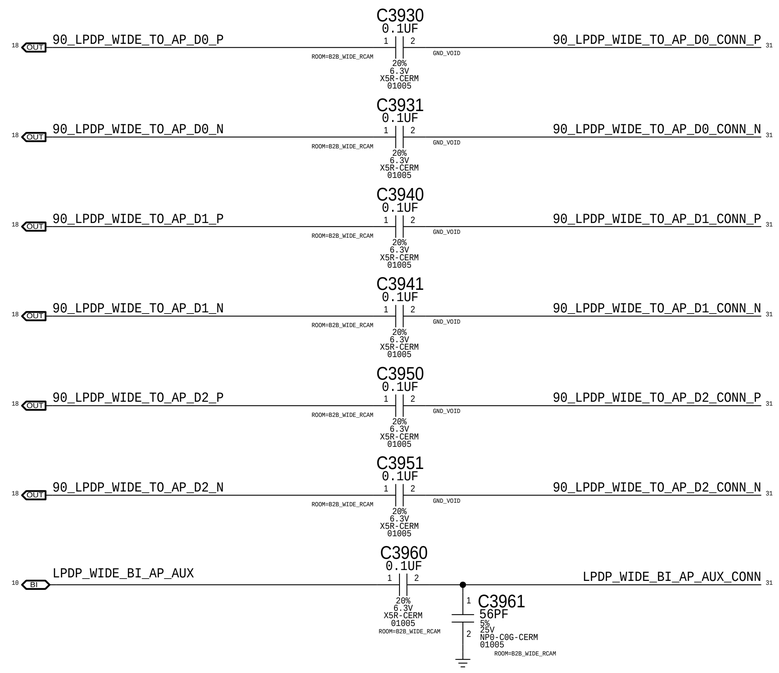
Power Filtering



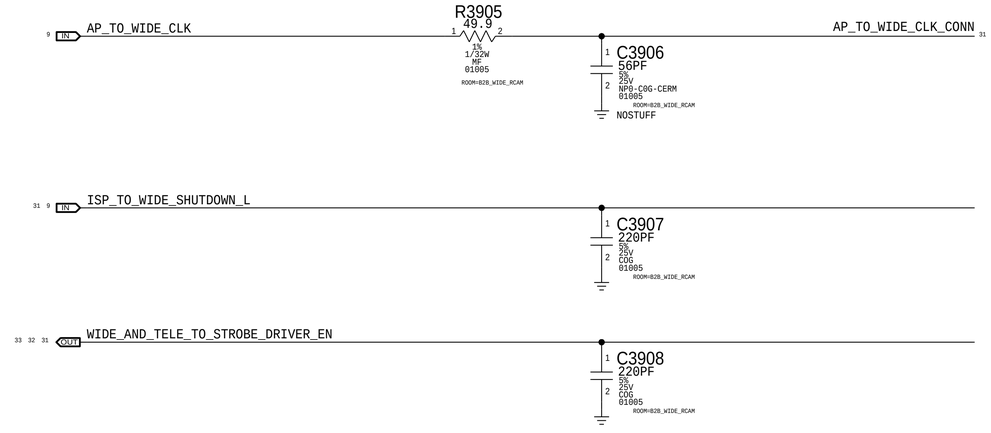
ISP I2C



LPDP Filters



IO Filters



PAGE TITLE

CAMERA: B2B Wide (TX)

Apple Inc.

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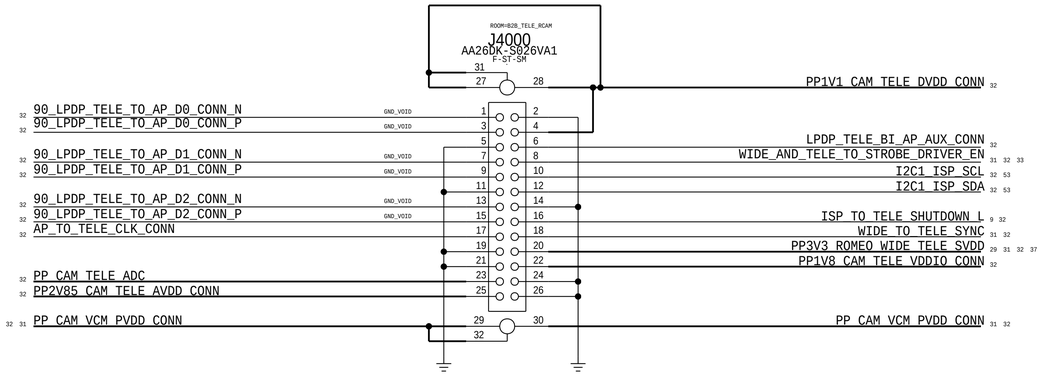
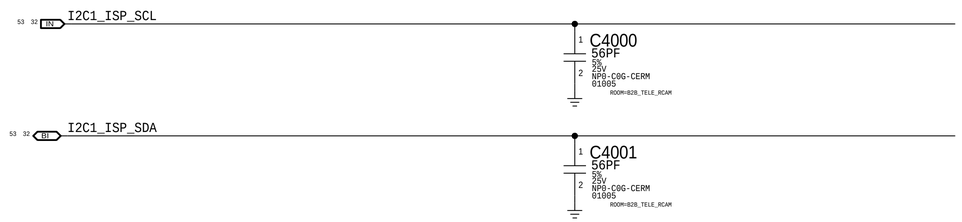
Tele Camera Connector

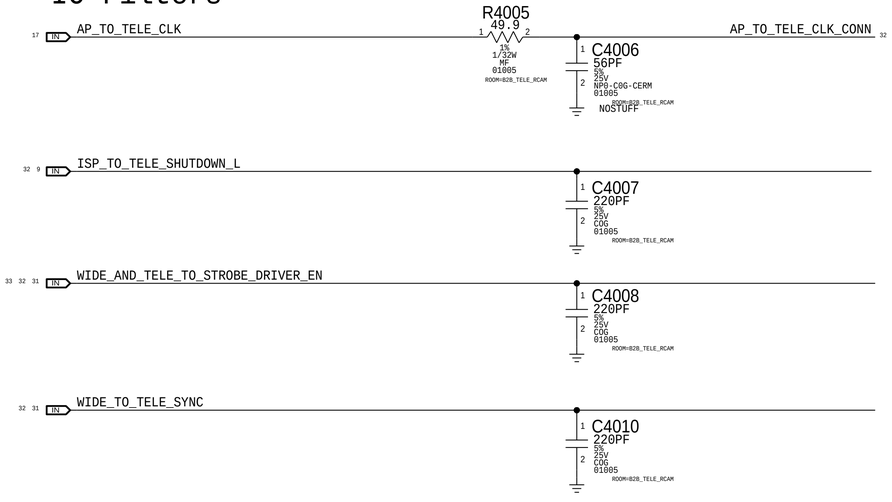
Rcpt: 516S00313 <-- This one on MLB
Plug: 516S00314



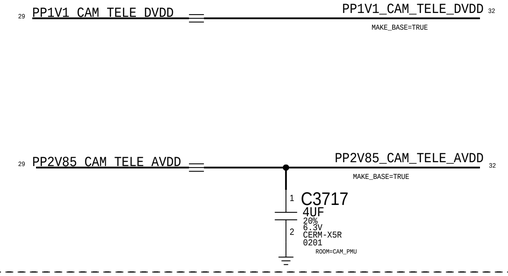
ISP I2C



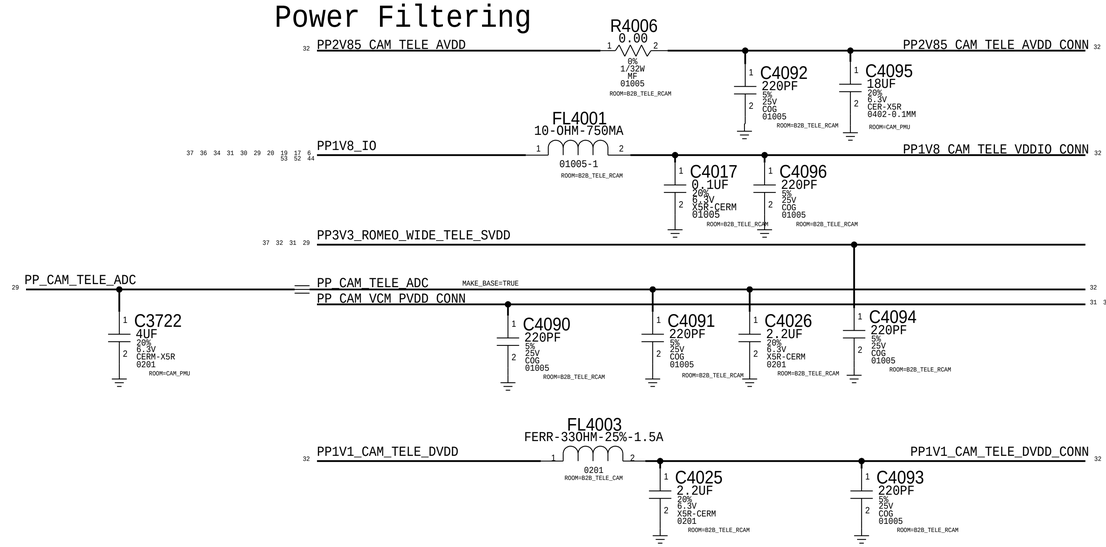
IO Filters



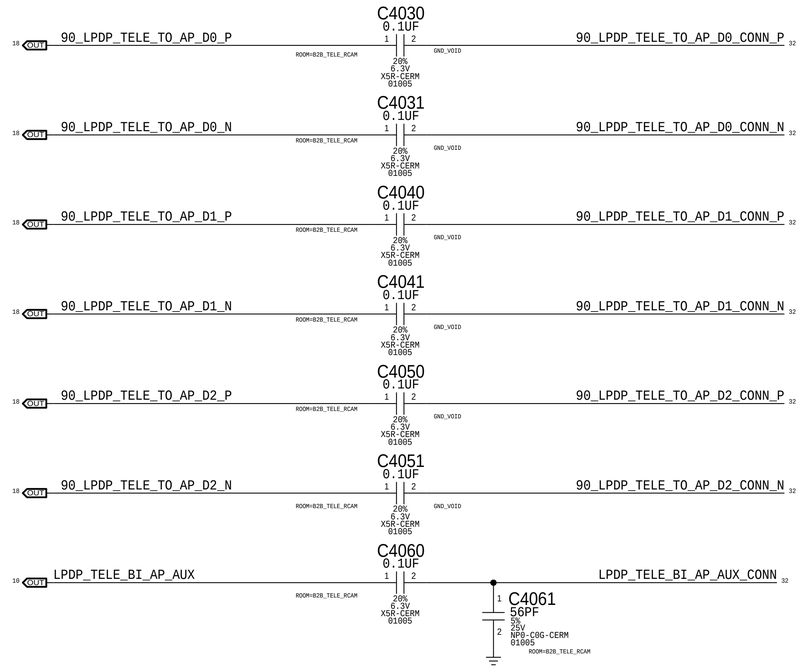
Lives Here For synccing purposes



Power Filtering



LPDP



PAGE TITLE
CAMERA: B2B Tele [MT]

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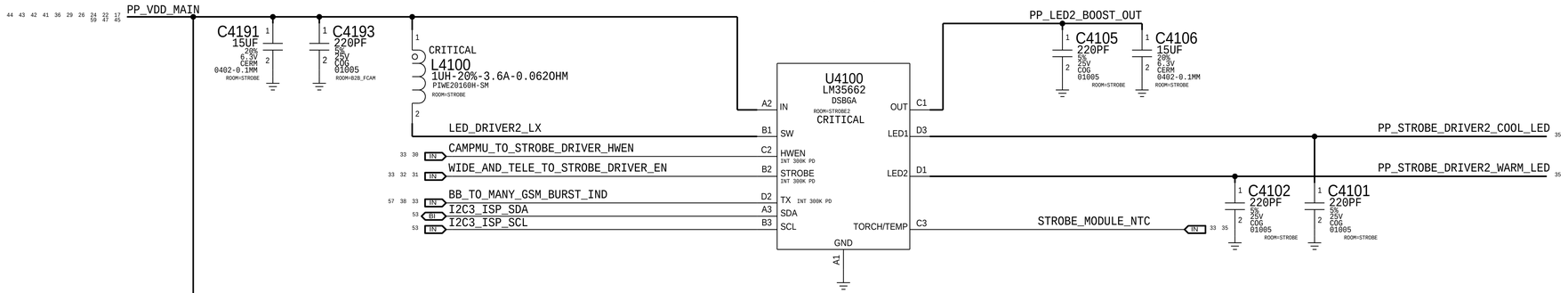
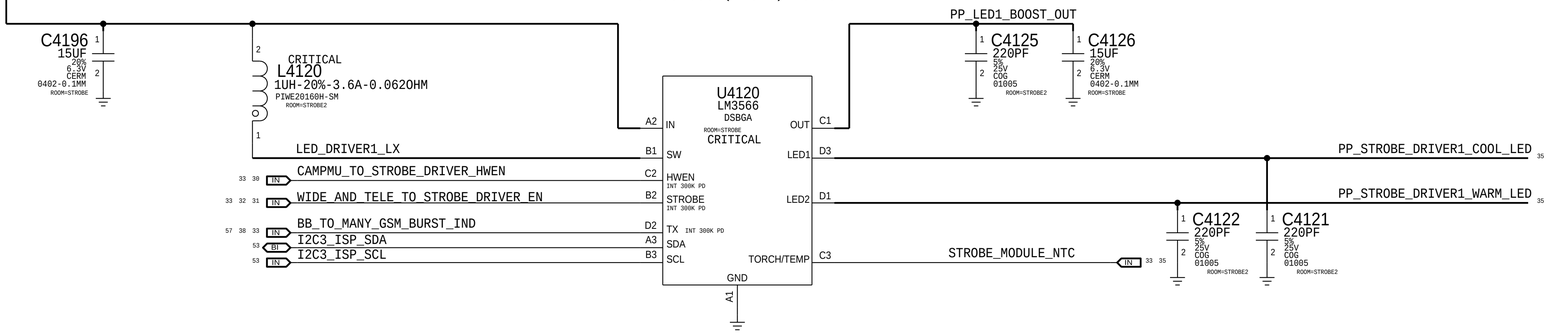
LED STROBE DRIVERS (NEON)

APN:353S00868
I2C Address (7-bit): 0x67



APN:353S00558
I2C Address (7-bit): 0x63



PAGE TITLE
CAMERA: Strobe Drivers

Apple Inc.

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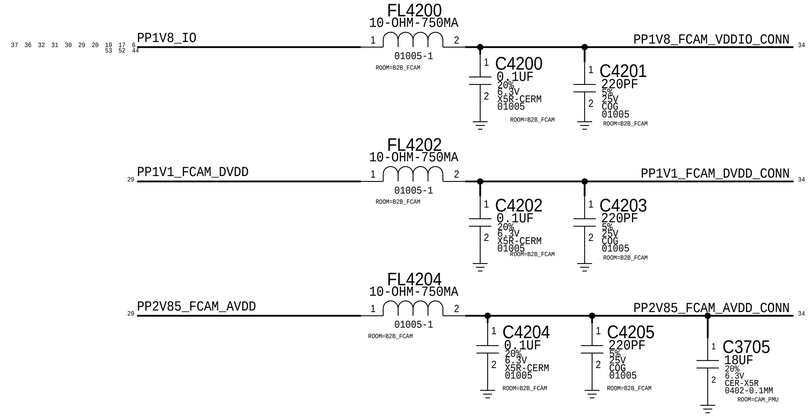
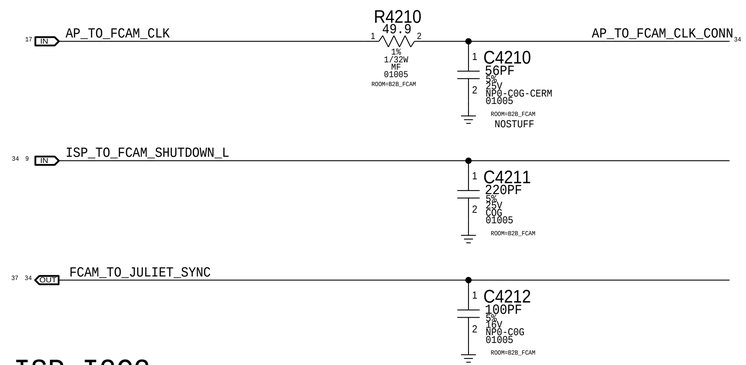
LONG ISLAND POWER

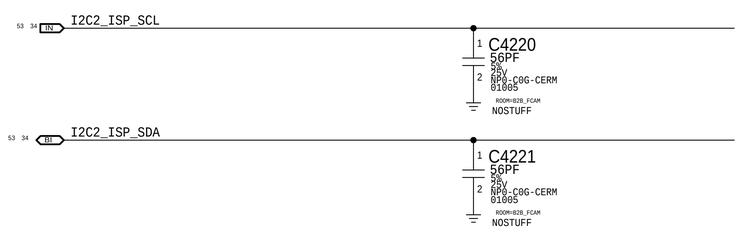


FCAM I/O



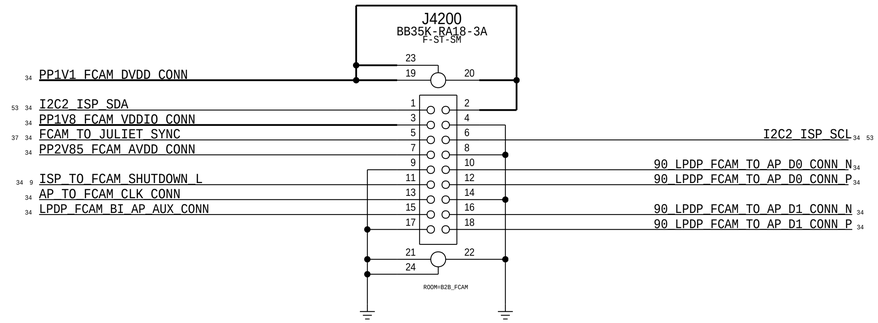
ISP I2C2

NOTE: SAME I2C as FCAM

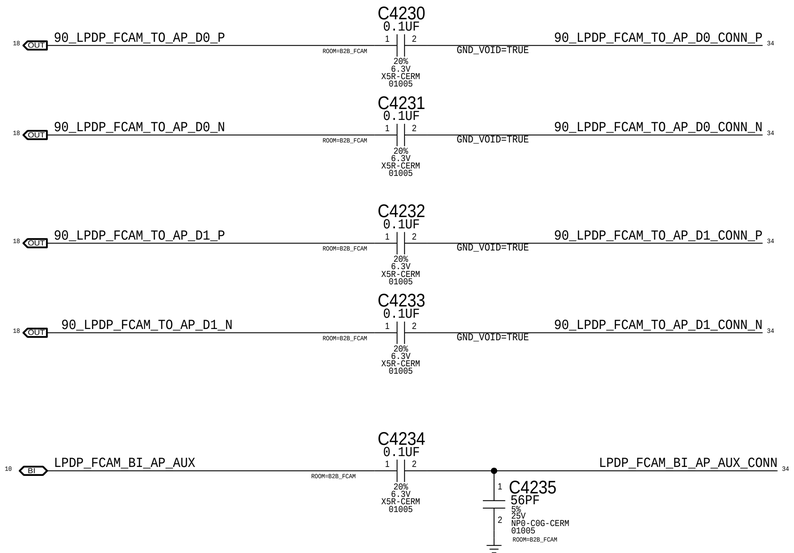


FCAM Connector

Rcpt: 516S00244 <-- This one on MLB
Plug: 516S00245



LPDP FILTERS



PAGE TITLE

CAMERA: B2B Fcam

Apple Inc.

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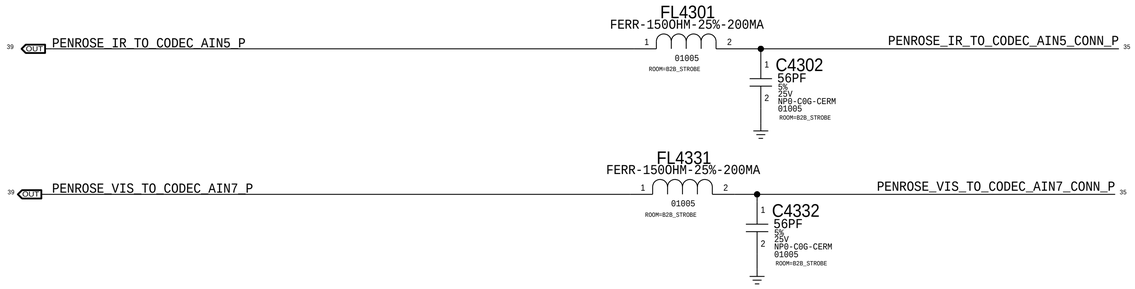
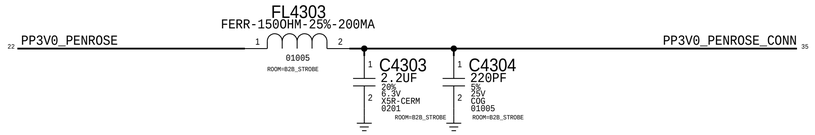
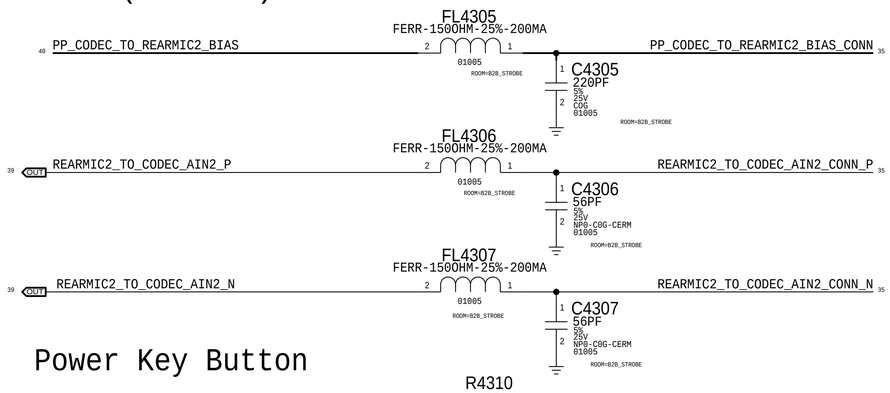
PENROSE

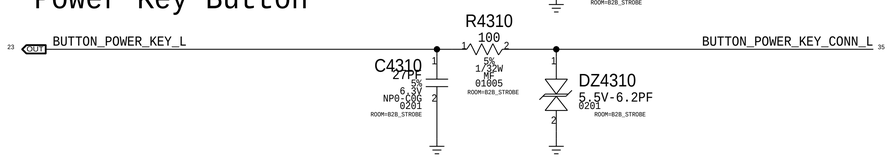




MIC2 (ANC REF)

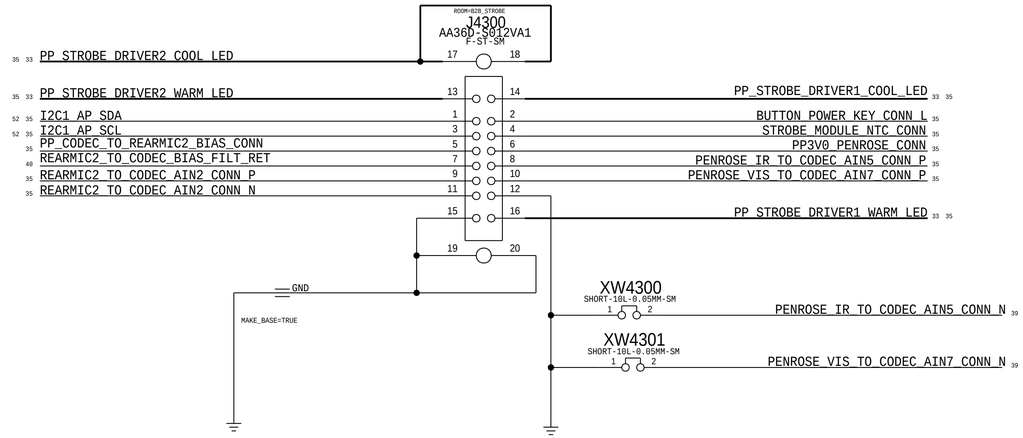


Power Key Button

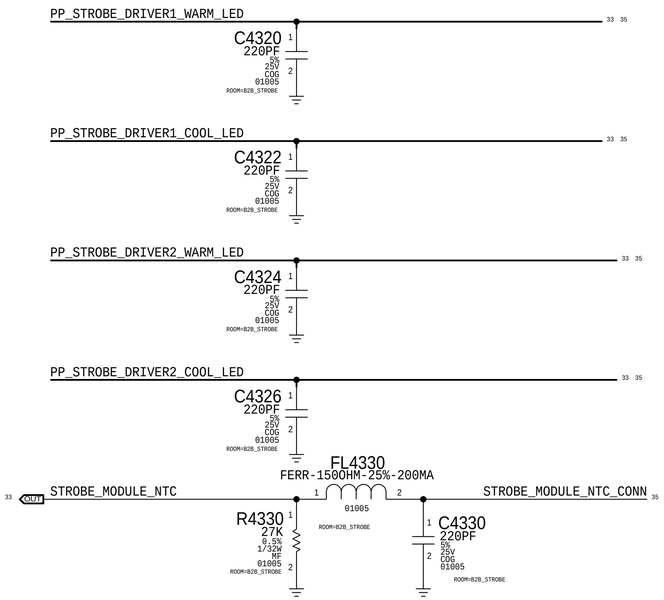


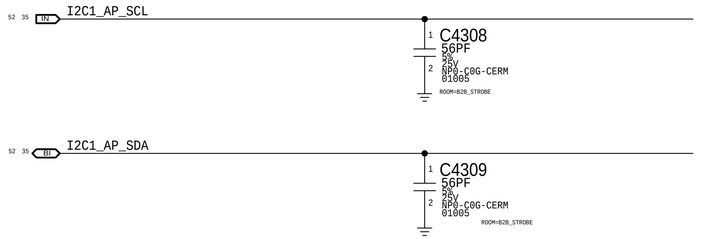
Strobe Connector

Rcpt: 516S00381 <-- This one on MLB
Plug: 516S00382



Strobe Filtering





PAGE TITLE
CAMERA: B2B Strobe + Hold Button

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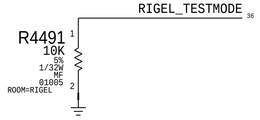
Rigel Driver

Test Mode Debugging



Rigel ALTs

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00720	152S00640	ALT_PARTS	L4400,L4401	RIGEL Inductors

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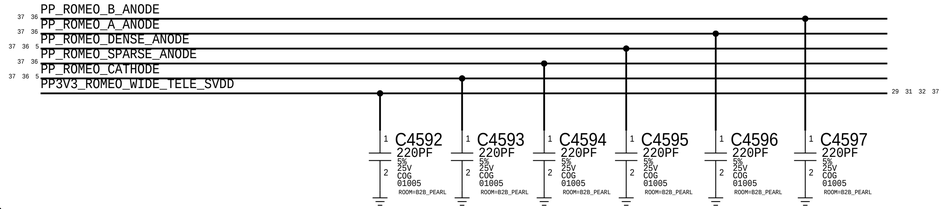
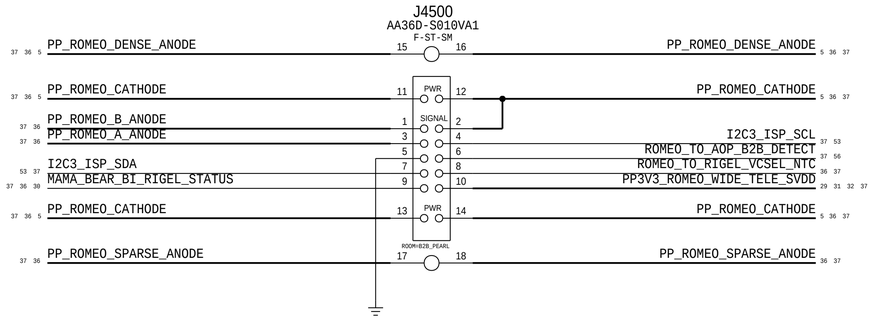
Romeo Power Filtering

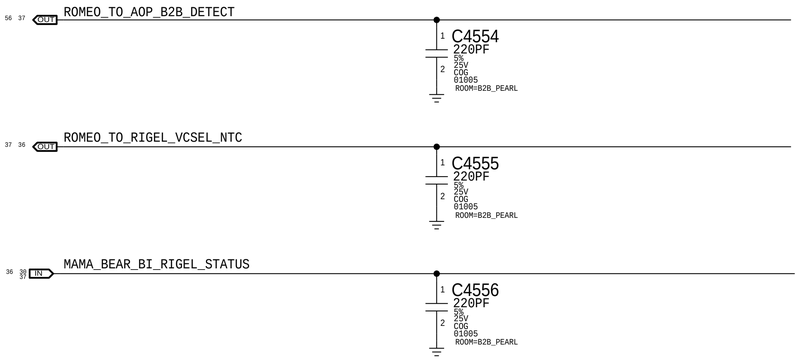


Romeo Connector

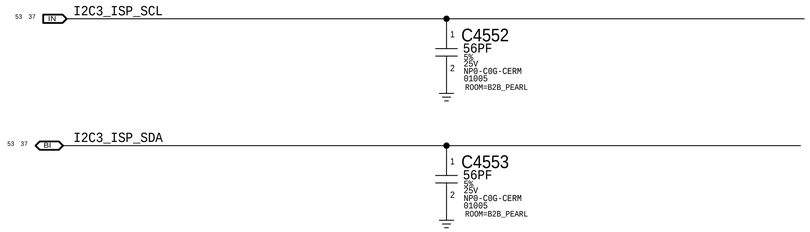
Rcpt: 516S00267 <-- This one on MLB
Plug: 516S00268



Romeo I/O

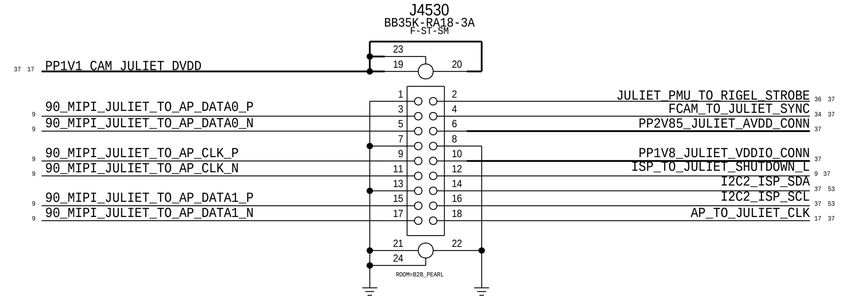


ISP I2C3

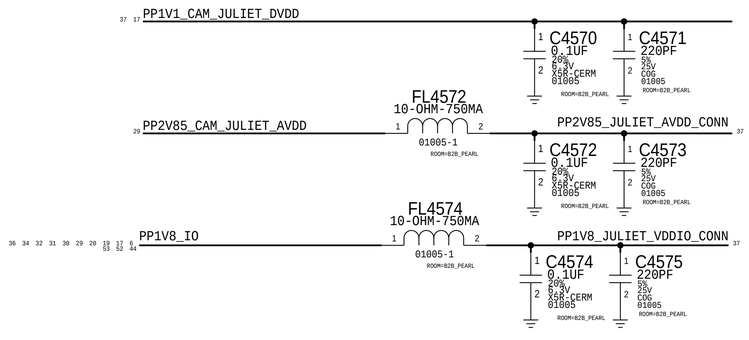


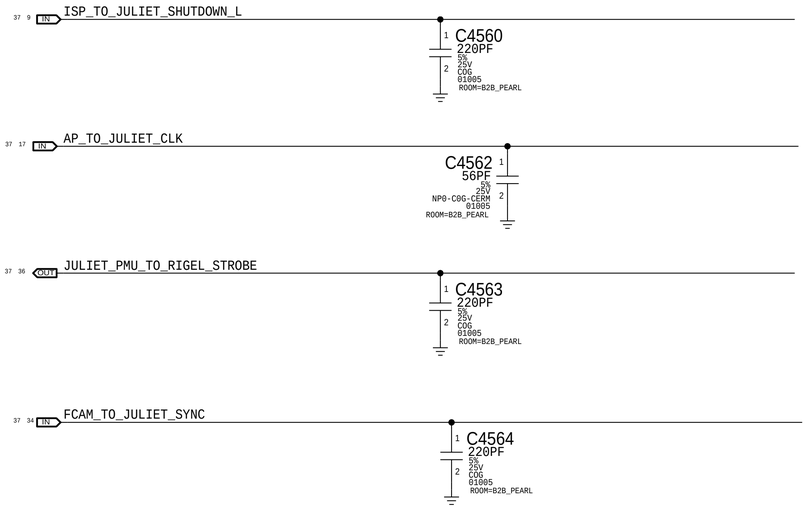
Juliet Connector

Rcpt: 516S00244 <-- This one on MLB
Plug: 516S00245

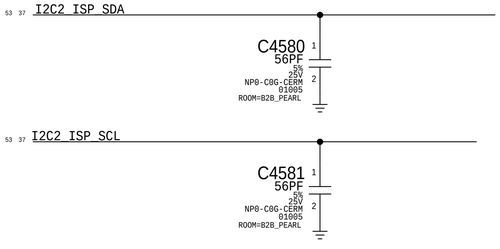


Juliet Power and I/O





NOTE: SAME I2C as FCAM



PAGE TITLE
PEARL: B2B Romeo + Juliet

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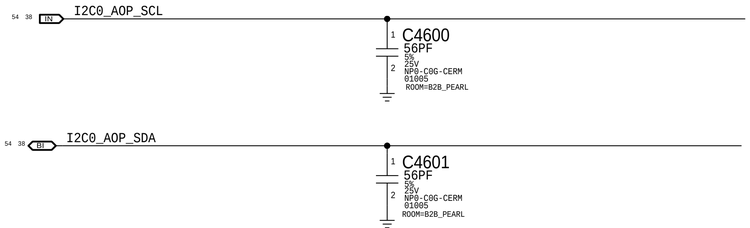
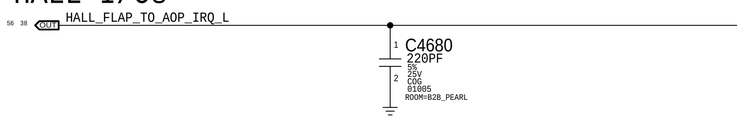
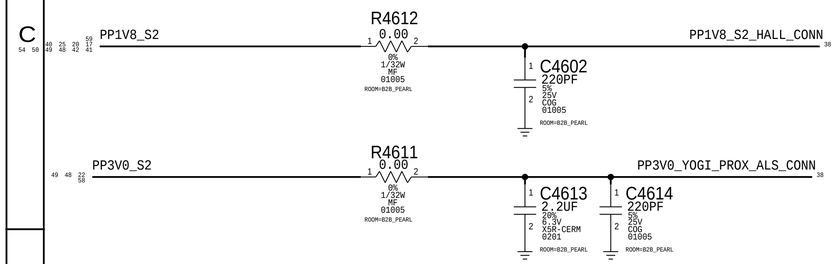
AOP I2C



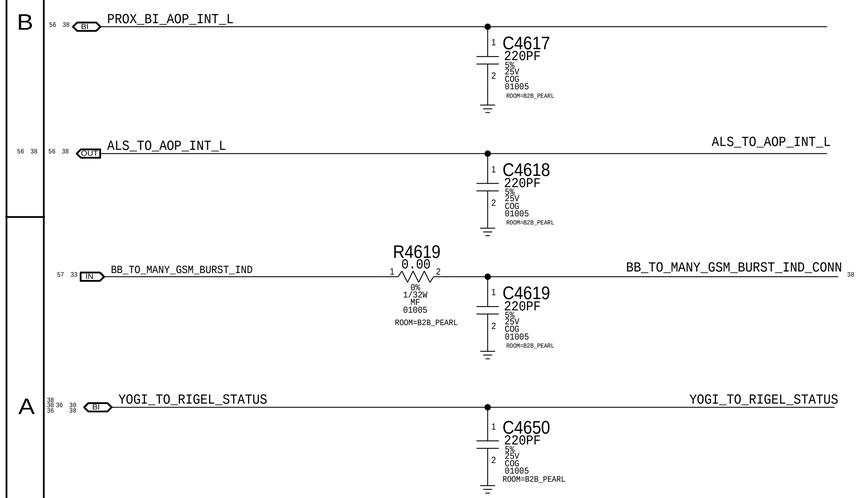
HALL I/Os



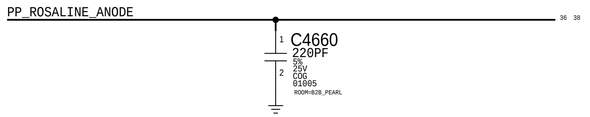
PROX & HALL POWER



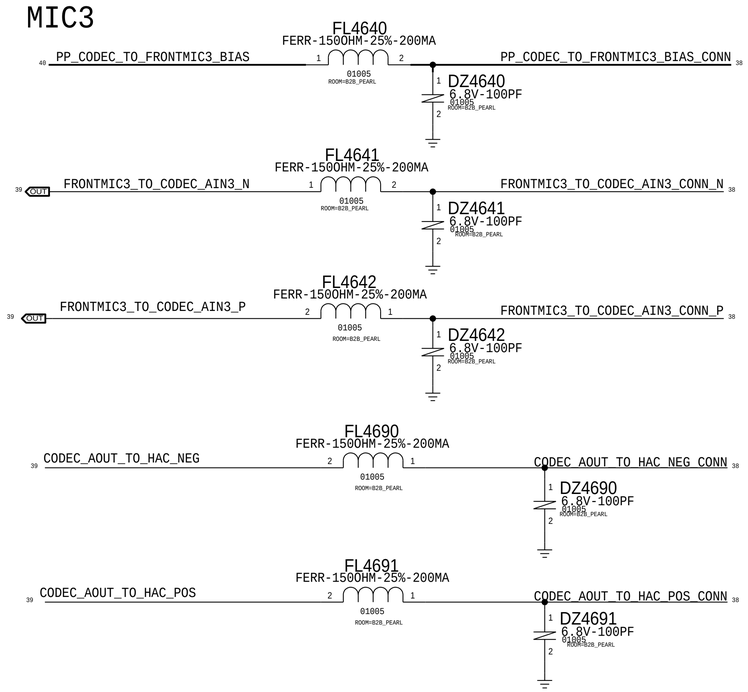
PROX/ALS/YOGI I/O



Yogi Signals

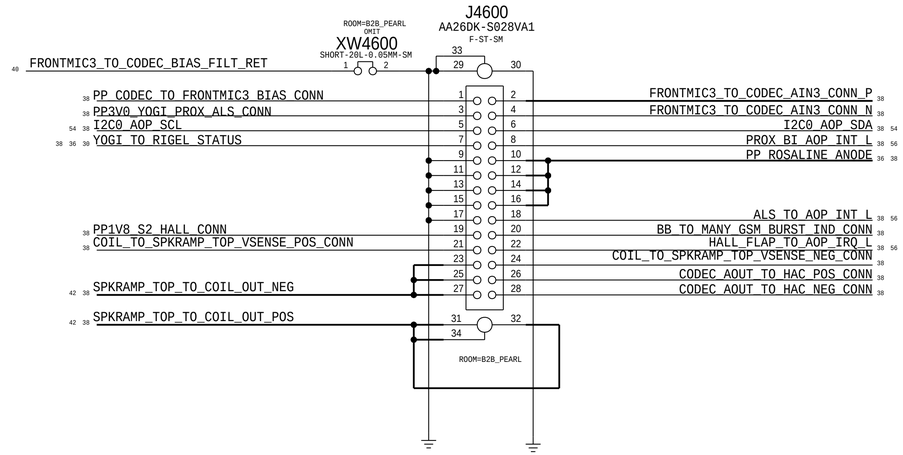


MIC3

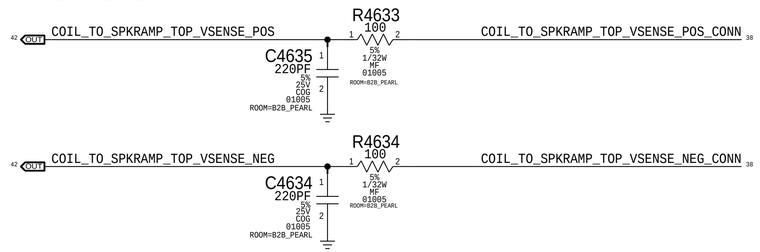


Rosaline + Sensor Connector

Rcpt: 516S00325 <-- This one on MLB
Plug: 516S00326



SPEAKER2



PAGE TITLE
PEARL: B2B Rosaline + Sensor

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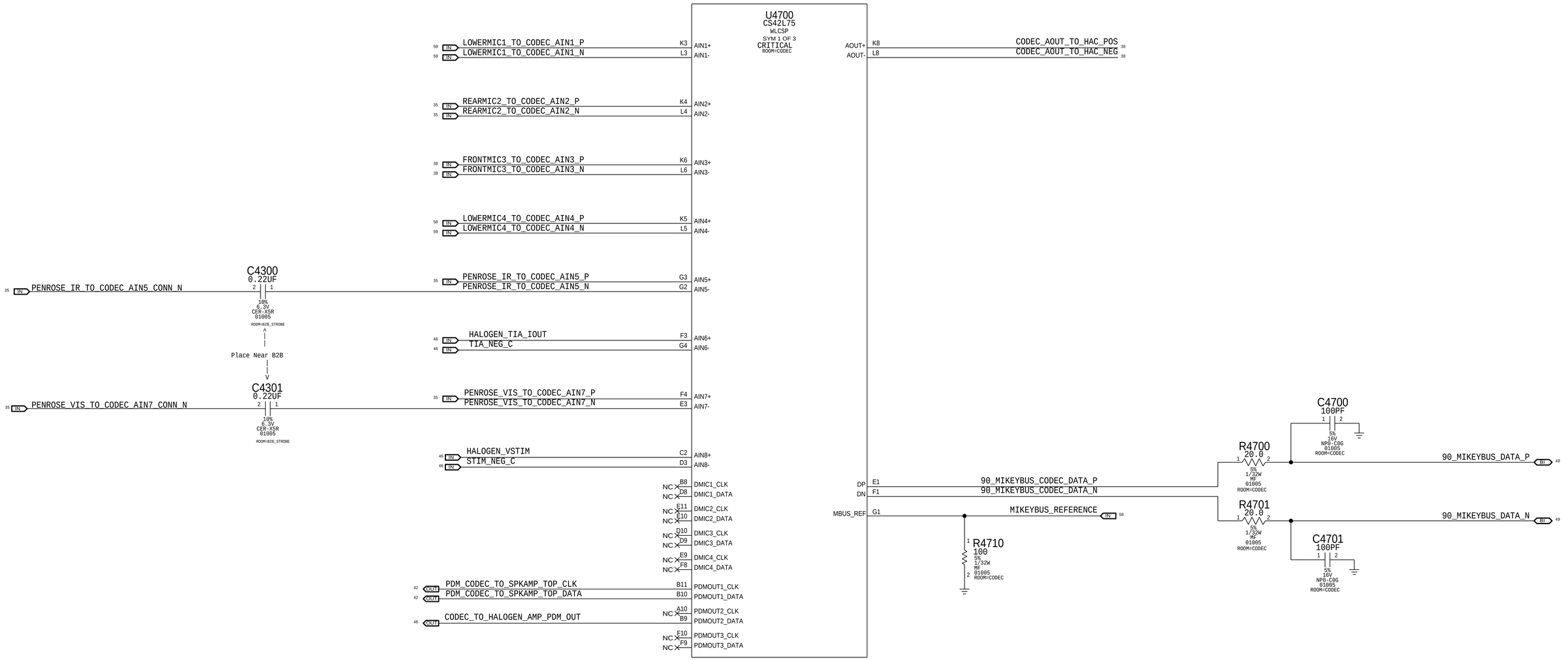
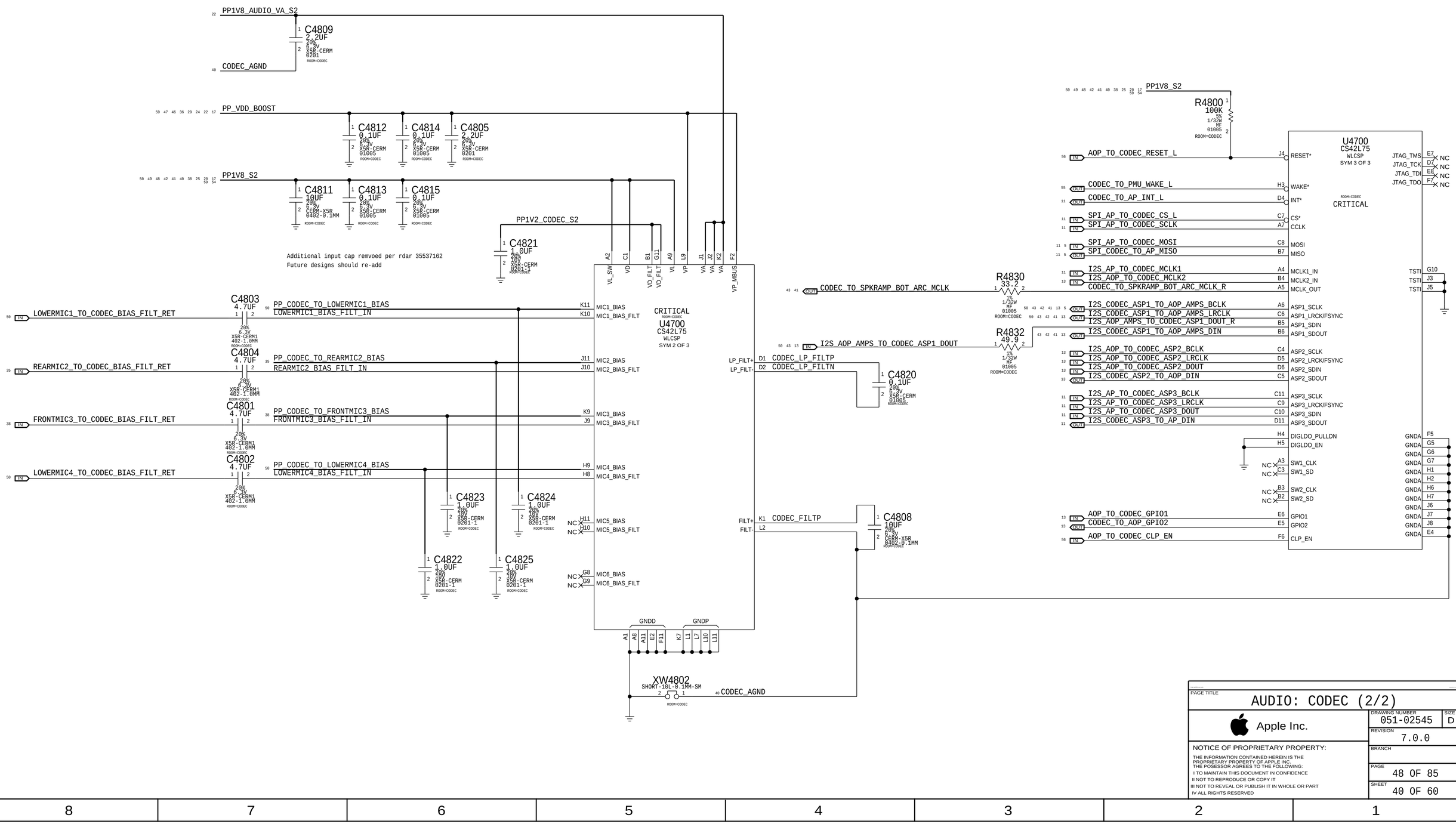
CALLAN AUDIO CODEC (ANALOG INPUTS & OUTPUTS)



CALLAN AUDIO CODEC (POWER & I/O)



PAGE TITLE

AUDIO: CODEC (2/2)

Apple Inc.

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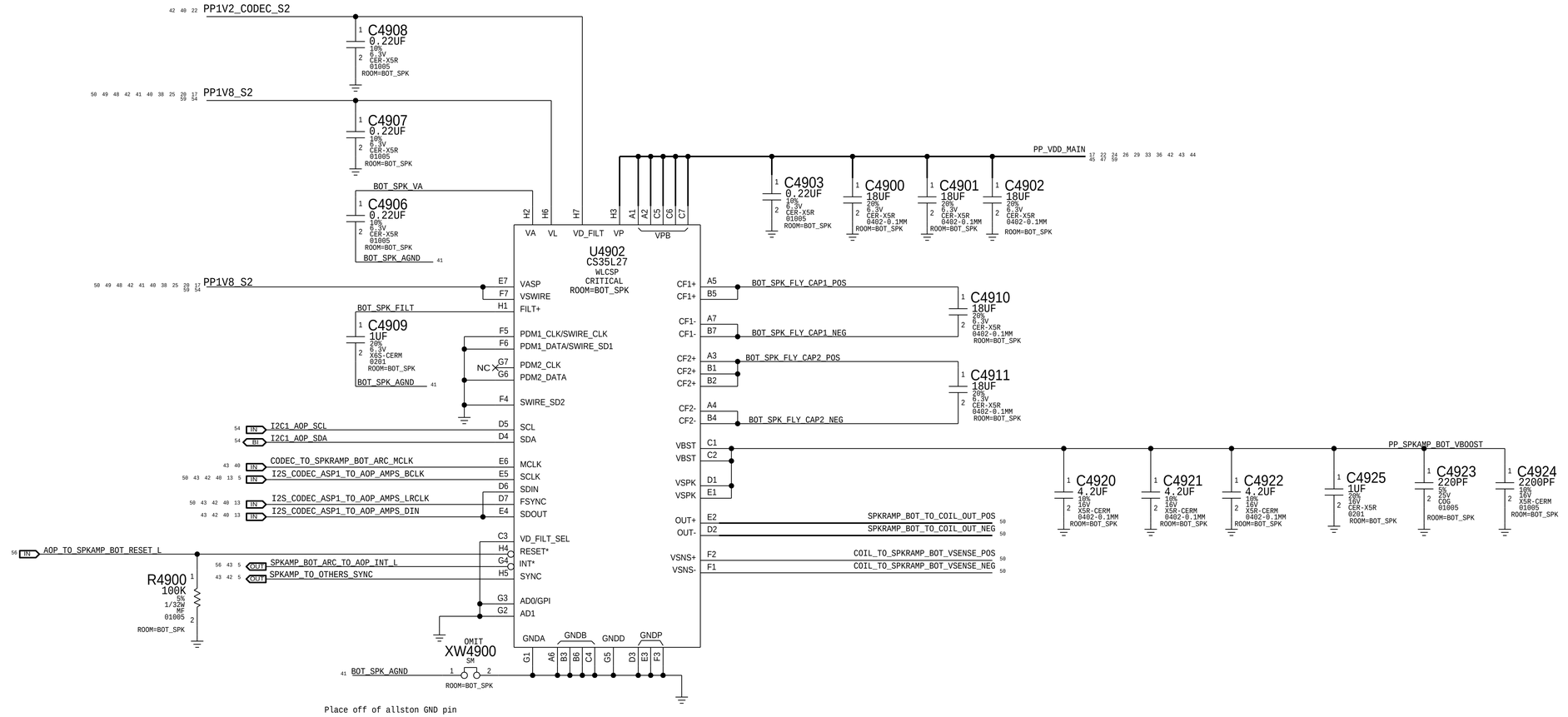
AMP	AD0	AD1	I2C_ADR	
TOP	0	0	TBD1	AP I2C2
BOT	0	0	TBD1	AOP I2C1
ARC	0	1	TBD2	



Place off of allston GND pin

SYNC_DATE=04/05/2017

PAGE TITLE

AUDIO: SOUTH SPKAMP

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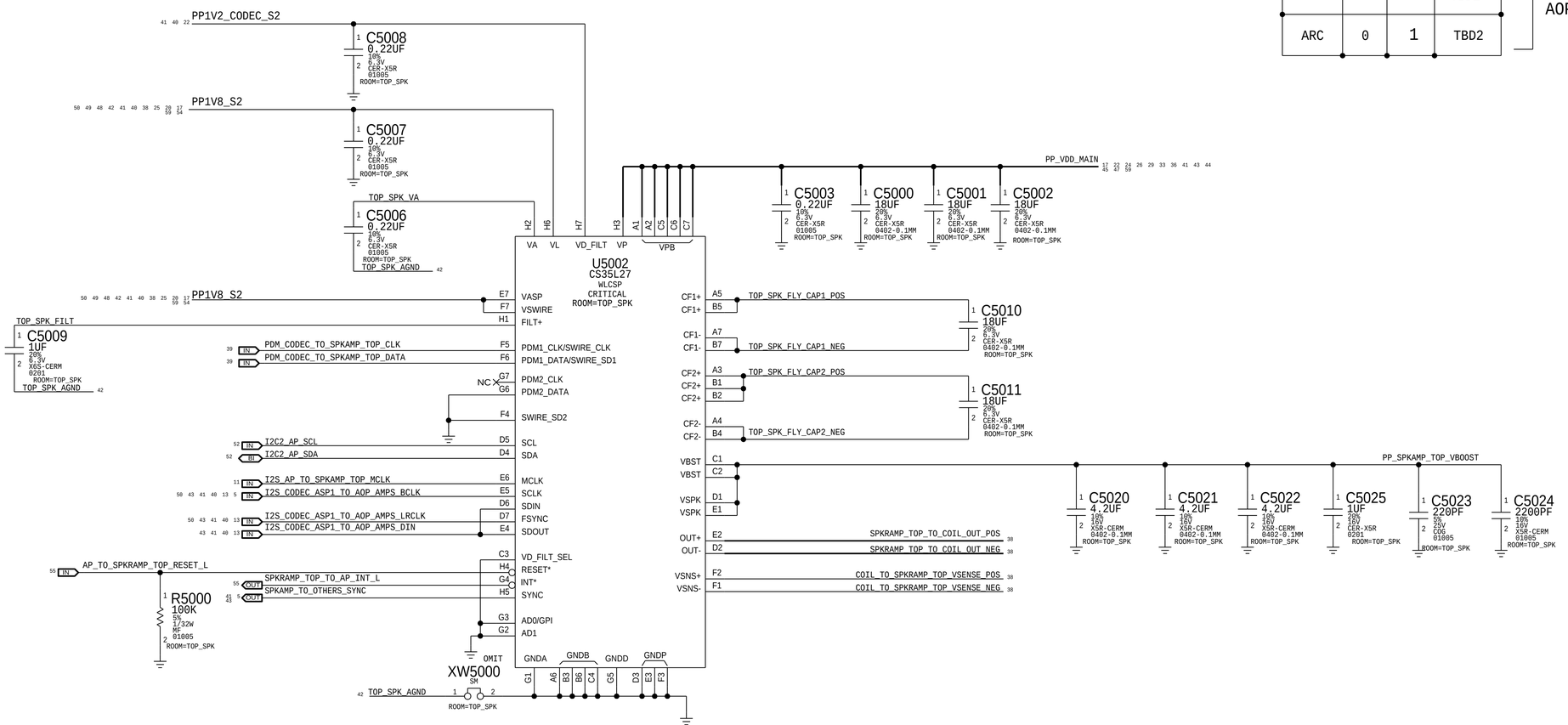
AMP	AD0	AD1	I2C_ADR	
TOP	0	0	TBD1	AP I2C2
BOT	0	0	TBD1	AOP I2C1
ARC	0	1	TBD2	



SYNC_DATE=04/05/2017

PAGE TITLE

AUDIO: NORTH SPKAMP

Apple Inc.

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AMP	AD0	AD1	I2C_ADR	
TOP	0	0	TBD1	AP I2C2
BOT	0	0	TBD1	AOP I2C1
ARC	0	1	TBD2	

PP1V2_ARC_VD_FILT
C5108 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC
PP1V8_ARC_VA_INTERNAL
C5107 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC
C5106 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC
ARC_AGND
PP_VDD_MAIN
C5103 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC
C5100 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC
C5101 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC
C5102 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC
VA VL VD_FILT VP VPB

U5102
CS35L27
WLCSP
CRITICAL
ROOM=ARC

E7 VASP
F7 VSWIRE
H1 FILT+
ARC_FILT
C5109 1UF 20% 6.3V X6S-CERM 0201 ROOM=ARC
F5 PDM1_CLK/SWIRE_CLK
F6 PDM1_DATA/SWIRE_SD1
NC G7 PDM2_CLK
G6 PDM2_DATA
F4 SWIRE_SD2
I2C1_AOP_SCL D5 SCL
I2C1_AOP_SDA D4 SDA
CODEC_TO_SPKRAMP_BOT_ARC_MCLK E6 MCLK
I2S_CODEC_ASP1_TO_AOP_AMPS_BCLK E5 SCLK
I2S_CODEC_ASP1_TO_AOP_AMPS_DIN D6 SDIN
I2S_CODEC_ASP1_TO_AOP_AMPS_LRCLK D7 FSYNC
I2S_AOP_AMPS_TO_CODEC_ASP1_DOUT E4 SDOUT
NC C3 VD_FILT_SEL
H4 RESET*
SPKAMP_BOT_ARC_TO_AOP_INT_L G4 INT*
SPKAMP_TO_OTHERS_SYNC H5 SYNC
G3 ADO/GPI
PP1V8_ARC_VA_INTERNAL G2 AD1
GNDA GNDB GNDD GNDP
G1 A6 B3 B6 C4 C5 D3 E3 F3

CF1+ A5 ARC_FLY_CAP1_POS
CF1+ B5
CF1- A7
CF1- B7 ARC_FLY_CAP1_NEG
C5110 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC
CF2+ A3 ARC_FLY_CAP2_POS
CF2+ B1
CF2+ B2
CF2- A4
CF2- B4 ARC_FLY_CAP2_NEG
C5111 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC
VBST C1
VBST C2
VSPK D1
VSPK E1
OUT+ E2 ARC_TO_SOLENOID_OUT_POS
OUT- D2 ARC_TO_SOLENOID_OUT_NEG
VSNS+ F2 SOLENOID_TO_ARC_VSENSE_POS
VSNS- F1 SOLENOID_TO_ARC_VSENSE_NEG

PP_ARC_VBOOST
C5120 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC
C5121 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC
C5122 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC
C5125 1UF 20% 16V CER-X5R 0201 ROOM=ARC
C5123 220PF 5% 25V C0G 01005 ROOM=ARC
C5124 2200PF 10% 16V X5R-CERM 01005 ROOM=ARC

R5112 61.9K 1% 1/32W MF 01005
NFC_TO_ARC_RESET_L
R5111 61.9K 1% 1/32W MF 01005
NFC_TO_ARC_TRIG
PMU_MASK_NFC_TO_ARC_TRIG
PMU_NFC_TO_ARC_RESET_L
R5100 200K 1% 1/32W MF 01005
R5101 200K 1% 1/32W MF 01005

OMIT
XW5100 SM
ARC_AGND
ROOM=ARC
Place off of allston GND pin

SYNC_DATE=04/05/2017

PAGE TITLE
ARC: AMP

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Display Control Signals

FL5700
FERR-150OHM-25%-200MA
01005
ROOM=B2B_DISPLAY

55 IN PMU_TO_DISPLAY_RESET_L → PMU_TO_DISPLAY_RESET_CONN_L 44

R5700 100K 5% 1/32W MF 01005 NOSTUFF
C5700 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

55 IN PMU_TO_DISPLAY_PANICB → PMU_TO_DISPLAY_PANICB_CONN 44

R5701 10 5% 1/32W MF 01005 ROOM=B2B_DISPLAY
C5701 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

9 OUT DISPLAY_TO_AP_BSYNC_WATCHDOG → DISPLAY_TO_AP_BSYNC_WATCHDOG_CONN 44

R5702 0.00 0% 1/32W MF 01005 ROOM=B2B_DISPLAY
C5702 56PF 5% 25V NP0_C0G-CERM 01005 ROOM=B2B_DISPLAY

FL5703
FERR-150OHM-25%-200MA
01005
ROOM=B2B_DISPLAY

23 IN DISPLAY_TO_PMU_AMUX → DISPLAY_TO_PMU_AMUX_CONN 44

C5703 56PF 5% 25V NP0_C0G-CERM 01005 ROOM=B2B_DISPLAY

R5704 0.00 0% 1/32W MF 01005 ROOM=B2B_DISPLAY

9 IN ISP_TO_DISPLAY_FLASH_INT → ISP_TO_DISPLAY_FLASH_INT_CONN 44

C5704 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

Here for syncccing purposes

22 PP3V0_DISPLAY = PP3V0_DISPLAY 44
MAKE_BASE=TRUE

C2910 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

22 PP1V0_DISPLAY_DVDD = PP1V0_DISPLAY_DVDD 44
MAKE_BASE=TRUE

C2914 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

1.2V LDO is for LGC test chip

Once normal panel is available switch to 1.1V

29 22 20 17 PP1V26_S2 → A1 IN
55 PMU_TO_DISPLAY_LDO_EN → B1 EN

U5701
SCY99224-1.15V
WLCSP
CRITICAL
ROOM=B2B_DISPLAY
OUT A2
GND B2

C5721 0.47UF 20% 6.3V X5R 01005 ROOM=B2B_DISPLAY
R5720 100K 5% 1/32W MF 01005 ROOM=B2B_DISPLAY NOSTUFF
C5705 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=B2B_DISPLAY

FL5781
FERR-33OHM-25%-1.5A
0201
ROOM=B2B_DISPLAY

PP1V1_DISPLAY_VDD → PP1V1_DISPLAY_VDD_CONN 44
VOLTAGE=1.1V

C5706 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

Display 1V0 LDO for D33 second display vendor

rdar: #29872369

R5705 1.00K 5% 1/32W MF 01005 ROOM=B2B_DISPLAY

55 DISPLAY_TO_AP_PANEL_ID → DISPLAY_TO_AP_PANEL_ID_R 44

Display MIPI

Display MIPI

L5700
350HM-7GHZ-0.05MA-3OHM
TAM0403S-SM
SYM_VER=1
ROOM=B2B_DISPLAY
GND_VOID

9 IN 90_MIPI_AP_TO_DISPLAY_DATA0_N → 90_MIPI_AP_TO_DISPLAY_DATA0_CONN_N 44
9 IN 90_MIPI_AP_TO_DISPLAY_DATA0_P → 90_MIPI_AP_TO_DISPLAY_DATA0_CONN_P 44

L5710
350HM-7GHZ-0.05MA-3OHM
TAM0403S-SM
SYM_VER=1
ROOM=B2B_DISPLAY
GND_VOID

9 IN 90_MIPI_AP_TO_DISPLAY_DATA1_N → 90_MIPI_AP_TO_DISPLAY_DATA1_CONN_N 44
9 IN 90_MIPI_AP_TO_DISPLAY_DATA1_P → 90_MIPI_AP_TO_DISPLAY_DATA1_CONN_P 44

L5720
350HM-7GHZ-0.05MA-3OHM
TAM0403S-SM
SYM_VER=1
ROOM=B2B_DISPLAY
GND_VOID

9 IN 90_MIPI_AP_TO_DISPLAY_DATA2_P → 90_MIPI_AP_TO_DISPLAY_DATA2_CONN_P 44
9 IN 90_MIPI_AP_TO_DISPLAY_DATA2_N → 90_MIPI_AP_TO_DISPLAY_DATA2_CONN_N 44

L5730
350HM-7GHZ-0.05MA-3OHM
TAM0403S-SM
SYM_VER=1
ROOM=B2B_DISPLAY
GND_VOID

9 IN 90_MIPI_AP_TO_DISPLAY_DATA3_P → 90_MIPI_AP_TO_DISPLAY_DATA3_CONN_P 44
9 IN 90_MIPI_AP_TO_DISPLAY_DATA3_N → 90_MIPI_AP_TO_DISPLAY_DATA3_CONN_N 44

L5740
350HM-7GHZ-0.05MA-3OHM
TAM0403S-SM
SYM_VER=1
ROOM=B2B_DISPLAY
GND_VOID

9 IN 90_MIPI_AP_TO_DISPLAY_CLK_P → 90_MIPI_AP_TO_DISPLAY_CLK_CONN_P 44
9 IN 90_MIPI_AP_TO_DISPLAY_CLK_N → 90_MIPI_AP_TO_DISPLAY_CLK_CONN_N 44

Display Flex Connector

Rcpt: 516S00210 <-- This one on MLB
Plug: 516S00211

J5700
BM28P0.6-34DS/2-0.35V
F-ST-SM
ROOM=B2B_DISPLAY

44	PP_VDD_MAIN_DISPLAY_CONN	35	PWR	36	PP_VDD_MAIN_DISPLAY_CONN 44
44	PP1V8_DISPLAY_DVDD_CONN	1	SIG	2	
44	DISPLAY_TO_PMU_AMUX_CONN	3		4	
44	PMU_TO_DISPLAY_RESET_CONN_L	5		6	NC
44	DISPLAY_TO_AP_PANEL_ID_R	7		8	PP3V0_DISPLAY_VCI_CONN 44
44	PMU_TO_DISPLAY_PANICB_CONN	9		10	NC_SPI_AP_TO_DISPLAY_FLASH_SCLK 44
	NC_SPI_DISPLAY_FLASH_CS_L	11		12	PP1V0_DISPLAY_VDD_CONN 44
	NC_PP_VPP	13		14	PP1V1_DISPLAY_VDD_CONN 44
	NC_SPI_AP_TO_DISPLAY_FLASH_MOSI	15		16	ISP_TO_DISPLAY_FLASH_INT_CONN 44
		17		18	NC_SPI_DISPLAY_FLASH_TO_AP_MISO
44	90_MIPI_AP_TO_DISPLAY_DATA2_CONN_P	19		20	DISPLAY_TO_AP_BSYNC_WATCHDOG_CONN 44
44	90_MIPI_AP_TO_DISPLAY_DATA2_CONN_N	21		22	
		23		24	
44	90_MIPI_AP_TO_DISPLAY_CLK_CONN_P	25		26	90_MIPI_AP_TO_DISPLAY_DATA1_CONN_P 44
44	90_MIPI_AP_TO_DISPLAY_CLK_CONN_N	27		28	90_MIPI_AP_TO_DISPLAY_DATA1_CONN_N 44
		29		30	
44	90_MIPI_AP_TO_DISPLAY_DATA3_CONN_P	31		32	90_MIPI_AP_TO_DISPLAY_DATA0_CONN_P 44
44	90_MIPI_AP_TO_DISPLAY_DATA3_CONN_N	33		34	90_MIPI_AP_TO_DISPLAY_DATA0_CONN_N 44
		37	PWR	38	

Display Power

FL5780
FERR-33OHM-25%-1.5A
0201
ROOM=B2B_DISPLAY

36 34 32 31 30 29 20 19 17 6 59 57 PP1V8_IO → PP1V8_DISPLAY_DVDD_CONN 44

C5781 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

FL5782
0 5% 1/20W MF 0201

44 PP1V0_DISPLAY_DVDD → PP1V0_DISPLAY_VDD_CONN 44

C5782 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

FL5783
FERR-70OHM-25%-0.300A
01005
ROOM=B2B_DISPLAY

44 PP3V0_DISPLAY → PP3V0_DISPLAY_VCI_CONN 44

C5783 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

XW5784
SHORT-0201
ROOM=B2B_DISPLAY

43 42 41 36 33 29 26 24 23 17 59 47 45 PP_VDD_MAIN → PP_VDD_MAIN_DISPLAY_CONN 44

XW5785
SHORT-0201
ROOM=B2B_DISPLAY

C5784 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY
C5785 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY
C5786 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

PAGE TITLE
CG: B2B Display

Apple Inc.

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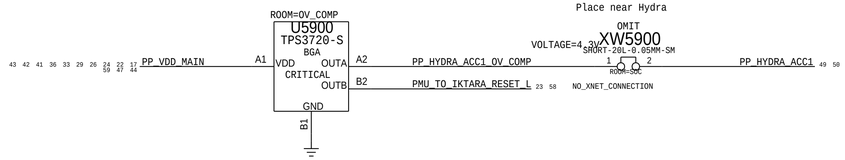
VDD_MAIN OV CUT-OFF CIRCUIT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01375	353S01398	ALT_PARTS	U5900	ON SEMI

PAGE TITLE
I/O: Overvoltage Cut-Off Circuit

Apple Inc.

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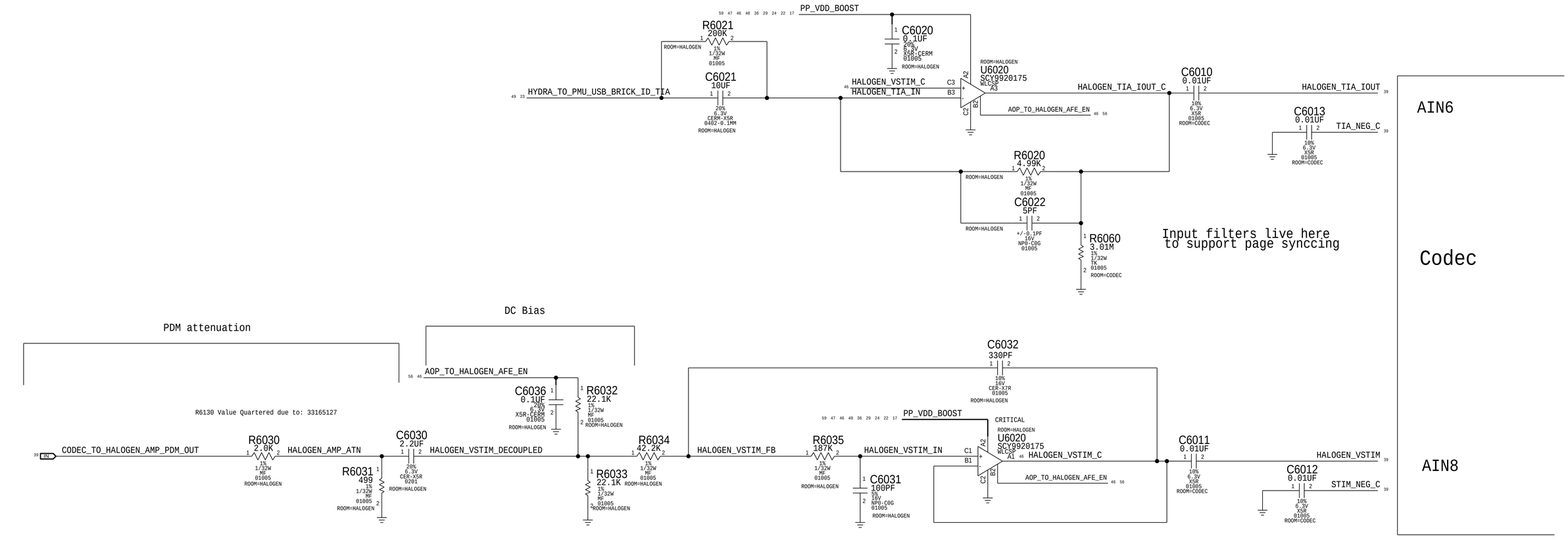
CDS_LTB=apple

LDCM



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Apple Inc.	
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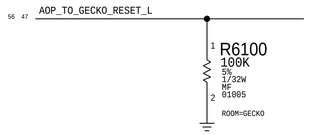
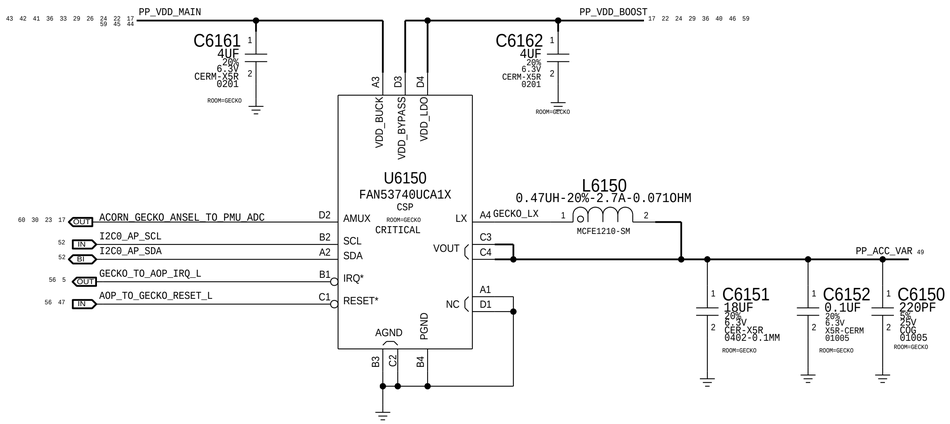
GECKO Reset Pull Down



Gecko

I2C ADDRESS: 0X52



IND Alternate

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00854	152S00853	ALT_PARTS	L6150	IND,PWR,0.47UH,20%,2.8A,CY
152S00855	152S00853	ALT_PARTS	L6150	IND,PWR,0.47UH,20%,2.7A,Murata

PAGE TITLE

I/O: Gecko

Apple Inc.

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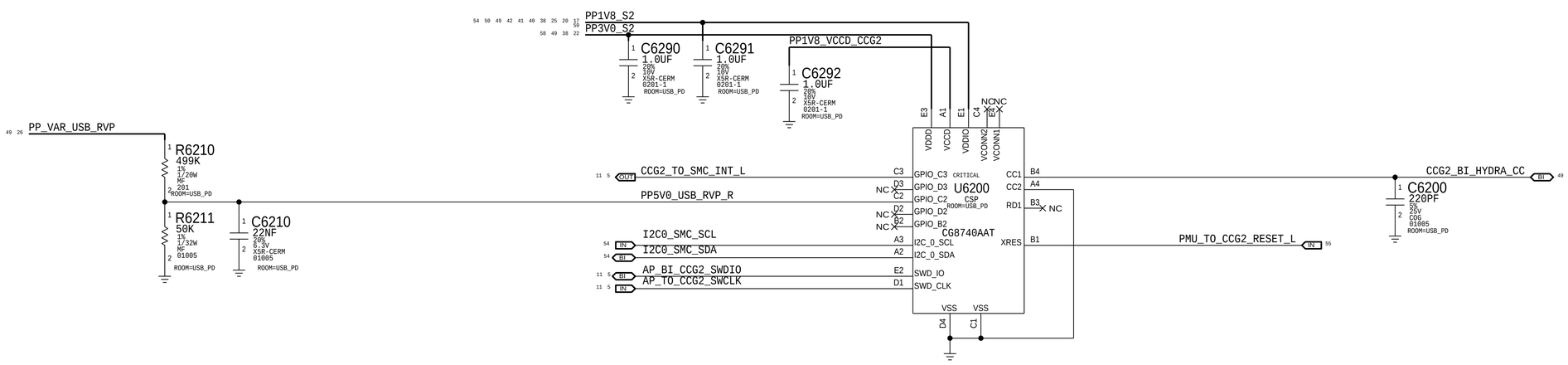
USB-PD



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Apple Inc.	
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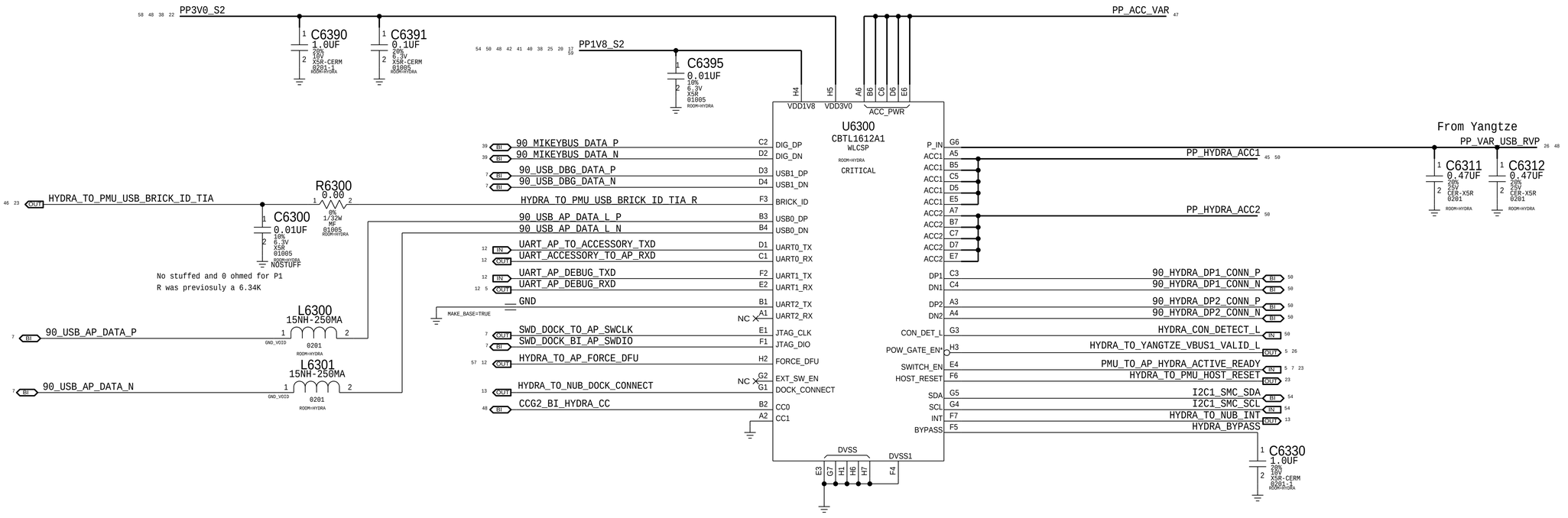
Hydra

I2C Address: 0011010X



PAGE TITLE	I/O: Hydra
	Apple Inc.
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ARC

SOLENOID_TO_ARC_VSENSE_POS → R6490 100 5% 1/32W MF 01005 → SOLENOID_TO_ARC_VSENSE_POS_CONN
- C6475 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

SOLENOID_TO_ARC_VSENSE_NEG → R6491 100 5% 1/32W MF 01005 → SOLENOID_TO_ARC_VSENSE_NEG_CONN
- C6474 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

FL6400

FERR-1500HM-25%-200MA 01005 ROOM=B2B_DOCK

PP1V8_S2 → PP1V8_S2_SAKONNET_CONN
- C6400 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

I2C0_AP_SCL (IN)
- C6416 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

I2C0_AP_SDA (BI)
- C6418 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

I2S_CODEC_ASP1_TO_AOP_AMPS_BCLK (IN) → R6419 49.9 1% 1/32W MF 01005 → I2S_CODEC_ASP1_TO_AOP_AMPS_BCLK_CONN
- C6419 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

I2S_CODEC_ASP1_TO_AOP_AMPS_LRCLK (IN) → R6420 49.9 1% 1/32W MF 01005 → I2S_CODEC_ASP1_TO_AOP_AMPS_LRCLK_CONN
- C6420 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

I2S_AOP_AMPS_TO_CODEC_ASP1_DOUT (BI) → R6421 49.9 1% 1/32W MF 01005 → I2S_AOP_AMPS_TO_CODEC_ASP1_DOUT_CONN
- C6421 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

POTASSIUM

PP1V8_IMU_S2
- R6440 10K 5% 1/32W MF 01005

POTASSIUM_TO_AOP_INT (OUT) → R6433 0.00 0% 1/32W MF 01005 ROOM=B2B_BUTTON → POTASSIUM_TO_AOP_INT_CONN
- C6433 220PF 5% 25V C0G 01005 ROOM=B2B_BUTTON

I2C1_AOP_SCL (IN)
- C6431 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

I2C1_AOP_SDA (BI) → R6432 0.00 0% 1/32W MF 01005 ROOM=B2B_PEARL → I2C1_AOP_BI_POTASSIUM_SDA_CONN
- C6432 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

CKPLUS_WAIVE=I2C_PULLUP

FL6430

FERR-150OHM-25%-200MA 01005 ROOM=B2B_DOCK

PP1V8_IMU_S2 → PP1V8_IMU_POTASSIUM_S2_CONN
- C6430 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

LOWER MIC1

LOWERMIC1_TO_CODEC_AIN1_P (OUT) → FL6450 FERR-150OHM-25%-200MA → LOWERMIC1_TO_CODEC_AIN1_CONN_P
- C6450 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

LOWERMIC1_TO_CODEC_AIN1_N (OUT) → FL6452 FERR-150OHM-25%-200MA → LOWERMIC1_TO_CODEC_AIN1_CONN_N
- C6452 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

PP_CODEC_TO_LOWERMIC1_BIAS → FL6454 FERR-150OHM-25%-200MA → PP_CODEC_TO_LOWERMIC1_BIAS_CONN
- C6454 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

PHALANX

PMU_TO_PHALANX2 (IN)
- C6465 330PF 10% 16V CER-X7R 01005 ROOM=B2B_DOCK

PMU_TO_PHALANX1 (BI)
- C6466 330PF 10% 16V CER-X7R 01005 ROOM=B2B_DOCK

Hydra

HYDRA_CON_DETECT_L (OUT) → R6410 100 5% 1/32W MF 01005 ROOM=B2B_DOCK → HYDRA_CON_DETECT_CONN_L
- C6410 27PF 5% 16V NP0-C0G 01005 ROOM=B2B_DOCK

PP_HYDRA_ACC1 → FL6411 10-OHM-1.1A 01005 ROOM=B2B_DOCK → PP_HYDRA_ACC1_CONN
- C6411 100PF 5% 16V NP0-C0G 01005 ROOM=B2B_DOCK

PP_HYDRA_ACC2 → FL6413 22-OHM-25%-1800MA 0201 ROOM=B2B_DOCK → PP_HYDRA_ACC2_CONN
- C6413 100PF 5% 16V NP0-C0G 01005 ROOM=B2B_DOCK

MIC4

LOWERMIC4_TO_CODEC_AIN4_N (OUT) → FL6462 FERR-150OHM-25%-200MA → LOWERMIC4_TO_CODEC_AIN4_CONN_N
- C6462 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

PP_CODEC_TO_LOWERMIC4_BIAS → FL6464 FERR-150OHM-25%-200MA → PP_CODEC_TO_LOWERMIC4_BIAS_CONN
- C6464 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

LOWERMIC4_TO_CODEC_AIN4_P (OUT) → FL6460 FERR-150OHM-25%-200MA → LOWERMIC4_TO_CODEC_AIN4_CONN_P
- C6460 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=B2B_DOCK

DOCK FLEX CONNECTOR

Rcpt: 516S00423 <-- This one on MLB
Plug: 516S00424

J6400 BM28PS-44DS-2-0.35V F-ST-SM

SPKRAMP_BOT_TO_COIL_OUT_NEG	45	46	
SPKRAMP_BOT_TO_COIL_OUT_POS	1	2	COIL_TO_SPKRAMP_BOT_VSENSE_NEG_CONN
	3	4	
COIL_TO_SPKRAMP_BOT_VSENSE_POS_CONN	5	6	PP_CODEC_TO_LOWERMIC4_BIAS_CONN
	7	8	LOWERMIC4_TO_CODEC_AIN4_CONN_N
LOWERMIC4_TO_CODEC_BIAS_FILT_RET	9	10	PP1V8_IMU_POTASSIUM_S2_CONN
LOWERMIC4_TO_CODEC_AIN4_CONN_P	11	12	I2C1_AOP_BI_POTASSIUM_SDA_CONN
POTASSIUM_TO_AOP_INT_CONN	13	14	PMU_TO_PHALANX2
I2C1_AOP_SCL	15	16	LOWERMIC1_TO_CODEC_BIAS_FILT_RET
PMU_TO_PHALANX1	17	18	LOWERMIC1_TO_CODEC_AIN1_CONN_P
PP_CODEC_TO_LOWERMIC1_BIAS_CONN	19	20	MIKEYBUS_REFERENCE
LOWERMIC1_TO_CODEC_AIN1_CONN_N	21	22	
I2C0_AP_SDA	23	24	90_HYDRA_DP2_CONN_P
HYDRA_CON_DETECT_CONN_L	25	26	90_HYDRA_DP2_CONN_N
I2S_AOP_AMPS_TO_CODEC_ASP1_DOUT_CONN	27	28	90_HYDRA_DP1_CONN_P
PP1V8_S2_SAKONNET_CONN	29	30	90_HYDRA_DP1_CONN_N
I2S_CODEC_ASP1_TO_AOP_AMPS_BCLK_CONN	31	32	
I2C0_AP_SCL	33	34	ARC_TO_SOLENOID_OUT_POS
I2S_CODEC_ASP1_TO_AOP_AMPS_LRCLK_CONN	35	36	
	37	38	SOLENOID_TO_ARC_VSENSE_POS_CONN
	39	40	PP_HYDRA_ACC1_CONN
ARC_TO_SOLENOID_OUT_NEG	41	42	PP_HYDRA_ACC2_CONN
SOLENOID_TO_ARC_VSENSE_NEG_CONN	43	44	
PP_VBUS1_E75	47	48	

- C6490 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
- C6491 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
- C6492 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
- C6493 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
- C6494 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
- C6495 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
- C6496 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
- C6497 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK

SOUTH SPEAKER

COIL_TO_SPKRAMP_BOT_VSENSE_NEG (OUT) → R6480 100 5% 1/32W MF 01005 ROOM=B2B_DOCK → COIL_TO_SPKRAMP_BOT_VSENSE_NEG_CONN
- C6480 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

COIL_TO_SPKRAMP_BOT_VSENSE_POS (OUT) → R6482 100 5% 1/32W MF 01005 ROOM=B2B_DOCK → COIL_TO_SPKRAMP_BOT_VSENSE_POS_CONN
- C6482 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

SPKRAMP_BOT_TO_COIL_OUT_POS (IN)
- C6483 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
- C6486 1000PF 10% 25V X5R 0201 ROOM=B2B_DOCK

SPKRAMP_BOT_TO_COIL_OUT_NEG (IN)
- C6485 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
- C6487 1000PF 10% 25V X5R 0201 ROOM=B2B_DOCK

ARC_TO_SOLENOID_OUT_NEG
ARC_TO_SOLENOID_OUT_POS
- C6471 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
- C6472 1000PF 10% 25V X5R 0201
- C6470 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
- C6473 1000PF 10% 25V X5R 0201

PAGE TITLE: I/O: B2B Dock

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Top Board Interposer APN:998-12513 <--- STUFFED
Bot Board Interposer APN:998-12514

J_INT_BOT
SMT-PAD
SYM 1 OF 2
INTERPOSER-MLB-BOT-V3-D32

57	GND	1	IO1	IO95	95	AP_TO_NFC_DEV_WAKE	57
57	GND	2	IO2	IO96	96	AP_TO_NFC_FW_DWLD_REQ	57
57	GND	3	IO3	IO97	97	GND	57
57	GND	4	IO4	IO98	98	PMU_TO_NFC_VDD_MAIN_EN	57
57	GND	5	IO5	IO99	99	UART_AOP_TO_BB_TXD	57
57	GND	6	IO6	IO100	100	UART_AP_TO_GNSS_TXD	57
57	PMU_TO_SYSTEM_COLD_RESET_L	7	IO7	IO101	101	GND	57
57	GND	8	IO8	IO102	102	AP_TO_BB_COREDUMP_TRIG	57
57	AP_TO_CAMPMU_RESET_L	9	IO9	IO103	103	UART_AP_TO_NFC_TXD	57
57	GND	10	IO10	IO104	104	UART_NFC_TO_AP_RXD	57
57	BB_TO_MANY_GSM_BURST_IND	11	IO11	IO105	105	BB_TO_AP_RESET_DETECT_L	57
57	GND	12	IO12	IO106	106	GND	57
57	HALL_CASE_TO_AOP_NORTH_L	13	IO13	IO107	107	BOARD_ID2	57
57	GND	14	IO14	IO108	108	AP_TO_GNSS_TIME_MARK	57
57	AP_TO_TOUCH_SCAN_CLK	15	IO15	IO109	109	NC_INTERPOSER_109	57
57	GND	16	IO16	IO110	110	AP_TO_BB_PEAK_POWER_INDICATOR	57
57	I2S_BB_TO_AP_BCLK	17	IO17	IO111	111	AP_TO_BBPMU_RADIO_ON_L	57
57	GND	18	IO18	IO112	112	PP_VDD_MAIN	57
57	I2S_BB_TO_AP_DIN	19	IO19	IO113	113	PP_VDD_MAIN	57
57	GND	20	IO20	IO114	114	PP_VDD_MAIN	57
57	I2S_AP_TO_BB_DOUT	21	IO21	IO115	115	GND	57
57	GND	22	IO22	IO116	116	90_PCIE_BB_TO_AP_RXD_N	57
57	I2S_BB_TO_AP_LRCLK	23	IO23	IO117	117	90_PCIE_BB_TO_AP_RXD_P	57
57	GND	24	IO24	IO118	118	GND	57
57	PP1V8_ALWAYS	25	IO25	IO119	119	90_PCIE_AP_TO_BB_TXD_N	57
57	GND	26	IO26	IO120	120	90_PCIE_AP_TO_BB_TXD_P	57
57	GND	27	IO27	IO121	121	GND	57
57	GND	28	IO28	IO122	122	90_PCIE_AP_TO_BB_REFCLK_P	57
57	GND	29	IO29	IO123	123	90_PCIE_AP_TO_BB_REFCLK_N	57
57	GND	30	IO30	IO124	124	GND	57
57	GND	31	IO31	IO125	125	UART_BB_TO_AOP_RXD	57
57	GND	32	IO32	IO126	126	UART_GNSS_TO_AP_RXD	57
57	GND	33	IO33	IO127	127	PCIE_AP_TO_BB_PERST_L	57
57	GND	34	IO34	IO128	128	UART_NFC_TO_AP_CTS_L	57
57	GND	35	IO35	IO129	129	GND	57
57	GND	36	IO36	IO130	130	UART_AP_TO_NFC_RTS_L	57
57	GND	37	IO37	IO131	131	PMU_AMUX_BY	57
57	GND	38	IO38	IO132	132	PMU_AMUX_AY	57
57	GND	39	IO39	IO133	133	GND	57
57	GND	40	IO40	IO134	134	PCIE_BB_BI_AP_CLKREQ_L	57
57	GND	41	IO41	IO135	135	NC_INT_135	57
57	GND	42	IO42	IO136	136	BB_TO_AP_PEAK_POWER_INDICATOR	57
57	GND	43	IO43	IO137	137	GND	57
57	GND	44	IO44	IO138	138	PP_VDD_MAIN	57
57	GND	45	IO45	IO139	139	PP_VDD_MAIN	57
57	GND	46	IO46	IO140	140	PP_VDD_MAIN	57
57	GND	47	IO47	IO141	141	GND	57
57	GND	48	IO48	IO142	142	GND	57
57	GND	49	IO49	IO143	143	GND	57
57	NFC_TO_ARC_RESET_L	50	IO50	IO144	144	GND	57
57	GND	51	IO51	IO145	145	GND	58
57	NFC_TO_ARC_TRIG	52	IO52	IO146	146	GND	58
57	GND	53	IO53	IO147	147	GND	58
57	GND	54	IO54	IO148	148	GND	58
57	GND	55	IO55	IO149	149	GND	58
57	GND	56	IO56	IO150	150	GND	58
57	GND	57	IO57	IO151	151	GND	58
57	GND	58	IO58	IO152	152	GND	58
57	GND	59	IO59	IO153	153	GND	58
57	GND	60	IO60	IO154	154	PP_VDD_MAIN	58
57	GND	61	IO61	IO155	155	PP_VDD_MAIN	58
57	GND	62	IO62	IO156	156	GND	58
57	GND	63	IO63	IO157	157	PP_VDD_MAIN	58
57	GND	64	IO64	IO158	158	PP_VDD_MAIN	58
57	AP_TO_BB_RESET_L	65	IO65	IO159	159	GND	58
57	GND	66	IO66	IO160	160	PMU_TO_NFC_EN	58
57	SWD_AOP_BI_BB_SWDIO	67	IO67	IO161	161	GND	58
57	GND	68	IO68	IO162	162	PMU_TO_BBPMU_RESET_L	58
57	UART_GNSS_TO_AP_CTS_L	69	IO69	IO163	163	GND	58
57	GND	70	IO70	IO164	164	PMU_TO_TOUCH_CLK32K	58
57	UART_AP_TO_GNSS_RTS_L	71	IO71	IO165	165	GND	58
57	GND	72	IO72	IO166	166	PCIE_WLAN_BI_AP_CLKREQ_L	58
57	PCIE_AP_TO_WLAN_PERST_L	73	IO73	IO167	167	GND	58
57	GND	74	IO74	IO168	168	GND	58
57	AP_TO_RACER_RESET_L	75	IO75	IO169	169	BB_TO_PMU_PCIE_HOST_WAKE_L	58
57	GND	76	IO76	IO170	170	GND	58
57	AP_TO_WLAN_TIME_SYNC	77	IO77	IO171	171	GND	58
57	GND	78	IO78	IO172	172	WLAN_TO_PMU_HOST_WAKE	58
57	GNSS_TO_AP_LOW_PWR_IND	79	IO79	IO173	173	GND	58
57	GND	80	IO80	IO174	174	PMU_TO_WLAN_CLK32K	58
57	HYDRA_TO_AP_FORCE_DFU	81	IO81	IO175	175	GND	58
57	GND	82	IO82	IO176	176	NFC_TO_AOP_HOST_WAKE	58
57	PP1V8_S2	83	IO83	IO177	177	GND	58
57	PP1V8_S2	84	IO84	IO178	178	TOUCH_TO_MANY_FORCE_PWM	58
57	GND	85	IO85	IO179	179	GND	58
57	GND	86	IO86	IO180	180	UART_AP_TO_BT_TXD	58
57	GND	87	IO87	IO181	181	GND	58
57	GND	88	IO88	IO182	182	UART_AP_TO_BT_RTS_L	58
57	GND	89	IO89	IO183	183	GND	58
57	INTERPOSER_PIN_90	90	IO90	IO184	184	GND	58
57	GND	91	IO91	IO185	185	GND	58
57	AP_TO_BB_COEX	92	IO92	IO186	186	GND	58
57	BB_TO_AP_COEX	93	IO93	IO187	187	GND	58
57	GND	94	IO94	IO188	188	GND	58

J_INT_BOT
SMT-PAD
SYM 2 OF 2
INTERPOSER-MLB-BOT-V3-D32

58	GND	189	IO189	IO282	282	GND	58
58	GND	190	IO190	IO283	283	GND	58
58	GND	191	IO191	IO284	284	GND	58
58	GND	192	IO192	IO285	285	GND	58
58	AP_CANARY2	193	IO193	IO286	286	GND	60
58	GND	194	IO194	IO287	287	ACORN_GECKO_ANSEL_TO_PMU_ADC	60
58	GND	195	IO195	IO288	288	GND	60
58	PP1V8_NFC_S2	196	IO196	IO289	289	RACER_TO_AOP_INT_L	60
58	PMU_TO_GNSS_EN	197	IO197	IO290	290	GND	60
58	PMU_TO_BT_REG_ON	198	IO198	IO291	291	HALL_CASE_TO_AOP_SOUTH_L	60
58	GND	199	IO199	IO292	292	GND	60
58	90_PCIE_AP_TO_WLAN_REFCLK_N	200	IO200	IO293	293	PMU_TO_IKTARA_EN_EXT_1V8	60
58	90_PCIE_AP_TO_WLAN_REFCLK_P	201	IO201	IO294	294	GND	60
58	GND	202	IO202	IO295	295	IKTARA_TO_SMC_INT	60
58	90_PCIE_AP_TO_WLAN_TXD_P	203	IO203	IO296	296	GND	60
58	90_PCIE_AP_TO_WLAN_TXD_N	204	IO204	IO297	297	I2C0_SMC_SCL	60
58	GND	205	IO205	IO298	298	I2C0_SMC_SDA	60
58	90_PCIE_WLAN_TO_AP_RXD_N	206	IO206	IO299	299	GND	60
58	90_PCIE_WLAN_TO_AP_RXD_P	207	IO207	IO300	300	IKTARA_COIL2	60
58	GND	208	IO208	IO301	301	IKTARA_COIL2	60
58	PP3V0_S2	209	IO209	IO302	302	IKTARA_COIL2	60
58	PP1V8_TOUCH_RACER_S2	210	IO210	IO303	303	IKTARA_COIL2	60
58	PP1V8_TOUCH_RACER_S2	211	IO211	IO304	304	IKTARA_COIL1	60
58	PMU_TO_WLAN_REG_ON	212	IO212	IO305	305	IKTARA_COIL1	60
58	RADIO_PA_NTC	213	IO213	IO306	306	IKTARA_COIL1	60
58	BT_TO_AP_TIME_SYNC	214	IO214	IO307	307	IKTARA_COIL1	60
58	UART_BT_TO_AP_RXD	215	IO215	IO308	308	GND	60
58	GND	216	IO216	IO309	309	NC_INTERPOSER_309	60
58	GND	217	IO217	IO310	310	GND	60
58	UART_BT_TO_AP_CTS_L	218	IO218	IO311	311	NC_INTERPOSER_311	60
58	GND	219	IO219	IO312	312	GND	60
58	GND	220	IO220	IO313	313	AP_CANARY1	60
58	GND	221	IO221	IO314	314	GND	60
58	GND	222	IO222	IO315	315	GND	60
58	GND	223	IO223	IO316	316	GND	60
58	GND	224	IO224	IO317	317	GND	60
58	GND	225	IO225	IO318	318	GND	60
58	GND	226	IO226	IO319	319	GND	60
58	GND	227	IO227	IO320	320	GND	60
58	GND	228	IO228	IO321	321	GND	60
58	PP_VBUS1_E75	229	IO229	IO322	322	GND	60
58	GND	230	IO230	IO323	323	GND	60
58	PP_GPU_LVCC	231	IO231	IO324	324	GND	60
58	GND	232	IO232	IO325	325	GND	60
58	PP_CPU_PCORE_LVCC	233	IO233	IO326	326	GND	60
58	GND	234	IO234	IO327	327	GND	60
58	PP_BATT_VCC	235	IO235	IO328	328	GND	60
58	PP_BATT_VCC	236	IO236	IO329	329	GND	60
58	GND	237	IO237	IO330	330	GND	60
58	AP_TO_BT_DEVICE_WAKE	238	IO238	IO331	331	GND	60
58	AOP_TO_WLAN_CONTEXT_A	239	IO239	IO332	332	GND	60
58	UART_AOP_TO_RACER_TXD	240	IO240	IO333	333	GND	60
58	SWD_AOP_TO_MANY_SWCLK	241	IO241	IO334	334	GND	60
58	SPI_AP_TO_RACER_MOSI	242	IO242	IO335	335	GND	60
58	SPI_AP_TO_RACER_SCLK	243	IO243	IO336	336	GND	60
58	PP1V1_RACER_S2	244	IO244	IO337	337	GND	60
58	PP1V1_RACER_S2	245	IO245	IO338	338	GND	60
58	PP1V1_RACER_S2	246	IO246	IO339	339	GND	60
58	AP_TO_RACER_REF_CLK	247	IO247	IO340	340	GND	60
58	GND	248	IO248	IO341	341	GND	60
58	AOP_TO_BBPMU_COEX	249	IO249	IO342	342	GND	60
58	PP_VBUS2_IKTARA	250	IO250	IO343	343	GND	60
58	PP_VBUS2_IKTARA	251	IO251	IO344	344	GND	60
58	PP_VBUS2_IKTARA	252	IO252	IO345	345	GND	60
58	PP_VBUS2_IKTARA	253	IO253	IO346	346	GND	60
58	GND	254	IO254	IO347	347	GND	60
58	AOP_TO_WLAN_CONTEXT_B	255	IO255	IO348	348	GND	60
58	GND	256	IO256	IO349	349	GND	60
58	UART_RACER_TO_AOP_RXD	257	IO257	IO350	350	GND	60
58	GND	258	IO258	IO351	351	GND	60
58	SPI_RACER_TO_AP_MISO	259	IO259	IO352	352	GND	60
58	GND	260	IO260	IO353	353	GND	60
58	SPI_AP_TO_RACER_CS_L	261	IO261	IO354	354	GND	60
58	GND	262	IO262	IO355	355	GND	60
58	PMU_TO_IKTARA_RESET_L	263	IO263	IO356	356	GND	60
58	GND	264	IO264	IO357	357	GND	60
58	SWD_AOP_BI_RACER_SWDIO	265	IO265	IO358	358	GND	60
58	GND	266	IO266				
58	I2C3_AP_SDA	267	IO267				
58	GND	268	IO268				
58	I2C3_AP_SCL	269	IO269				
58	GND	270	IO270				
58	GND	271	IO271				
58	GND	272	IO272				
58	GND	273	IO273				
58	GND	274	IO274				
58	GND	275	IO275				
58	GND	276	IO276				
58	GND	277	IO277				
58	GND	278	IO278				
58	GND	279	IO279				
58	GND	280	IO280				
58	GND	281	IO281				

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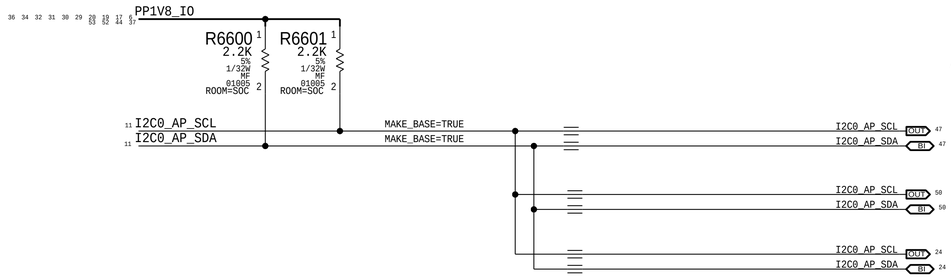
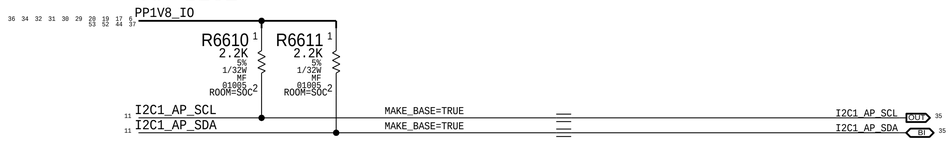
AP I2C

AP I2C0



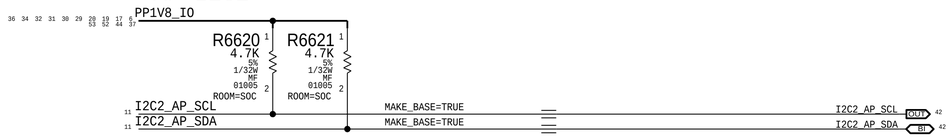
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C0	PP1V8_IO	400 kHz	GECKO	0x52	1010 010X	0xA4, 0xA5	-	1 MHz	TOP MLB
			SAKONNET	0x08	0001 000X	0x10, 0x11	-	1 MHz	Dock Flex
			BOOST	0x75	1110 101X	0xEA, 0xEB	-	400 KHz	TOP MLB
			ARC EEPROM	0x50	1010 000X	0xA0, 0xA1	-	400 KHz	Dock Flex

AP I2C1



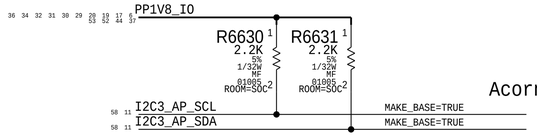
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C1	PP1V8_IO	100 kHz	MIC2	0x56	1010 100X	0xA8, 0xA9	-	1 MHz	Strobe Flex

AP I2C2



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C2	PP1V8_IO	1 MHz	Top Speaker Amp	0x40	1000 000X	0x80, 0x81	-	1 MHz	Top MLB

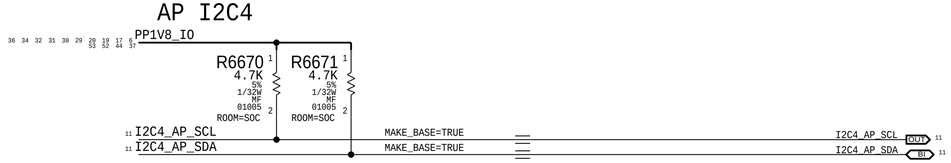
AP I2C3



Acorn and Touch EEPROM Live on Bottom Board

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C3	PP1V8_IO	400 kHz	ACORN	0X2A	0101 010X	0x54, 0x55	-	1 MHz	Bot MLB
			TOUCH EEPROM	0x51	1010 001X	0xA2, 0xA3	-	1 MHz	Touch Flex

AP I2C4



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Location
AP I2C4	PP1V8_IO	400 kHz	LYNX	0X71	Top MLB

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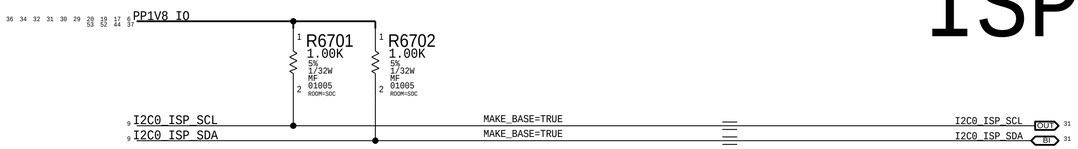
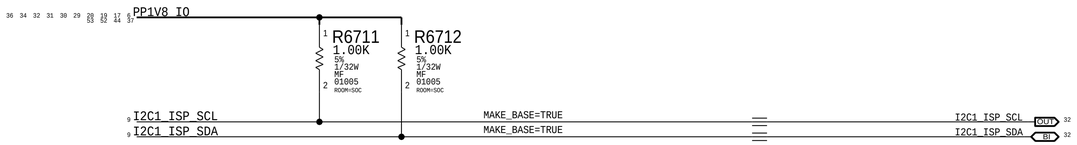
ISP I2C

ISP I2C0



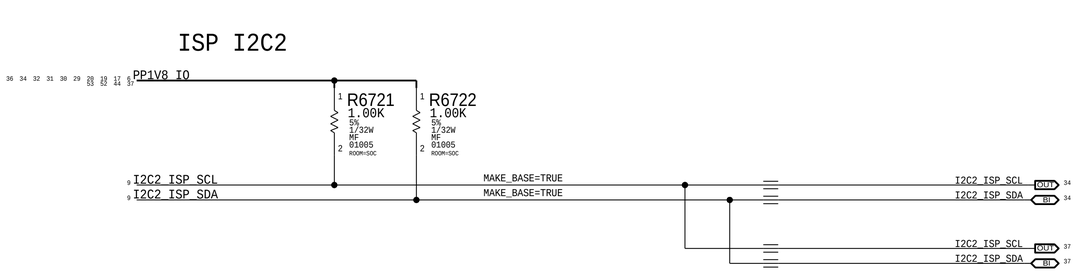
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
ISP I2C0	PP1V8_IO	1 MHz	Austin	0X10	0010 000X	0x20, 0x21	-	1 MHz	Wide Cam
			Raman	0X3C	0111 100X	0x78, 0x79	-	1 MHz	Wide Cam

ISP I2C1



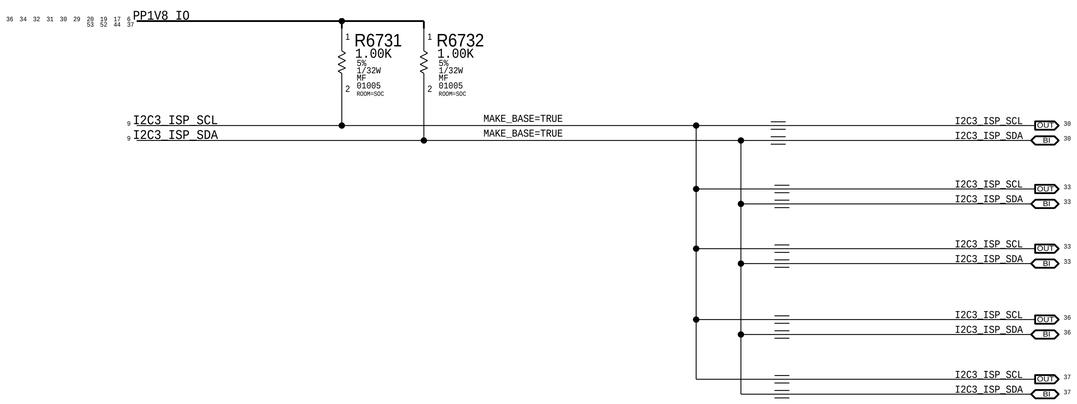
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
ISP I2C1	PP1V8_IO	1 MHz	Billings	0x20	0100 000X	0x40, 0x41	-	1 MHz	Tele Cam
			Grunberg+	0x1C	0011 100X	0x38, 0x39	-	1 MHz	Tele Cam

ISP I2C2



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
ISP I2C2	PP1V8_IO	1 MHz	Yonkers	0x10	0010 000X	0x20, 0x21	-	1 MHz	Fcam
			Flatiron	0x70	1110 000X	0xE0, 0xE1	-	1 MHz	Fcam
			Savage	0x18	0011 000X	0x30, 0x31	-	1 MHz	Juliet Flex

ISP I2C3



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
ISP I2C3	PP1V8_IO	1 MHz	Ansel	0x40	1000 000X	0x80, 0x81	-	1 MHz	Top Board
			Neon	0x63	1100 011X	0xC6, 0xC7	-	1 MHz	Top Board
			Neon	0x67	1100 111X	0xCE, 0xCF	-	1 MHz	Top Board
			Rigel	0x55	1100 011X	0xAA, 0xAB	-	1 MHz	Top Board
			Mama Bear	0x50	1010 000X	0xA0, 0xA1	-	1 MHz	Romeo Flex

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SYSTEM: ISP I2C

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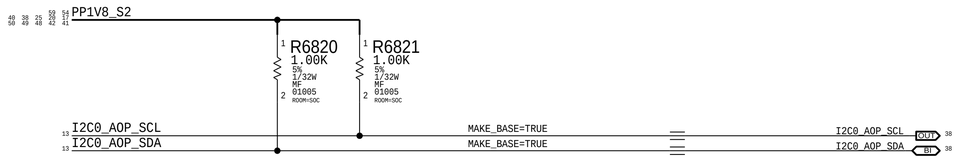
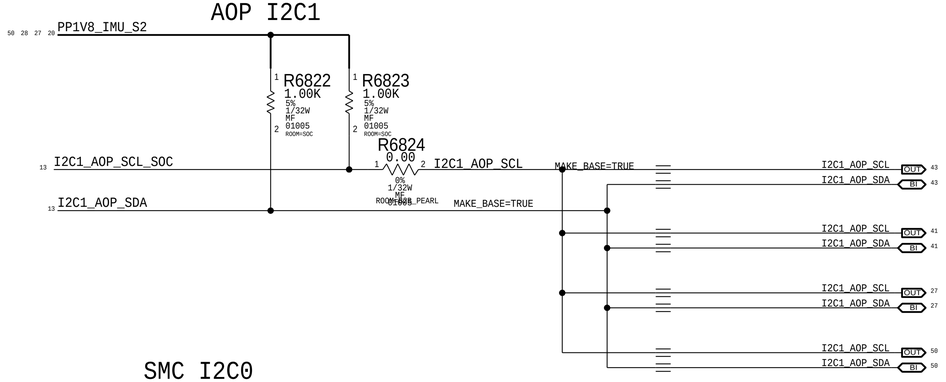
AOP/SMC I2C

AOP I2C0



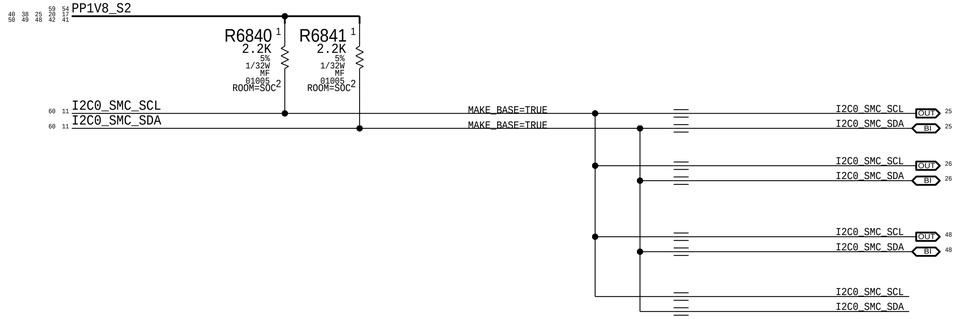
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AOP I2C0	PP1V8_S2	750 kHz	Doppler	0x58	1011 000X	0xB0, 0xB1	-	1 MHz	Sensor Flex
			Blackbird	0x29	0101 001X	0x52, 0x53	-	1 MHz	Sensor Flex
			Yogi	0x33	0110 011X	0x66, 0x67	-	1 MHz	Sensor Flex

AOP I2C1



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AOP I2C1	PP1V8_IMU_S2	400 kHz	Arc	0x42	1000 001X	0x82, 0x83	-	1 MHz	Top Board
			Bottom Speaker	0x40	1000 000X	0x80, 0x81	-	1 MHz	Top Board
			Moly	0x0E	0001 110X	0x1C, 0x1D	-	1 MHz	Button Cyclone
			Potassium	0x76	1110 110X	0xEC, 0xED	-	1 MHz	Dock Flex

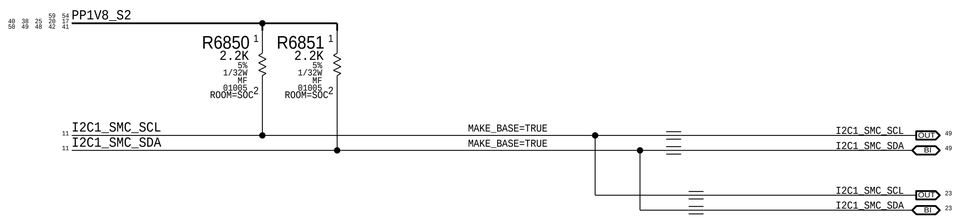
SMC I2C0



Lives on bottom board

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
SMC I2C0	PP1V8_S2	400 kHz	Yangtze	0x71	1110 001X	0xE2, 0xE3	-	400 KHz	Top Board
			Iktara	0x39	0111 001X	0x72, 0x73	-	400 KHz	Bot Board
			CCG2	0x12	0010 010X	0x24, 0x25	-	1 MHz	Top Board
			Gas Guage	0x55	0010 010X	0xAA, 0xAB	-	1 MHz	BMU Flex
			Roswell	0x10	0100 000X	0x20, 0x21	-	400 KHz	BMU Flex

SMC I2C1



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
SMC I2C1	PP1V8_S2	400 kHz	Hydra	0x1A	0011 010X	0x34, 0x35	-	400 KHz	Top Board
			Denali	0x74	1110 100X	0xE8, 0xE9	-	400 KHz	Top Board

AP/PMU GPIOs

SOC

GPIO_0	12	AP_TO_BT_DEVICE_WAKE	AP_TO_BT_DEVICE_WAKE	IN	58
GPIO_1	12	BOARD_REV0	BOARD_REV0	IN	6
GPIO_2	12	BOARD_REV1	BOARD_REV1	IN	6
GPIO_3	12	BOARD_REV2	BOARD_REV2	IN	6
GPIO_4	12	AP_TO_PMU_AMUX_SYNC	AP_TO_PMU_AMUX_SYNC	IN	23
GPIO_5	12	BOARD_REV3	BOARD_REV3	IN	6
GPIO_6	12	AP_CANARY1	AP_CANARY1	IN	60
GPIO_7	12	PMU_TO_AP_BUTTON_VOL_UP_L	PMU_TO_AP_BUTTON_VOL_UP_L	OUT	23
GPIO_8	12	NC_AP_GPIO8	NC_AP_GPIO8		
GPIO_9	12	AP_TO_BBPMU_RADIO_ON_L	AP_TO_BBPMU_RADIO_ON_L	OUT	57
GPIO_10	12	AP_TO_SPKRAMP_TOP_RESET_L	AP_TO_SPKRAMP_TOP_RESET_L	OUT	42
GPIO_11	12	AP_TO_NFC_FW_DWLD_REQ	AP_TO_NFC_FW_DWLD_REQ	IN	57
GPIO_12	12	AP_TO_BB_PEAK_POWER_INDICATOR	AP_TO_BB_PEAK_POWER_INDICATOR	OUT	57
GPIO_13	12	AP_TO_NFC_DEV_WAKE	AP_TO_NFC_DEV_WAKE	OUT	57
GPIO_14	12	CAMPMU_TO_AP_IRQ_L	CAMPMU_TO_AP_IRQ_L	IN	30
GPIO_15	12	AP_TO_GNSS_TIME_MARK	AP_TO_GNSS_TIME_MARK	OUT	57
GPIO_16	12	SPKRAMP_TOP_TO_AP_INT_L	SPKRAMP_TOP_TO_AP_INT_L	IN	42
GPIO_17	12	BB_TO_AP_COEX	BB_TO_AP_COEX	OUT	57
GPIO_18	12	BT_TO_AP_TIME_SYNC	BT_TO_AP_TIME_SYNC	IN	58
GPIO_19	12	AP_TO_BB_RESET_L	AP_TO_BB_RESET_L	OUT	57
GPIO_20	12	BB_TO_AP_PEAK_POWER_INDICATOR	BB_TO_AP_PEAK_POWER_INDICATOR	IN	57
GPIO_21	12	BB_TO_AP_RESET_DETECT_L	BB_TO_AP_RESET_DETECT_L	OUT	57
GPIO_22	12	AP_TO_BB_COREDUMP_TRIG	AP_TO_BB_COREDUMP_TRIG	IN	57
GPIO_23	12	AP_TO_CAMPMU_RESET_L	AP_TO_CAMPMU_RESET_L	OUT	30 57
GPIO_24	12	AP_TO_BB_COEX	AP_TO_BB_COEX	IN	57
GPIO_25	12	DISPLAY_TO_AP_PANEL_ID	DISPLAY_TO_AP_PANEL_ID	OUT	44
GPIO_26	12	AP_CANARY2	AP_CANARY2	OUT	58
GPIO_27	12	NC_AP_GPIO27	NC_AP_GPIO27		
GPIO_28	12	NC_AP_GPIO28	NC_AP_GPIO28		
GPIO_29	12	AP_TO_RACER_RESET_L	AP_TO_RACER_RESET_L	OUT	57
GPIO_30	12	GNSS_TO_AP_LOW_PWR_IND	GNSS_TO_AP_LOW_PWR_IND	IN	57

PMU

GPIO_1	23	PMU_TO_CCG2_RESET_L	PMU_TO_CCG2_RESET_L	OUT	48
GPIO_2	23	PMU_TO_AP_THROTTLE_GPU1_L	PMU_TO_AP_THROTTLE_GPU1_L	OUT	7
GPIO_3	23	NC_BT_TO_PMU_HOST_WAKE	NC_BT_TO_PMU_HOST_WAKE		
GPIO_4	23	WLAN_TO_PMU_HOST_WAKE	WLAN_TO_PMU_HOST_WAKE	IN	58
GPIO_5	23	BB_TO_PMU_PCIE_HOST_WAKE_L	BB_TO_PMU_PCIE_HOST_WAKE_L	IN	58
GPIO_6	23	PMU_NFC_TO_ARC_RESET_L	PMU_NFC_TO_ARC_RESET_L	OUT	43
GPIO_7	23	PMU_TO_GNSS_EN	PMU_TO_GNSS_EN	OUT	58
GPIO_8	23	PMU_TO_WLAN_CLK32K	PMU_TO_WLAN_CLK32K	OUT	23 58
GPIO_9	23	PMU_TO_BT_REG_ON	PMU_TO_BT_REG_ON	OUT	58
GPIO_10	23	PMU_TO_PHALANX2	PMU_TO_PHALANX2	IN	59
GPIO_11	23	YANGTZE_TO_PMU_INT_L	YANGTZE_TO_PMU_INT_L	IN	26
GPIO_12	23	CODEC_TO_PMU_WAKE_L	CODEC_TO_PMU_WAKE_L	IN	49
GPIO_13	23	PMU_MASK_NFC_TO_ARC_TRIG	PMU_MASK_NFC_TO_ARC_TRIG	OUT	43
GPIO_14	23	PMU_TO_WLAN_REG_ON	PMU_TO_WLAN_REG_ON	OUT	58
GPIO_15	23	PMU_TO_NFC_VDD_MAIN_EN	PMU_TO_NFC_VDD_MAIN_EN	OUT	57
IRQ GPIO_16	23	PMU_TO_NAND_LOW_BATT_BOOT_L	PMU_TO_NAND_LOW_BATT_BOOT_L	OUT	19
Held Through 1 Reset GPIO_17	23	PMU_TO_PHALANX1	PMU_TO_PHALANX1	IN	59
GPIO_18	23	PMU_TO_DISPLAY_RESET_L	PMU_TO_DISPLAY_RESET_L	OUT	44
GPIO_19	23	PMU_TO_BBPMU_RESET_R_L	PMU_TO_BBPMU_RESET_R_L		
GPIO_20	23	PMU_TO_NFC_EN	PMU_TO_NFC_EN	OUT	58
GPIO_21	23	NC_PMU_GPIO21	NC_PMU_GPIO21		
Sequenced GPIOs GPIO_22	23	PMU_TO_IKTARA_EN_EXT_1V8	PMU_TO_IKTARA_EN_EXT_1V8	OUT	60
GPIO_23	23	PMU_TO_BOOST_EN	PMU_TO_BOOST_EN	OUT	24
GPIO_24	23	PMU_TO_DISPLAY_PANICB	PMU_TO_DISPLAY_PANICB	OUT	44
GPIO_25	23	PMU_TO_DISPLAY_LDO_EN	PMU_TO_DISPLAY_LDO_EN	IN	44

GPIO16 is the only PIN capable of nIRQ

R3070
1.00K
5%
1/32W
MF
01005
ROOM=PMU

PMU_TO_BBPMU_RESET_L 58

SYNC_DATE=05/09/2017

PAGE TITLE
SYSTEM: SOC/PMU GPIOs

Apple Inc.

DRAWING NUMBER 051-02545
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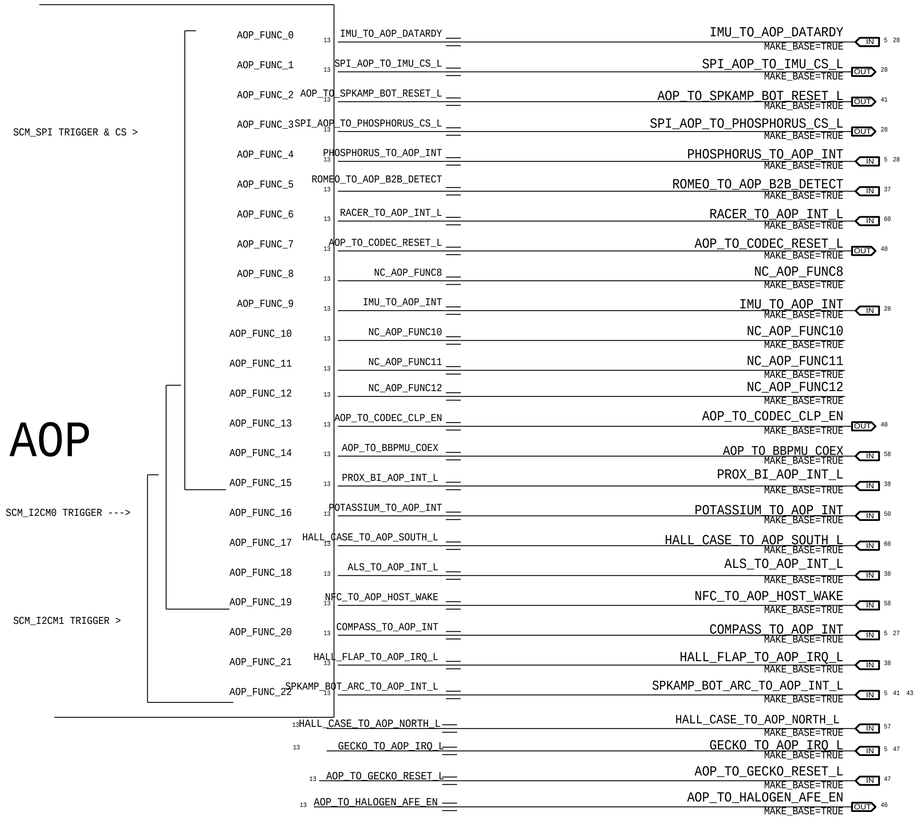
SHEET 55 OF 60

TDS_LTB=apple

A0P GPIOs



SYNC_DATE=05/09/2017

PAGE TITLE

SYSTEM: AOP GPIOs

Apple Inc.

DRAWING NUMBER 051-02545

SIZE D

REVISION 7.0.0

BRANCH

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CDS_LIB=apple

Interposer Aliases: Pins 1-144

THIS SIDE HAS ATTRIBUTE
MAKE_BASE=TRUE

Sheet	Net	Attribute	Alias net	Sheets
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	PMU_TO_SYSTEM_COLD_RESET_L	MAKE_BASE=TRUE	PMU_TO_SYSTEM_COLD_RESET_L	7 15 23
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	AP_TO_CAMPMU_RESET_L	MAKE_BASE=TRUE	AP_TO_CAMPMU_RESET_L	30 55
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	BB_TO_MANY_GSM_BURST_IND	MAKE_BASE=TRUE	BB_TO_MANY_GSM_BURST_IND	33 38
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	HALL_CASE_TO_AOP_NORTH_L	MAKE_BASE=TRUE	HALL_CASE_TO_AOP_NORTH_L	56
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	AP_TO_TOUCH_SCAN_CLK	MAKE_BASE=TRUE	AP_TO_TOUCH_SCAN_CLK	9
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	I2S_BB_TO_AP_BCLK	MAKE_BASE=TRUE	I2S_BB_TO_AP_BCLK	11
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	I2S_BB_TO_AP_DIN	MAKE_BASE=TRUE	I2S_BB_TO_AP_DIN	11
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	I2S_AP_TO_BB_DOUT	MAKE_BASE=TRUE	I2S_AP_TO_BB_DOUT	11
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	I2S_BB_TO_AP_LRCLK	MAKE_BASE=TRUE	I2S_BB_TO_AP_LRCLK	11
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	PP1V8_ALWAYS	MAKE_BASE=TRUE	PP1V8_ALWAYS	17 22 23 26
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59 60
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	NFC_TO_ARC_RESET_L	MAKE_BASE=TRUE	NFC_TO_ARC_RESET_L	5 43
51	GND	MAKE_BASE=TRUE	GND	57 59
51	NFC_TO_ARC_TRIG	MAKE_BASE=TRUE	NFC_TO_ARC_TRIG	5 43
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	59
51	AP_TO_BB_RESET_L	MAKE_BASE=TRUE	AP_TO_BB_RESET_L	55
51	GND	MAKE_BASE=TRUE	GND	57 59
51	SWD_AOP_BI_BB_SWDIO	MAKE_BASE=TRUE	SWD_AOP_BI_BB_SWDIO	13
51	GND	MAKE_BASE=TRUE	GND	57 59
51	UART_GNSS_TO_AP_CTS_L	MAKE_BASE=TRUE	UART_GNSS_TO_AP_CTS_L	12
51	GND	MAKE_BASE=TRUE	GND	57 59
51	UART_AP_TO_GNSS_RTS_L	MAKE_BASE=TRUE	UART_AP_TO_GNSS_RTS_L	12
51	GND	MAKE_BASE=TRUE	GND	57 59

THIS SIDE HAS ATTRIBUTE
MAKE_BASE=TRUE

Sheet	Net	Attribute	Alias net	Sheets
51	PCIE_AP_TO_WLAN_PERST_L	MAKE_BASE=TRUE	PCIE_AP_TO_WLAN_PERST_L	8
51	GND	MAKE_BASE=TRUE	GND	57 59
51	AP_TO_RACER_RESET_L	MAKE_BASE=TRUE	AP_TO_RACER_RESET_L	55
51	GND	MAKE_BASE=TRUE	GND	57 59
51	AP_TO_WLAN_TIME_SYNC	MAKE_BASE=TRUE	AP_TO_WLAN_TIME_SYNC	12
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GNSS_TO_AP_LOW_PWR_IND	MAKE_BASE=TRUE	GNSS_TO_AP_LOW_PWR_IND	55
51	GND	MAKE_BASE=TRUE	GND	57 59
51	HYDRA_TO_AP_FORCE_DFU	MAKE_BASE=TRUE	HYDRA_TO_AP_FORCE_DFU	12 49
51	GND	MAKE_BASE=TRUE	GND	57 59
51	PP1V8_S2	MAKE_BASE=TRUE	PP1V8_S2	59
51	PP1V8_S2	MAKE_BASE=TRUE	PP1V8_S2	59
51	GND	MAKE_BASE=TRUE	GND	57 59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	INTERPOSER_PIN_90		INTERPOSER_PIN_90	
51	GND	MAKE_BASE=TRUE	GND	59
51	AP_TO_BB_COEX	MAKE_BASE=TRUE	AP_TO_BB_COEX	55
51	BB_TO_AP_COEX	MAKE_BASE=TRUE	BB_TO_AP_COEX	55
51	GND	MAKE_BASE=TRUE	GND	59
51	AP_TO_NFC_DEV_WAKE	MAKE_BASE=TRUE	AP_TO_NFC_DEV_WAKE	55
51	AP_TO_NFC_FW_DWLD_REQ	MAKE_BASE=TRUE	AP_TO_NFC_FW_DWLD_REQ	55
51	GND	MAKE_BASE=TRUE	GND	59
51	PMU_TO_NFC_VDD_MAIN_EN	MAKE_BASE=TRUE	PMU_TO_NFC_VDD_MAIN_EN	55
51	UART_AOP_TO_BB_TXD	MAKE_BASE=TRUE	UART_AOP_TO_BB_TXD	13
51	UART_AP_TO_GNSS_TXD	MAKE_BASE=TRUE	UART_AP_TO_GNSS_TXD	12
51	GND	MAKE_BASE=TRUE	GND	59
51	AP_TO_BB_COREDUMP_TRIG	MAKE_BASE=TRUE	AP_TO_BB_COREDUMP_TRIG	55
51	UART_AP_TO_NFC_TXD	MAKE_BASE=TRUE	UART_AP_TO_NFC_TXD	12
51	UART_NFC_TO_AP_RXD	MAKE_BASE=TRUE	UART_NFC_TO_AP_RXD	12
51	BB_TO_AP_RESET_DETECT_L	MAKE_BASE=TRUE	BB_TO_AP_RESET_DETECT_L	55
51	GND	MAKE_BASE=TRUE	GND	59
51	BOARD_ID2	MAKE_BASE=TRUE	BOARD_ID2	6 12
51	AP_TO_GNSS_TIME_MARK	MAKE_BASE=TRUE	AP_TO_GNSS_TIME_MARK	55
51	NC_INTERPOSER_109	MAKE_BASE=TRUE	NC_INTERPOSER_109	
51	AP_TO_BB_PEAK_POWER_INDICATOR	MAKE_BASE=TRUE	AP_TO_BB_PEAK_POWER_INDICATOR	55
51	AP_TO_BBPMU_RADIO_ON_L	MAKE_BASE=TRUE	AP_TO_BBPMU_RADIO_ON_L	55
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	90_PCIE_BB_TO_AP_RXD_N	MAKE_BASE=TRUE	90_PCIE_BB_TO_AP_RXD_N	17
51	90_PCIE_BB_TO_AP_RXD_P	MAKE_BASE=TRUE	90_PCIE_BB_TO_AP_RXD_P	17
51	GND	MAKE_BASE=TRUE	GND	57 59
51	90_PCIE_AP_TO_BB_TXD_N	MAKE_BASE=TRUE	90_PCIE_AP_TO_BB_TXD_N	17
51	90_PCIE_AP_TO_BB_TXD_P	MAKE_BASE=TRUE	90_PCIE_AP_TO_BB_TXD_P	17
51	GND	MAKE_BASE=TRUE	GND	57 59
51	90_PCIE_AP_TO_BB_REFCLK_P	MAKE_BASE=TRUE	90_PCIE_AP_TO_BB_REFCLK_P	8
51	90_PCIE_AP_TO_BB_REFCLK_N	MAKE_BASE=TRUE	90_PCIE_AP_TO_BB_REFCLK_N	8
51	GND	MAKE_BASE=TRUE	GND	57 59
51	UART_BB_TO_AOP_RXD	MAKE_BASE=TRUE	UART_BB_TO_AOP_RXD	13
51	UART_GNSS_TO_AP_RXD	MAKE_BASE=TRUE	UART_GNSS_TO_AP_RXD	12
51	PCIE_AP_TO_BB_PERST_L	MAKE_BASE=TRUE	PCIE_AP_TO_BB_PERST_L	8
51	UART_NFC_TO_AP_CTS_L	MAKE_BASE=TRUE	UART_NFC_TO_AP_CTS_L	12
51	GND	MAKE_BASE=TRUE	GND	57 59
51	UART_AP_TO_NFC_RTS_L	MAKE_BASE=TRUE	UART_AP_TO_NFC_RTS_L	12
51	PMU_AMUX_BY	MAKE_BASE=TRUE	PMU_AMUX_BY	23
51	PMU_AMUX_AY	MAKE_BASE=TRUE	PMU_AMUX_AY	23
51	GND	MAKE_BASE=TRUE	GND	57 59
51	PCIE_BB_BI_AP_CLKREQ_L	MAKE_BASE=TRUE	PCIE_BB_BI_AP_CLKREQ_L	8
51	NC_INT_135	MAKE_BASE=TRUE	NC_INT_135	
51	BB_TO_AP_PEAK_POWER_INDICATOR	MAKE_BASE=TRUE	BB_TO_AP_PEAK_POWER_INDICATOR	55
51	GND	MAKE_BASE=TRUE	GND	57 59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59

Interposer Aliases: Pins 145-285

THIS SIDE HAS ATTRIBUTE
MAKE_BASE=TRUE

Ref	Net	Attribute	Alias	Refs
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 59 60
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN	59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PMU_TO_NFC_EN	MAKE_BASE=TRUE	PMU_TO_NFC_EN	55
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PMU_TO_BBPMU_RESET_L	MAKE_BASE=TRUE	PMU_TO_BBPMU_RESET_L	55
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PMU_TO_TOUCH_CLK32K	MAKE_BASE=TRUE	PMU_TO_TOUCH_CLK32K	17
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PCIE_WLAN_BI_AP_CLKREQ_L	MAKE_BASE=TRUE	PCIE_WLAN_BI_AP_CLKREQ_L	8
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	BB_TO_PMU_PCIE_HOST_WAKE_L	MAKE_BASE=TRUE	BB_TO_PMU_PCIE_HOST_WAKE_L	55
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	WLAN_TO_PMU_HOST_WAKE	MAKE_BASE=TRUE	WLAN_TO_PMU_HOST_WAKE	55
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	PMU_TO_WLAN_CLK32K	MAKE_BASE=TRUE	PMU_TO_WLAN_CLK32K	23 55
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	NFC_TO_AOP_HOST_WAKE	MAKE_BASE=TRUE	NFC_TO_AOP_HOST_WAKE	56
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	TOUCH_TO_MANY_FORCE_PWM	MAKE_BASE=TRUE	TOUCH_TO_MANY_FORCE_PWM	23 24 30
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	UART_AP_TO_BT_TXD	MAKE_BASE=TRUE	UART_AP_TO_BT_TXD	12
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	UART_AP_TO_BT_RTS_L	MAKE_BASE=TRUE	UART_AP_TO_BT_RTS_L	12
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	57 58 59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	AP_CANARY2	MAKE_BASE=TRUE	AP_CANARY2	55
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	PP1V8_NFC_S2	MAKE_BASE=TRUE	PP1V8_NFC_S2	20
51	PMU_TO_GNSS_EN	MAKE_BASE=TRUE	PMU_TO_GNSS_EN	55
51	PMU_TO_BT_REG_ON	MAKE_BASE=TRUE	PMU_TO_BT_REG_ON	55
51	GND	MAKE_BASE=TRUE	GND	58 59
51	90_PCIE_AP_TO_WLAN_REFCLK_N	MAKE_BASE=TRUE	90_PCIE_AP_TO_WLAN_REFCLK_N	8
51	90_PCIE_AP_TO_WLAN_REFCLK_P	MAKE_BASE=TRUE	90_PCIE_AP_TO_WLAN_REFCLK_P	8
51	GND	MAKE_BASE=TRUE	GND	58 59
51	90_PCIE_AP_TO_WLAN_TXD_P	MAKE_BASE=TRUE	90_PCIE_AP_TO_WLAN_TXD_P	17
51	90_PCIE_AP_TO_WLAN_TXD_N	MAKE_BASE=TRUE	90_PCIE_AP_TO_WLAN_TXD_N	17
51	GND	MAKE_BASE=TRUE	GND	58 59
51	90_PCIE_WLAN_TO_AP_RXD_N	MAKE_BASE=TRUE	90_PCIE_WLAN_TO_AP_RXD_N	17
51	90_PCIE_WLAN_TO_AP_RXD_P	MAKE_BASE=TRUE	90_PCIE_WLAN_TO_AP_RXD_P	17
51	GND	MAKE_BASE=TRUE	GND	58 59
51	PP3V0_S2	MAKE_BASE=TRUE	PP3V0_S2	22 38 48 49
51	PP1V8_TOUCH_RACER_S2	MAKE_BASE=TRUE	PP1V8_TOUCH_RACER_S2	59
51	PP1V8_TOUCH_RACER_S2	MAKE_BASE=TRUE	PP1V8_TOUCH_RACER_S2	59
51	PMU_TO_WLAN_REG_ON	MAKE_BASE=TRUE	PMU_TO_WLAN_REG_ON	55
51	RADIO_PA_NTC	MAKE_BASE=TRUE	RADIO_PA_NTC	23
51	BT_TO_AP_TIME_SYNC	MAKE_BASE=TRUE	BT_TO_AP_TIME_SYNC	55
51	UART_BT_TO_AP_RXD	MAKE_BASE=TRUE	UART_BT_TO_AP_RXD	12

THIS SIDE HAS ATTRIBUTE
MAKE_BASE=TRUE

Ref	Net	Attribute	Alias	Refs
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	UART_BT_TO_AP_CTS_L	MAKE_BASE=TRUE	UART_BT_TO_AP_CTS_L	12
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	59
51	GND	MAKE_BASE=TRUE	GND	59
51	PP_VBUS1_E75	MAKE_BASE=TRUE	PP_VBUS1_E75	26 50
51	GND	MAKE_BASE=TRUE	GND	58 59
51	PP_GPU_LVCC	MAKE_BASE=TRUE	PP_GPU_LVCC	5
51	GND	MAKE_BASE=TRUE	GND	58 59
51	PP_CPU_PCORE_LVCC	MAKE_BASE=TRUE	PP_CPU_PCORE_LVCC	5
51	GND	MAKE_BASE=TRUE	GND	58 59
51	PP_BATT_VCC	MAKE_BASE=TRUE	PP_BATT_VCC	59
51	PP_BATT_VCC	MAKE_BASE=TRUE	PP_BATT_VCC	59
51	GND	MAKE_BASE=TRUE	GND	59
51	AP_TO_BT_DEVICE_WAKE	MAKE_BASE=TRUE	AP_TO_BT_DEVICE_WAKE	55
51	AOP_TO_WLAN_CONTEXT_A	MAKE_BASE=TRUE	AOP_TO_WLAN_CONTEXT_A	13
51	UART_AOP_TO_RACER_TXD	MAKE_BASE=TRUE	UART_AOP_TO_RACER_TXD	13
51	SWD_AOP_TO_MANY_SWCLK	MAKE_BASE=TRUE	SWD_AOP_TO_MANY_SWCLK	5 13 19
51	SPI_AP_TO_RACER_MOSI	MAKE_BASE=TRUE	SPI_AP_TO_RACER_MOSI	11
51	SPI_AP_TO_RACER_SCLK	MAKE_BASE=TRUE	SPI_AP_TO_RACER_SCLK	11
51	PP1V1_RACER_S2	MAKE_BASE=TRUE	PP1V1_RACER_S2	59
51	PP1V1_RACER_S2	MAKE_BASE=TRUE	PP1V1_RACER_S2	59
51	PP1V1_RACER_S2	MAKE_BASE=TRUE	PP1V1_RACER_S2	59
51	AP_TO_RACER_REF_CLK	MAKE_BASE=TRUE	AP_TO_RACER_REF_CLK	17
51	GND	MAKE_BASE=TRUE	GND	59
51	AOP_TO_BBPMU_COEX	MAKE_BASE=TRUE	AOP_TO_BBPMU_COEX	56
51	PP_VBUS2_IKTARA	MAKE_BASE=TRUE	PP_VBUS2_IKTARA	59
51	PP_VBUS2_IKTARA	MAKE_BASE=TRUE	PP_VBUS2_IKTARA	59
51	PP_VBUS2_IKTARA	MAKE_BASE=TRUE	PP_VBUS2_IKTARA	59
51	PP_VBUS2_IKTARA	MAKE_BASE=TRUE	PP_VBUS2_IKTARA	59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	AOP_TO_WLAN_CONTEXT_B	MAKE_BASE=TRUE	AOP_TO_WLAN_CONTEXT_B	13
51	GND	MAKE_BASE=TRUE	GND	58 59
51	UART_RACER_TO_AOP_RXD	MAKE_BASE=TRUE	UART_RACER_TO_AOP_RXD	13
51	GND	MAKE_BASE=TRUE	GND	58 59
51	SPI_RACER_TO_AP_MISO	MAKE_BASE=TRUE	SPI_RACER_TO_AP_MISO	11
51	GND	MAKE_BASE=TRUE	GND	58 59
51	SPI_AP_TO_RACER_CS_L	MAKE_BASE=TRUE	SPI_AP_TO_RACER_CS_L	11
51	GND	MAKE_BASE=TRUE	GND	58 59
51	PMU_TO_IKTARA_RESET_L	MAKE_BASE=TRUE	PMU_TO_IKTARA_RESET_L	23 45
51	GND	MAKE_BASE=TRUE	GND	58 59
51	SWD_AOP_BI_RACER_SWDIO	MAKE_BASE=TRUE	SWD_AOP_BI_RACER_SWDIO	13
51	GND	MAKE_BASE=TRUE	GND	58 59
51	I2C3_AP_SDA	MAKE_BASE=TRUE	I2C3_AP_SDA	CKPLUS_WAIVE=I2C_PULLUP 11 52
51	GND	MAKE_BASE=TRUE	GND	58 59
51	I2C3_AP_SCL	MAKE_BASE=TRUE	I2C3_AP_SCL	CKPLUS_WAIVE=I2C_PULLUP 11 52
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
51	GND	MAKE_BASE=TRUE	GND	58 59
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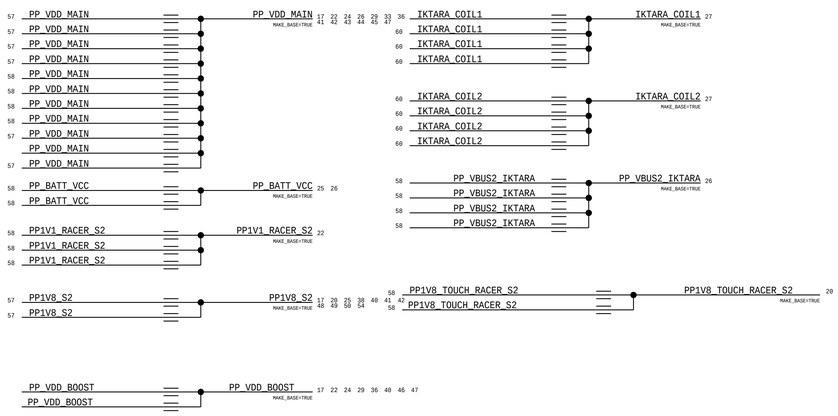
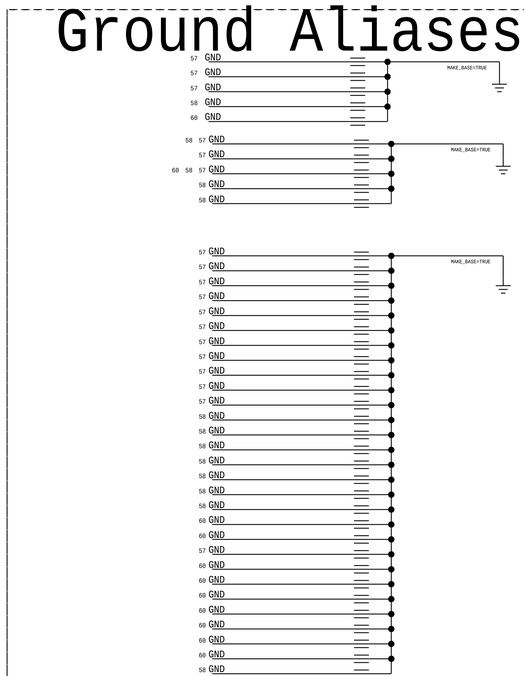
Interposer Top Level Aliases

Power Aliases



Ground Aliases



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