1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D53 Bottom MLB

EVT

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0022732381	ENGINEERING RELEASED	2020-03-28

LAST_MODIFICATION=Fri Mar 27 22:25:46 2020

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3	3	CONSTRAINTS: Impedance Controlled		
4	4	CONSTRAINTS: Power		
5	5	CONSTRAINTS: Misc.		
6	6	CONSTRAINTS: Stackup/Misc. (FF-Specific)		
7	50	SYS PWR: NTCs (Bottom)	D52_AP_MASTER_3.47.0	
8	63	CAMERA: Actuator Supply (Lex)	D52_AP_MASTER_3.47.0	
9	65	CAMERA: Strobe Driver	D52_AP_MASTER_3.47.0	
10	73	SENSORS: Accel / Gyro	D52_AP_MASTER_3.47.0	
11	75	SENSORS: Jarvis (Bottom)	D52_AP_MASTER_3.47.0	
12	122	B2B: LAT		
13	125	MECHANICAL: Standoffs, Shields, etc.		
14	128	TESTING: Probe Points		
15	130	INTERPOSER: Symbol (1/2)		
16	131	INTERPOSER: Symbol (2/2)		
17	132	INTERPOSER: Aliases (1/4)	D53_MLB_TOP_3.39.1	
18	133	INTERPOSER: Aliases (2/4)	D53_MLB_TOP_3.39.1	
19	134	INTERPOSER: Aliases (3/4)	D53_MLB_TOP_3.39.1	
20	135	INTERPOSER: Aliases (4/4)	D53_MLB_TOP_3.39.1	
21	136	INTERPOSER: Misc. Aliases		
22	150	HIER: WiFi		
23	160	HIER: Radio		
24	1	FRONT PAGE		
25	2	BOMS AND CONSTRAINTS		07/30/2019
26	4	PMIC: BUCKs		07/30/2019
27	5	PMIC: LDOs		07/30/2019
28	6	PMIC: CLOCKS & CONTROL		07/30/2019
29	7	BB: POWER		08/22/2019
30	8	BB: GND		07/30/2019
31	9	BB: GPIOS & QLINK		07/30/2019
32	11	XCVR POWER_1		07/30/2019
33	12	XCVR POWER_2		07/30/2019
34	13	XCVR DIGITAL & GND		07/30/2019
35	14	XCVR RF		07/30/2019
36	16	QET_DISCRETE_0		07/30/2019
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LAST_MODIFICATION=Fri Mar 27 22:25:46 2020

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41	25	LB DSM		07/30/2019
42	26	HB TXDSM		07/30/2019
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44	28	MIMO DSM LOWER		07/30/2019
45	29	MIMO DSM UPPER		07/30/2019
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50	35	LOWER ANTENNA FEEDS_ANT3		07/30/2019
51	37	LOWER ANTENNA FEEDS_ANT8		07/30/2019
52	38	LOWER ANTENNA FEEDS_ANT9		07/30/2019
53	41	PSIM		07/30/2019
54	43	UAT SAWTOOTH		07/30/2019
55	44	LAT SAWTOOTH		07/30/2019
56	46	DEBUG & TEST POINTS		07/30/2019
57	53	SYNONYMS		07/30/2019
58	57	MLB_ADJUSTABLES		07/30/2019
59	58	MMW		07/30/2019
60	59	TANGIER SIP		07/30/2019
61	60	BG1 ARRAY		07/30/2019
62	1	Table of Contents		
63	2	THELONIOUS	D52_WIFI_MASTER_0.21.0	
64	5	5G rFEM (LAT)	D52_WIFI_MASTER_0.21.0	

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE for 639-08663	MVVQ	CRITICAL	EEEE:08663
825-7691	1	EEEE for 639-10094	NY13	CRITICAL	EEEE:10094
825-7691	1	EEEE for 639-10104	NY61	CRITICAL	EEEE:10104

APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05262	1	SCH,MLB,BOT,MAV,D53	SCH	CRITICAL	?
820-01970	1	PCB,MLB,BOT,MAV,D53	PCB	CRITICAL	?

Sub-designs

Hierarchies

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/ SOFT	SYNC_DATE/TIME	FORCE SUBDESIGN
D53	HIER_RADIO_MAV_BOT	2.74.0	S	2020_03_26_20:22:01	N
D53	HIER_WIFI_BOT	0.15.0	S	2020_03_13_12:08:25	N

Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	AP_MASTER	2,50,63,65,73,75	3.47.0	S	2020_03_26_20:18:18
D53	MLB_TOP	132-135	3.39.1	S	2020_03_26_20:21:09

Packaging Options

PACK_OPTIONS TO INCLUDE IN NETLIST
D53

TABLE OF CONTENTS

DRAWING TITLE: SCH,MLB,BOT,MAV,D53

DRAWING NUMBER: 051-05262 | SIZE: D

REVISION: 6.0.0

BRANCH: evt-0

PAGE: 1 OF191

SHEET:

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Multi-Vendor Criticals

Capacitors

In descending order of value, then package size

CRITICAL PART#	COMMENT
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
132S0663	CAP,CER,X5R,1UF,10%,25V,0402
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
132S00008	CAP,CER,0.1UF,10%,50V,X7R,0402
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S0664	CAP,CER,0.047UF,10%,25V,X5R,0201
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S00093	CAP,X5R,0.022UF,20%,6.3V,01005
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S0396	CAP,CER,X5R,1000PF,10%,10V,01005
132S0296	CAP,CER,X5R,1000PF,10%,6.3V,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
131S0883	CAP,CER,NP0/C0G,220PF,2%,50V,0201
131S00170	CAP,CER,C0G,220PF,5%,25V,01005
131S00053	CAP,CER,C0G,220PF,5%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
131S0307	CAP,CER,NP0/C0G,100PF,5%,16V,01005

Capacitors (cont'd)

CRITICAL PART#	COMMENT
131S00303	CAP,CER,NPO/C0G,100PF,5%,16V,01005
131S00323	CAP,CER,NPO/C0G,56PF,5%,25V,01005
131S0643	CAP,CER,NP0/C0G,56PF,5%,25V,01005
131S0216	CAP,CER,NP0/C0G,47PF,5%,16V,01005
131S0804	CAP,CER,27PF,5%,C0G,25V,0201
131S0223	CAP,CER,NP0/C0G,27PF,5%,16V,01005
131S0215	CAP,CER,NPO/C0G,22PF,5%,16V,01005
131S0225	CAP,CER,NP0/C0G,15PF,5%,16V,01005
131S0220	CAP,CER,NP0/C0G,12PF,5%,16V,01005
131S00353	CAP,CER,NPO/C0G,10PF,5%,16V,01005

Ferrites

CRITICAL PART#	COMMENT
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605

Resistors

CRITICAL PART#	COMMENT
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
117S0055	RES,MF,1/20W,2M OHM,5,0201,SMD

Misc.

CRITICAL PART#	COMMENT
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005

2020 MLCCs

16uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00316	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402	Primary: Murata
138S00314	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402	Taiyo
138S00315	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402	Kyocera
					Samsung

11uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00318	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T	Primary: Murata
138S00319	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T	Kyocera
138S00320	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T	Samsung
					Taiyo

2.7uF, 0201, 6.3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00326	138S00325	?	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201	Primary: Murata
138S00327	138S00325	?	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201	Kyocera
					Samsung

2.7uF, 0201, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00324	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201	Primary: Murata
138S00322	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201	Taiyo
138S00323	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201	Kyocera
					Samsung

MAV20 PDN Single-source

0.22uF, 01005

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Kyocera

(C700,E-C710,E-C711,E-C712,E-C717,E-C730,E-C731,E-C732,E-C733,E-C742,E-C744,E-C745,E-C746,E-C747,E-C778,E-C779,E-C780,E)
(C700,E-C710,E-C711,E-C712,E-C717,E-C730,E-C731,E-C732,E-C733,E-C742,E-C744,E-C745,E-C746,E-C747,E-C778,E-C779,E-C780,E)

2.2uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	[SEE BELOW]	CAP,CER,X5R,2.2UF,20%,6.3V,0201

(C700,E-C702,E-C704,E-C711,E-C712,E-C720,E-C725,E-C732,E-C733,E-C742,E-C744,E-C747,E-C748,E-C749,E-C757,E-C760,E-C762,E-C764,E-C765,E-C766,E-C767,E-C768,E-C772,E-C773,E-C778,E)

4uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C511,E-C518,E-C522,E-C524,E-C526,E-C702,E-C704,E-C708,E-C709,E-C777,E-C787,E-C788,E-C1138,E-C1142,E-C1226,E-C1227,E-C5001,E-C5003,E-C5023,E-C5027,E-C5028,E)
(C511,E-C518,E-C522,E-C524,E-C526,E-C702,E-C704,E-C708,E-C709,E-C777,E-C787,E-C788,E-C1138,E-C1142,E-C1226,E-C1227,E-C5001,E-C5003,E-C5023,E-C5027,E-C5028,E)

Capacitor Alternates

0.1uF, 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	?	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005

CRITICAL PART#	COMMENT
132S0316	01005,0.1uF, 6.3V

0.22uF, 01005

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?		01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?		01005,0.22uF,6.3V,Kyocera

CRITICAL PART#	COMMENT
132S00014	01005,0.22uF, 6.3V

0.47uF, 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00133	138S00128	?	ALL	01005,0.47uF,6.3V,Murata
138S00269	138S00128	?	ALL	01005,0.47uF,6.3V,Taiyo

CRITICAL PART#	COMMENT
138S00128	01005,0.47uF, 6.3V

1uF, 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA

CRITICAL PART#	COMMENT
138S0706	CAP,X5R,1UF,20%,10V,0201

2.2uF, 0201

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?		CAP,CER,X5R,2.2UF,20%,6.3V,0201

CRITICAL PART#	COMMENT
138S0831	CAP,CER,X5R,2.2UF,20%,6.3V,0201

3uF @ 1V, 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	?	ALL	0201,3uF@1V,KYOCERA
138S00164	138S00139	?	ALL	0201,3uF@1V,TAIYO
138S00280	138S00139	?	ALL	0201,3uF@1V,SAMSUNG

CRITICAL PART#	COMMENT
138S00139	0201,3uF@1V

4uF, 0201

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?		CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?		CAP,X5R,4UF,0201,0.55MM,KYOCERA

CRITICAL PART#	COMMENT
138S00071	0201,X5R,4UF,0201,0.55MM,MURATA

4.7uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1103	138S0719	?	ALL	CAP,CER,X5R,4.7UF,20%,10V,0402

CRITICAL PART#	COMMENT
138S0719	0402,4.7uF,10V

15uF, 0402

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?		0402,15uF,6.3V, Kyocera

(C1805,C3321,C1872,C3371,C3382)

CRITICAL PART#	COMMENT
138S00003	0402,15uF,6.3V

18uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00221	138S00146	?	ALL	CAP,CER,X5R,18UF,20%,6.3V,MUR,0402

CRITICAL PART#	COMMENT
138S00146	CAP,CER,X5R,18UF,20%,6.3V,MUR,0402

20uF, 0402

All parts are single-sourced except for approved parts (listed below)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00339	138S0884	?		Taiyo
138S00338	138S0884	?		Kyocera

C3302,C3312,C3333,C3350,C3364,C1893,C3412,C3423,C3525,C3535,C3403,C1807,C1866,C1874,C2030
C3302,C3312,C3333,C3350,C3364,C1893,C3412,C3423,C3525,C3535,C3403,C1807,C1866,C1874,C2030

CRITICAL PART#	COMMENT
138S0884	CAP,CER,X5R,20UF,20%,6.3V,0402,H=0.7MM

22uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	?	ALL	CAP,X5R,26UF,20%,4V,MURATA,0402
138S00143	138S00279	?	ALL	CAP,X5R,22UF,20%,4V,KYOCERA,0402

CRITICAL PART#	COMMENT
138S00279	CAP,X5R,26UF,20%,4V,MURATA,0402

10uF @ 1V, 4-Term

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00148	138S00149	?	ALL	0402-3T,10.5uF@1V, Kyocera
138S00150	138S00149	?	ALL	0402-3T,10.5uF@1V, SEMCO
138S00151	138S00149	?	ALL	0402-3T,10.5UF@1V, TY

CRITICAL PART#	COMMENT
138S00149	0402-3T,10.5uF@1V

22uF, 0402 3T (WiFi)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00024	138S0986	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
138S0986	CAP,CER,3-TERM,7.5UF,20%,4V,0402

Display Choke Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00415	155S00524	?	ALL	FLTR,NOISE,35 OHMZ,3 OHM,7GHZ,50MA,0403

CRITICAL PART#	COMMENT
155S00524	FLTR,NOISE,35 OHMZ,3 OHM,7GHZ,50MA,0403

Level Shifter Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S00231	311S00232	?	ALL	IC,74AVC2T45,XCVR,2 BIT,2 SPLY,X2SON8
311S00230	311S00212	?	ALL	IC,74AVC1T45,XCVR,1 BIT,2 SPLY,X2SON6
311S00261	311S00233	?	ALL	IC,LSF0101,XCVR,2 BIT CFG,2 SPLY,X2SON6

CRITICAL PART#	COMMENT
311S00232	IC,74AVC2T45,XCVR,2 BIT,2 SPLY,X2SON8
311S00212	IC,74AVC1T45,XCVR,1 BIT,2 SPLY,X2SON6
311S00233	IC,LSF0101,XCVR,2 BIT CFG,2 SPLY,X2SON6
311S00235	IC,NVT0202,XCVR,2 BIT, 2 SPLY,BIDI,DFN8

Power Inductor Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00721	152S00876	?	ALL	Taiyo,IND,MLD,1UH,3.6A,60MΩ,2016
152S00930	152S00897	?	ALL	Cyntec,IND,CPL/D,0.33M,0.1A,27MΩ,2016
152S00826	152S00821	?	ALL	Taiyo,IND,MLD,1UH,2.3A,68MΩ,2012
152S00831	152S00818	?	ALL	Taiyo,IND,MLD,0.22UH,3.3A,49MΩ,1608
152S00991	152S00984	?	ALL	Taiyo,IND,MLD,0.47UH,3.5A,34MΩ,1614
152S00992	152S00985	?	ALL	Taiyo,IND,MLD,0.47UH,4.0A,45MΩ,2012
152S00989	152S00982	?	ALL	Taiyo,IND,MULT,0.47UH,2.8A,79MΩ,1608
152S00824	152S00819	?	ALL	Taiyo,IND,MLD,1UH,20%,3A,69MΩ,H=0.65,2012
152S00872	152S00918	?	ALL	TDK,IND,MLD,0.47UH,5.6A,30MΩ,H=0.8,2016
152S00847	152S00918	?	ALL	CYNTEC,IND,MLD,0.47UH,5.6A,19MΩ,H=0.8,3010
152S01282	152S01255	?	ALL	TAIYO,IND,MLD,0.47UH,5A,38MΩ,H=0.65,2117

CRITICAL PART#	COMMENT
152S00876	Cyntec,IND
152S00897	Taiyo,IND
152S00821	Cyntec,IND
152S00818	Cyntec,IND
152S00984	Cyntec.IND
152S00985	Cyntec,IND
152S00982	Cyntec,IND
152S00819	Cyntec,IND

Boost/Yeti (2117/0.8mm)

Boost/Yeti (2117/0.65mm)

Misc. Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00437	155S00402	?	ALL	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00194	155S00400	?	ALL	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
155S00414	155S0876	?	ALL	FERR BD,190HM,50%,1.1A,0.05OHM DCR,01005
155S00131	155S0755	?	ALL	FERR BD,2400HM,25%,200MA,1.0OHM DCR,01005
155S00583	155S00140	?	ALL	FERR BD,330HM,25%,400MA,0.20DCR,01005
377S00070	377S00001	?	ALL	TVS,BIDIR,5.8V,6PF,01005
377S00140	377S00001	?	ALL	TVS,BIDIR,5V,6PF,01005
377S0168	377S00129	?	ALL	SUPPRESS,TRANS,6.8V,100PF,AMOTECH,01005
107S0245	107S0244	?	ALL	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

CRITICAL PART#	COMMENT
155S00402	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00400	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
155S0876	FERR BD,190HM,50%,1.1A,0.05OHM DCR,01005
155S0755	FERR BD,240 OHM,25%,200MA,1.0 DCR,01005
155S00140	FERR BD,330HM,25%,400MA,0.20DCR,01005
377S00001	TVS,BIDIR,5.8V,6PF,01005
377S00129	SUPRESS,TRANS,6.8V,100PF,01005
107S0244	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

ZRB Cap ALTs

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00240	138S00187	?	ALL	CAP,X5R,4.7UF,20%,25V,0402
138S00246	138S00185	?	ALL	CAP,X5R,2.2UF,20%,25V,0402

CRITICAL PART#	COMMENT
138S00175	CAP,X5R,4.7UF,20%,25V,0402
138S00185	CAP,X5R,2.2UF,20%,25V,0402

0-ohm, 0201, 4.5A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
117S00040	117S00012	?	ALL	RES,MF,0 OHM,1/10W,4.5A,0201

CRITICAL PART#	COMMENT
117S00012	RES,MF,0 OHM,1/10W,4.5A,0201

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PAGE TITLE: SYSTEM: BOM Tables

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Spacing CSet Definitions

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from min-trace- spacing+distance in even units(1,*) for etch/via	EXAMPLE: 1,3,5,7,9,.../8,16,... 1.5,2,3,4
A_DIELECTRIC_(N)XD.XV,XVL,X Calculates dielectric distance from <value> table and adds <value> for etch/via (1,*) or etch/via	EXAMPLE: 2.125,.82,50.75,.85,.375 PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from min-trace- spacing+distance in even units(1,*) for etch/via	EXAMPLE: 2,.4,.5,.75 ?

90-ohm Diff Pair Constraints

Electrical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
QLINK (RF)	E_QLINK_SUB6	E	DIFF_PAIR_QLINK-SUB6	DP:DP_85_SUB6_QLINK_*	?
	E_QLINK_MMW	E	DIFF_PAIR_QLINK-MMW	DP:DP_85_MMW_QLINK_*	?
PCIe	E_PCIE_BB	E	DIFF_PAIR	DP:DP_90_PCIE_GP2_AP_*_BB_*	?
	E_PCIE_WLAN	E	DIFF_PAIR	DP:DP_90_PCIE_GP1_AP_*_WLAN_*	?
USB	E_USB_BB	E	DIFF_PAIR	DP:DP_90_USB_BB	?

Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
85-ohm	85_QLINK_SUB6	P	A_85_OHM_DIFF	DP:DP_85_SUB6_QLINK_*	?
	85_QLINK_MMW	P	A_85_OHM_DIFF	DP:DP_85_MMW_QLINK_*	?
	90_PCIE_BB	P	A_90_OHM_DIFF	DP:DP_90_PCIE_GP2_AP_*_BB_*	?
90-ohm	90_PCIE_WLAN	P	A_90_OHM_DIFF	DP:DP_90_PCIE_GP1_AP_*_WLAN_*	?
	90_USB_BB	P	A_90_OHM_DIFF	DP:DP_90_USB_BB	?

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
85-ohm	85_QLINK_SUB6	S	NA_DIELECTRIC_3X	=	?
	85_QLINK_MMW	S	NA_DIELECTRIC_3X	=	?
	90_PCIE_BB	S	NA_DIELECTRIC_3X	=	?
90-ohm	90_PCIE_WLAN	S	NA_DIELECTRIC_3X	=	?
	90_USB_BB	S	NA_DIELECTRIC_3X	=	?

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
90_PCIE_BB	GND	A_DIELECTRIC_2X
90_PCIE_WLAN	GND	A_DIELECTRIC_2X

50-ohm (Wide) Constraints

Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT1*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT3_MB_HB_WLAN24*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT7*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT8*	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_ANT9_UHB_N79	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB_M	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_CPLR_U_*, 50_TRX_CPL_U_*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HBDSM_HB_ANT1*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HB_PAD_ANT1	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HB_PAD_MIMO1_RX_OUT_M	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LBDSM_*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PAD_ANT1	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_TX	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_TX_M	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT2_TO_ANT9*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBU_N79_ANT2_TO_ANT8*	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_TPLX_*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_*	?
GNSS	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_L1_LNA_IN_M	?
	50_TRX_HYBRID2	P	A_50_WIDE-L1-L6_THIN-L3_SE	50_TRX_WLAN_G_BT_ANT3	?
WiFi	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_WLAN_G_BT_ANT3_M	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_WLAN_A_C1_TXRX	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_WLAN_A_C1_TXRX_BPF*	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_WLAN_A_C1_TXRX_FEM_M	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_A_LAA_ANT5*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_A_LAA_BPF	?
	50_TRX_UHB_PAD	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_UHB_PAD_*	?
UHB PAD	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_HBDSM_HB_ANT2*	?
Hybrids	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_HBDSM_MIMO2_RX_OUT*	?
	50_TRX_HYBRID	P	A_50_WIDE-L6_THIN-L1-L3_SE	50_TRX_LMB_HB_PORTB_RX1*	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HB_PAD_ANT1_M	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_DPLX_LB_LMB_MB_HB_ANT1	?
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PAD_ANT1_M	?

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Everything	50_TRX_WIDE	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	?
	50_TRX_UHB_PAD	S	NA_DIELECTRIC_4XV_50_WIDE-L6_THIN-L1-L3_SE	=	?
	50_TRX_HYBRID	S	NA_DIELECTRIC_4XV_50_WIDE-L6_THIN-L1-L3_SE	=	?
	50_TRX_HYBRID2	S	NA_DIELECTRIC_4XV_50_WIDE-L1-L6_THIN-L3_SE	=	?

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_TRX_WIDE	GND	NA_DIELECTRIC_2X_50_WIDE_SE
50_TRX_HYBRID	GND	NA_DIELECTRIC_2X_50_WIDE-L6_THIN-L1-L3_SE
50_TRX_HYBRID2	GND	NA_DIELECTRIC_2X_50_WIDE-L1-L6_THIN-L3_SE
50_TRX_UHB_PAD	GND	NA_DIELECTRIC_2X_50_WIDE-L6_THIN-L1-L3_SE
UHB PAD	50_TRX_UHB_PAD	NA_DIELECTRIC_4X

50-ohm (Thin) Constraints

Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	50_TX0_THIN	P	A_50_THIN_SE	50_TX_IN_*TX0_*	?
	50_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_*TX1_*	?
	50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_*TX2_*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_HBDSM_RXOUT_DRX*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_HB_PAD_PRX_OUT*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LAA_XCVR_*RX*, 50_LAA_RX_XCVR_*RX*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LBDSM_RXOUT*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_MIMO*_RXOUT_DRX*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM*RX_OUT*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_XCVR_DRX*	?
	50_RX_THIN	P	A_50_THIN_SE	50_RX_XCVR_PRX*	?
GNSS	50_THIN	P	A_50_THIN_SE	50_RX_GNSS_L*	?
	50_TRX_THIN	P	A_50_THIN_SE	50_L*_LNA_NOTCH*	?
	50_THIN	P	A_50_THIN_SE	50_RX_L1_LNA_OUT	?
	50_THIN	P	A_50_THIN_SE	50_RX_L5_LNA_OUT	?
WiFi	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_C0*	?
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_G_C0*	?
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_G_C1*	?
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_LAT_TXRX_FEM	?
Misc.	50_TRX_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_FBRX_1	?
	50_TRX_THIN	P	A_50_THIN_SE	50_CPLR_L_CPL1_LAT_OUT	?
	50_TRX_THIN	P	A_50_THIN_SE	50_UHB_L_CPLR_OUT	?
	50_TRX_THIN	P	A_50_THIN_SE	50_CPLR_U_CPL1_UHB_OUT	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LB_LMB_MB_HB	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_L5_LNA_IN	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_ANT3_L5	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_DPLX*, !50_TRX_DPLX_LB_LMB_MB_HB_ANT1	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_CPLR_L_CPL2_IN_LB_LMB_MB_HB	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_HB_PAD_ANT2*	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_HB_PAD_MIMO_RX_OUT	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_CPLR_L_CPL3_ANT_LMB_MB_HB	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_LMB_HB_PORTB_TX_UAT	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_ANT9_UHB_N79_M	?
	50_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT_M	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_PAUHBU_*_ANT1_TO_ANT4	?
	50_TRX_THIN	P	A_50_THIN_SE	50_CPLR_U_CPL1_UAT_OUT	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_ANT2_LB_LMB_MB_HB_L1	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TANGIER_TP11	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_L1_LNA_IN	?
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_LAA_BPF_M	?
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9_M	?

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
	50_TX0_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	?
	50_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	?
	50_TX2_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	?
	50_RX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	?
	50_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	?
	50_TRX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	?

Class-Class Spacing

CLASS TO CLASS SPACING			
	CLASS NAME	CLASS NAME	CONSTRAINT SET
Bundles	50_TX0_THIN	50_TX0_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	50_TX1_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	50_TX2_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	50_RX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
GND	50_TX0_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TRX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
Thin-Wide	50_TX0_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX2_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XV_50_THIN_SE
	50_RX_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TRX_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TRX_HYBRID	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TRX_HYBRID	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX2_THIN	50_TRX_HYBRID	NA_DIELECTRIC_4XV_50_THIN_SE
	50_RX_THIN	50_TRX_HYBRID	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TRX_THIN	50_TRX_HYBRID	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TRX_HYBRID2	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TRX_HYBRID2	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX2_THIN	50_TRX_HYBRID2	NA_DIELECTRIC_4XV_50_THIN_SE
	50_RX_THIN	50_TRX_HYBRID2	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TRX_THIN	50_TRX_HYBRID2	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TRX_UHB_PAD	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TRX_UHB_PAD	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX2_THIN	50_TRX_UHB_PAD	NA_DIELECTRIC_4XV_50_THIN_SE
	50_RX_THIN	50_TRX_UHB_PAD	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TRX_THIN	50_TRX_UHB_PAD	NA_DIELECTRIC_4XV_50_THIN_SE

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AP Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLAMP OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LX/CX Nodes	PWR_SHAPE_LX	P	PWR_SHAPE	LX*	?
System-Wide	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN*	?
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_BOOST*	?
	PWR_200UM	P	PWR_200UM	PP1V8_S2	?
	PWR_100UM	P	PWR_100UM	PP1V8_S4	?
	PWR_100UM	P	PWR_100UM	PP1V2_S2	?
	PWR_100UM	P	PWR_100UM	PP1V2_S4	?
	PWR_100UM	P	PWR_100UM	PP3V0_S2	?
	PWR_100UM	P	PWR_100UM	PP3V0_DEBUG	?
Yeti	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_COOL_LED	?
	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_WARM_LED	?
	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_BOOST_OUT	?
Kobol	PWR_50UM	P	PWR_50UM	PP_VDDIO_IMU	?
AF/OIS (Shared)	PWR_SHAPE	P	PWR_SHAPE	PPVAR_RCAM_PVDD	?
	PWR_80UM	P	PWR_80UM	PP1V8_LAT_S2_CONN	?

RF Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLAMP OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
SMPS 1/6	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS1_6	?
SMPS 2	PWR_SHAPE	P	PWR_SHAPE	PP_1V22_SMPS2	?
	PWR_DEFAULT	P	PWR_DEFAULT	PP_1V24_SMPS2_SNS	?
SMPS 3	PWR_SHAPE	P	PWR_SHAPE	PP_0V82_SMPS3	?
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V82_SMPS3_SNS	?
SMPS 4	PWR_SHAPE	P	PWR_SHAPE	PP_1V9_SMPS4	?
	PWR_DEFAULT	P	PWR_DEFAULT	PP_1V9_SMPS4_SNS	?
SMPS 5	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS5	?
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V75_SMPS5_SNS	?
SMPS 7	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS7	?
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V75_SMPS7_SNS	?
LDO1	PWR_SHAPE	P	PWR_SHAPE	PP_1V2_LDO1	?
	PWR_500UM	P	PWR_500UM	PP_1V2_LDO1_SDR_VDDAM_RP, PP_1V2_LDO1_SDR_VDDAM_RX	?
	PWR_300UM	P	PWR_300UM	PP_LDO1_SDR_VDDAM_BBRX_BOT_215	?
	PWR_200UM	P	PWR_200UM	PP_1V2_LDO1_SDR_VDDAM_TX	?
	PWR_200UM	P	PWR_200UM	PP_LDO1_SDR_VDDAM_RX0_171, PP_LDO1_SDR_VDDAM_RX5_138	?
	PWR_100UM	P	PWR_100UM	PP_1V2_LDO1_SDR_VDDAM_TP, PP_LDO1_SDR_VDDAM_BBRX_TOP_97	?
	PWR_80UM	P	PWR_80UM	PP_LDO1_SDR_VDDAM_RP*_57, PP_LDO1_SDR_VDDAM_TX*_40	?
	PWR_50UM	P	PWR_50UM	PP_LDO1_SDR_VDDAM_*P*_30	?
LDO2	PWR_500UM	P	PWR_500UM	PP_1V1_LDO2	?
LDO3	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO3	?
	PWR_500UM	P	PWR_500UM	PP_0V8_LDO3_SDR_VDDAL_DIG	?
	PWR_500UM	P	PWR_500UM	PP_0V8_LDO3_SDR_VDDAL_RP, PP_0V8_LDO3_SDR_VDDAL_RX	?
	PWR_300UM	P	PWR_300UM	PP_LDO3_SDR_VDDAL_DIG1_171	?
	PWR_200UM	P	PWR_200UM	PP_LDO3_SDR_VDDAL_DIG2_124	?
	PWR_100UM	P	PWR_100UM	PP_0V8_LDO3_SDR_VDDAL_RXLO	?
	PWR_100UM	P	PWR_100UM	PP_0V8_LDO3_SDR_VDDAL_TP, PP_0V8_LDO3_SDR_VDDAL_TX	?
	PWR_100UM	P	PWR_100UM	PP_LDO3_SDR_VDDAL_RP*_57	?
	PWR_100UM	P	PWR_100UM	PP_LDO3_SDR_VDDAL_RX0_67, PP_LDO3_SDR_VDDAL_RX6_90	?
	PWR_80UM	P	PWR_80UM	PP_0V8_LDO3_SDR_VDDAL_DIG_RP	?
	PWR_50UM	P	PWR_50UM	PP_0V8_LDO3_SDR_VDDAL_DIG_TP	?
	PWR_50UM	P	PWR_50UM	PP_0V8_LDO3_SDR_VDDAL_ICON	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_DIG_*	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_FBRX_20	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_GNSS_40	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_ICON*	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_RX*_22	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_RXLO*_27	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_TP*_30	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_TX*_20	?
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_XO_18	?
LDO4	PWR_SHAPE	P	PWR_SHAPE	PP_0V875_LDO4	?
	PWR_200UM	P	PWR_200UM	PP_LDO4_SMR_*, PP_LDO4_VDD_*	?
LDO5	PWR_300UM	P	PWR_300UM	PP_1V8_LDO5	?
	PWR_200UM	P	PWR_200UM	PP_LDO5_SMR_VDDAH_2_*	?
	PWR_50UM	P	PWR_50UM	PP_LDO5_SMR_VDDAH_1_*, PP_LDO5_SMR_VDDAH_3_*, PP_LDO5_SMR_VDDAH_4_*	?
LDO6	PWR_300UM	P	PWR_300UM	PP_LDO6_VIO_1V8	?
	PWR_50UM	P	PWR_50UM	PP_LDO6_SMR_VDD_PX_20	?
	PWR_50UM	P	PWR_50UM	PP_LDO6_SDR_VDD_PXM_20	?
LDO7	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO7	?
LDO8	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO8	?
LDO9	PWR_500UM	P	PWR_500UM	PP_0V8_LDO9	?
	PWR_200UM	P	PWR_200UM	PP_LDO9_SMR_VDDAL_3_140	?
	PWR_100UM	P	PWR_100UM	PP_LDO9_SMR_VDDAL_4_90	?
	PWR_80UM	P	PWR_80UM	PP_LDO9_SMR_VDDAL_1_50	?
	PWR_50UM	P	PWR_50UM	PP_LDO9_SMR_VDDAL_*_10	?
LDO10	PWR_100UM	P	PWR_100UM	PP_3V1_LDO10	?
LDO11	PWR_100UM	P	PWR_100UM	PP_UIM1_LDO11	?
LDO12	PWR_SHAPE	P	PWR_SHAPE	PP_1V2_LDO12	?
	PWR_300UM	P	PWR_300UM	PP_LDO12_SMR_VDDAM_4_240	?
	PWR_300UM	P	PWR_300UM	PP_LDO12_SMR_VDDAM_5_240	?
	PWR_200UM	P	PWR_200UM	PP_LDO12_SMR_VDDAM_2_120	?
	PWR_100UM	P	PWR_100UM	PP_LDO12_SMR_VDDAM_*_70	?
LDO13	PWR_100UM	P	PWR_100UM	PP_UIM2_LDO13	?
LDO14	PWR_500UM	P	PWR_500UM	PP_0V6_LDO14	?
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V6_LDO14_SNS	?
LDO15	PWR_100UM	P	PWR_100UM	PP_1V2_LDO15	?
LDO16	PWR_750UM	P	PWR_750UM	PP_1V7_LDO16	?
	PWR_200UM	P	PWR_200UM	PP_1V7_LDO16_SDR_VDDAH_RP	?
	PWR_200UM	P	PWR_200UM	PP_1V7_LDO16_SDR_VDDAH_TX	?
	PWR_100UM	P	PWR_100UM	PP_1V7_LDO16_SDR_VDDAH_TP	?
	PWR_80UM	P	PWR_80UM	PP_1V7_LDO16_SDR_VDDAH_TXDAC	?
	PWR_50UM	P	PWR_50UM	PP_LDO16_SDR_VDDAH_*	?

RF Physical (continued)

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLAMP OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
QET0	PWR_500UM	P	PWR_500UM	PP_QET0_PA	?
	PWR_500UM	P	PWR_500UM	PP_QET0_2G_PA	?
	PWR_100UM	P	PWR_100UM	PP_QET0_PA_VBAT_LDO	?
	PWR_100UM	P	PWR_100UM	PP_QET0_AMP_OUT	?
	PWR_100UM	P	PWR_100UM	PP_QET0_VAUX_S	?
	PWR_100UM	P	PWR_100UM	PP_QET0_VDD_AMP	?
	PWR_100UM	P	PWR_100UM	PP_QET0_VDD_AMP_S	?
QET1	PWR_500UM	P	PWR_500UM	PP_QET1_PA	?
	PWR_100UM	P	PWR_100UM	PP_QET1_PA_VBAT_LDO	?
	PWR_100UM	P	PWR_100UM	PP_QET1_AMP_OUT	?
	PWR_100UM	P	PWR_100UM	PP_QET1_VAUX_S	?
	PWR_100UM	P	PWR_100UM	PP_QET1_VDD_AMP	?
	PWR_100UM	P	PWR_100UM	PP_QET1_VDD_AMP_S	?
APT (Lower)	PWR_500UM	P	PWR_500UM	PP_APT_L_PA	?
	PWR_200UM	P	PWR_200UM	PP_APT_L_N1A1	?
	PWR_200UM	P	PWR_200UM	PP_APT_L_N2A1	?
	PWR_200UM	P	PWR_200UM	PP_APT_L_N1A2	?
	PWR_200UM	P	PWR_200UM	PP_APT_L_N2A2	?
	PWR_200UM	P	PWR_200UM	PP_APT_L_LXA	?
APT (Upper)	PWR_500UM	P	PWR_500UM	PP_APT_U_PA	?
	PWR_200UM	P	PWR_200UM	PP_APT_U_N1A1	?
	PWR_200UM	P	PWR_200UM	PP_APT_U_N2A1	?
	PWR_200UM	P	PWR_200UM	PP_APT_U_N1A2	?
	PWR_200UM	P	PWR_200UM	PP_APT_U_N2A2	?
	PWR_200UM	P	PWR_200UM	PP_APT_U_LXA	?
PAD/DSM VDDs	PWR_50UM	P	PWR_50UM	VDD_HB_DSM	?
	PWR_50UM	P	PWR_50UM	VDD_LB_DSM	?
	PWR_50UM	P	PWR_50UM	VDD_LNA_HB_PAD	?
	PWR_50UM	P	PWR_50UM	VDD_MIMO1_DSM	?
	PWR_50UM	P	PWR_50UM	VDD_MIMO2_DSM	?
	PWR_50UM	P	PWR_50UM	VDD_UHB_DSM	?
Misc Radio	PWR_100UM	P	PWR_100UM	PP_PMX_VIO_OUT	?
	PWR_300UM	P	PWR_300UM	PP_VDD_RF_1V2	?
	PWR_100UM	P	PWR_100UM	PP_VREF_SDX	?
	PWR_80UM	P	PWR_80UM	PP1V8_S4_UAT_BRIDGE_VIO	?
	PWR_80UM	P	PWR_80UM	PP1V8_S2_LAT_BRIDGE_VIO	?
WiFi	PWR_100UM	P	PWR_100UM	PP0V72_CBUCK*	?
	PWR_100UM	P	PWR_100UM	PP1V02_ABUCK*	?
	PWR_100UM	P	PWR_100UM	PP1V8_LAT_FEM_LNA	?
	PWR_100UM	P	PWR_100UM	PP3V3_BTLDO	?
Fez	PWR_SHAPE	P	PWR_SHAPE	PP_VBAT_FEZ	?
	PWR_100UM	P	PWR_100UM	PP_1V85_FEZ	?
	PWR_100UM	P	PWR_100UM	PP3V0_S2_SP3T	?
	GND	P	DEFAULT	GND	?

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLAMP OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	GND	S	MSAP_YIELD	=	?
Power	PWR_DEFAULT	S	DEFAULT	=	?
	PWR_50UM	S	DEFAULT	=	?
	PWR_80UM	S	DEFAULT	=	?
	PWR_100UM	S	DEFAULT	=	?
	PWR_200UM	S	DEFAULT	=	?
	PWR_300UM	S	DEFAULT	=	?
	PWR_500UM	S	DEFAULT	=	?
	PWR_750UM	S	DEFAULT	=	?
	PWR_SHAPE	S	DEFAULT	=	?
	PWR_SHAPE_HV	S	HV_SPACING	=	?
RFFE	PWR_80UM_RFFE	S	DEFAULT	=	?
	PWR_SHAPE_LX	S	LX_SPACING	=	?

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_100UM	GND	MSAP_YIELD_PWR
PWR_100UM	PWR_100UM	100UM-249UM_SPACING
PWR_100UM	PWR_200UM	100UM-249UM_SPACING
PWR_100UM	PWR_300UM	100UM-249UM_SPACING
PWR_100UM	PWR_500UM	100UM-249UM_SPACING
PWR_100UM	PWR_750UM	100UM-249UM_SPACING
PWR_100UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_200UM	GND	MSAP_YIELD_PWR
PWR_200UM	PWR_200UM	100UM-249UM_SPACING
PWR_200UM	PWR_300UM	100UM-249UM_SPACING
PWR_200UM	PWR_500UM	100UM-249UM_SPACING
PWR_200UM	PWR_750UM	100UM-249UM_SPACING
PWR_200UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_300UM	GND	MSAP_YIELD_PWR
PWR_300UM	PWR_300UM	250UM+_SPACING
PWR_300UM	PWR_500UM	250UM+_SPACING
PWR_300UM	PWR_750UM	250UM+_SPACING
PWR_300UM	PWR_SHAPE	250UM+_SPACING
PWR_500UM	GND	MSAP_YIELD_PWR
PWR_500UM	PWR_500UM	250UM+_SPACING
PWR_500UM	PWR_750UM	250UM+_SPACING
PWR_500UM	PWR_SHAPE	250UM+_SPACING
PWR_750UM	GND	MSAP_YIELD_PWR
PWR_750UM	PWR_750UM	250UM+_SPACING
PWR_750UM	PWR_SHAPE	250UM+_SPACING
PWR_SHAPE	GND	MSAP_YIELD_PWR
PWR_SHAPE	PWR_SHAPE	250UM+_SPACING

PWR_SHAPE_LX spacing on next page

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PAGE TITLE: CONSTRAINTS: Power

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Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET0	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_VREG_S1_S6_SENSE	Y
E_DP_NTC	E	GENERIC_DP	DP:DP_NTC_*	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_ETDAC_QET0	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET0	Y
DP_ETDAC_QET1	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_VREG_S1_S6_SENSE	Y
DP_NTC	P	GENERIC_DP	DP:DP_NTC_*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_GENERIC	S	DEFAULT	=	Y
DP_NTC	S	A_DIELECTRIC_1.5X	=	Y
DP_ETDAC_QET0	S	A_DIELECTRIC_1.5X	=	Y
DP_ETDAC_QET1	S	A_DIELECTRIC_1.5X	=	Y

RF-Shield

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
SuBus	RF_SHIELD_SUBUS	P	PWR_100UM	LAT_SUBUS*	Y
	RF_SHIELD_SUBUS	P	PWR_100UM	UAT_SUBUS*	Y
RFFE	RF_SHIELD_RFFE	P	DEFAULT	RFFE0_XCVR_TO_LAT_LAA_VIO_R	Y
	RF_SHIELD_RFFE	P	DEFAULT	SHIELD_RFFE*	Y
Clocks	RF_SHIELD_CLK	P	DEFAULT	SHIELD_*_CLK, SHIELD_*_CLK_R,!SHIELD_RFFE*CLK	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD_*_CLK_32K	Y
Analog	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_ZQ	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_CAL	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_REXT	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_CAL_RES	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD_RFFE	S	DEFAULT	=	Y
RF_SHIELD_SUBUS	S	NA_DIELECTRIC_3X	=	Y
RF_SHIELD_CLK	S	NA_DIELECTRIC_3X	=	Y
RF_SHIELD_ANALOG	S	NA_DIELECTRIC_3X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
RF_SHIELD_RFFE	PWR_DEFAULT	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_50UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_80UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_100UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_200UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_300UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_500UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_750UM	NA_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_SHAPE	NA_DIELECTRIC_3X
RF_SHIELD_CLK	GND	DEFAULT
RF_SHIELD_ANALOG	GND	DEFAULT
RF_SHIELD_SUBUS	GND	DEFAULT
RF_SHIELD_SUBUS	RF_SHIELD_SUBUS	DEFAULT

Clocks

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	P	DEFAULT	CLK_*	Y
CLK_SPMI	P	DEFAULT	SPMI*CLK*	Y
CLK_SPI	P	DEFAULT	SPI*SCLK*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	S	A_DIELECTRIC_1.5X	=	Y
CLK_SPI	S	A_DIELECTRIC_1.5X	=	Y
CLK_SPMI	S	A_DIELECTRIC_1.5X	=	Y

Sensitive Analog

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	P	DEFAULT	ANALOG_FB_LEX	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
ANALOG	GND	DEFAULT

Grouping Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	P	DEFAULT	GPIO*, IO_*	Y
GRP_I2C	P	DEFAULT	I2C*	Y
GRP_I2S	P	DEFAULT	I2S*LRCLK*, I2S*BCLK*, I2S*DOUT*, I2S*DIN*	Y
GRP_SPI	P	DEFAULT	SPI*MOSI*, SPI*MISO*, SPI*CS*	Y
GRP_UART	P	DEFAULT	UART*	Y
GRP_SWD	P	DEFAULT	SWD*	Y
GRP_SPMI_DATA	P	DEFAULT	SPMI*DATA*	Y
GRP_PCIE_SIDE	P	DEFAULT	PCIE*CLKREQ*, PCIE*PERST*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	S	DEFAULT	=	Y
GRP_I2C	S	DEFAULT	=	Y
GRP_I2S	S	DEFAULT	=	Y
GRP_SPI	S	DEFAULT	=	Y
GRP_UART	S	DEFAULT	=	Y
GRP_SWD	S	DEFAULT	=	Y
GRP_SPMI_DATA	S	DEFAULT	=	Y
GRP_PCIE_SIDE	S	DEFAULT	=	Y

PWR_SHAPE_LX

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_SHAPE_LX	DP_ETDAC_QET0	A_DIELECTRIC_3X
PWR_SHAPE_LX	DP_ETDAC_QET1	A_DIELECTRIC_3X
PWR_SHAPE_LX	DP_NTC	A_DIELECTRIC_3X
PWR_SHAPE_LX	RF_SHIELD_RFFE	A_DIELECTRIC_3X
PWR_SHAPE_LX	RF_SHIELD_SUBUS	A_DIELECTRIC_3X
PWR_SHAPE_LX	RF_SHIELD_CLK	A_DIELECTRIC_3X
PWR_SHAPE_LX	RF_SHIELD_ANALOG	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK_SPI	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK_SPMI	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG	A_DIELECTRIC_3X
PWR_SHAPE_LX	PWR_SHAPE_LX	DEFAULT
PWR_SHAPE_LX	GND	DEFAULT

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CONSTRAINTS: Misc.

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HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	
ISL3	ISL2,ISL4	50	
ISL7	BOTTOM,ISL6	50	

All Thins

Wide

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
TOP	ISL3	50	
ISL6	BOTTOM,ISL4	50	

All Wides

Hybrid 50-ohm CSets

Thin on TOP and L3, Wide on L6

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE-L6_THIN-L1-L3		ZONE NAME= PRIMARY	
TOP	ISL2	50	
ISL3	ISL2,ISL4	50	
ISL6	BOTTOM,ISL4	50	

Thins

Wide

Wide on TOP and L6, Thin on L3

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE-L1-L6_THIN-L3		ZONE NAME= PRIMARY	
TOP	ISL3	50	
ISL3	ISL2,ISL4	50	
ISL6	BOTTOM,ISL4	50	

Custom mmW Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	S/D/A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
mmW IF	50_MMW_IF	P	50_OHM_MMW_IF_SE	50_MMW_*IFH*, 50_MMW_*IFV*	Y
mmW RF	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S1H_HPOL,50_MMW_SMR525_S1L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S2H_HPOL,50_MMW_SMR525_S2L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S5H_HPOL,50_MMW_SMR525_S5L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S6H_HPOL,50_MMW_SMR525_S6L_HPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S7H_HPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S7L_HPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S8H_HPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S8L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S9H_VPOL,50_MMW_SMR525_S9L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S10H_VPOL,50_MMW_SMR525_S10L_VPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S11H_VPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S11L_VPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S12H_VPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S12L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S13H_VPOL,50_MMW_SMR525_S13L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S14H_VPOL,50_MMW_SMR525_S14L_VPOL	Y

Spacing

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	S/D/A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
mmW IF	50_MMW_IF	S	DIELECTRIC_4XV_50_MMW_IF_SE	=	Y
mmW RF	50_MMW_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y
	50_MMW_SMYRNA_HB_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y
	50_MMW_SMYRNA_LB_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_MMW_IF	GND	DIELECTRIC_2X_50_MMW_IF_SE
50_MMW_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SE
50_MMW_SMYRNA_HB_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SMYRNA_HB_SE
50_MMW_SMYRNA_LB_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SMYRNA_LB_SE

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	S/D/A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_80UM	P	PWR_80UM	PP_BBPMK_VREG_RF	Y
PWR_80UM	P	PWR_80UM	PP_BBPMK_VREG_XO	Y
PWR_80UM	P	PWR_80UM	PP_PMK_REF_BYP	Y

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	S/D/A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
XTAL_OSC	S	NA_DIELECTRIC_3X	XO_GND	Y
XTAL_OSC	S	NA_DIELECTRIC_3X	XO_THERM	Y
XTAL_OSC	S	NA_DIELECTRIC_3X	THERMAL_GNSS_XO_THERM	Y

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
XTAL_OSC	XTAL_OSC	DEFAULT
XTAL_OSC	GND	DEFAULT

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PAGE TITLE
CONSTRAINTS: Stackup/Misc. (FF-Specific)

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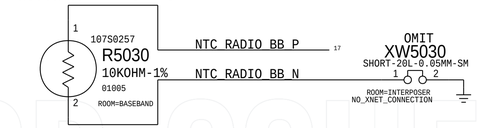
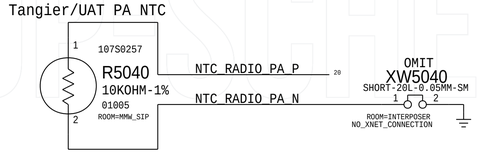
Bot MLB NTCs

Place NTC XWs near PMU, route P/N differentially

Baseband/BB PMU NTC



Tangier/UAT PA NTC



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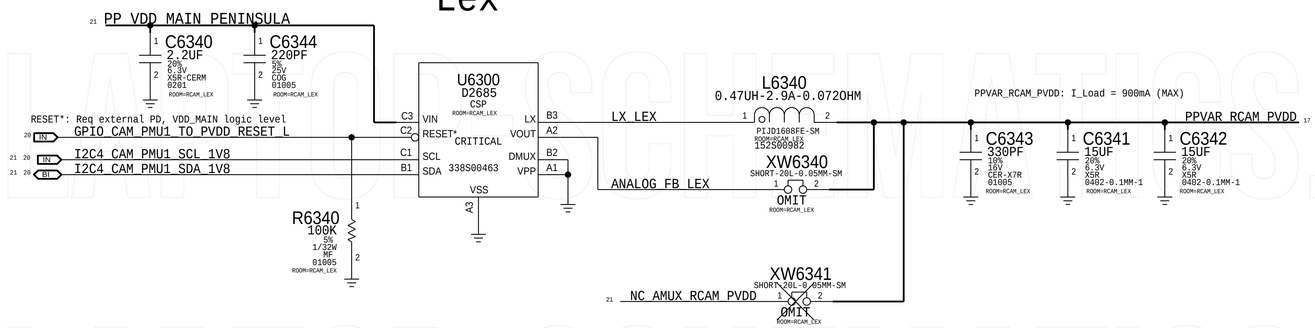
SUBSYSTEM SPECIFIC BOM TABLES

15uF 0402 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C6341,C6342)	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

Lex



SYNCING: D52, D53

PAGE TITLE	CAMERA: Actuator Supply (Lex)
DRAWING NUMBER	051-05262
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LED STROBE DRIVER (YETI)

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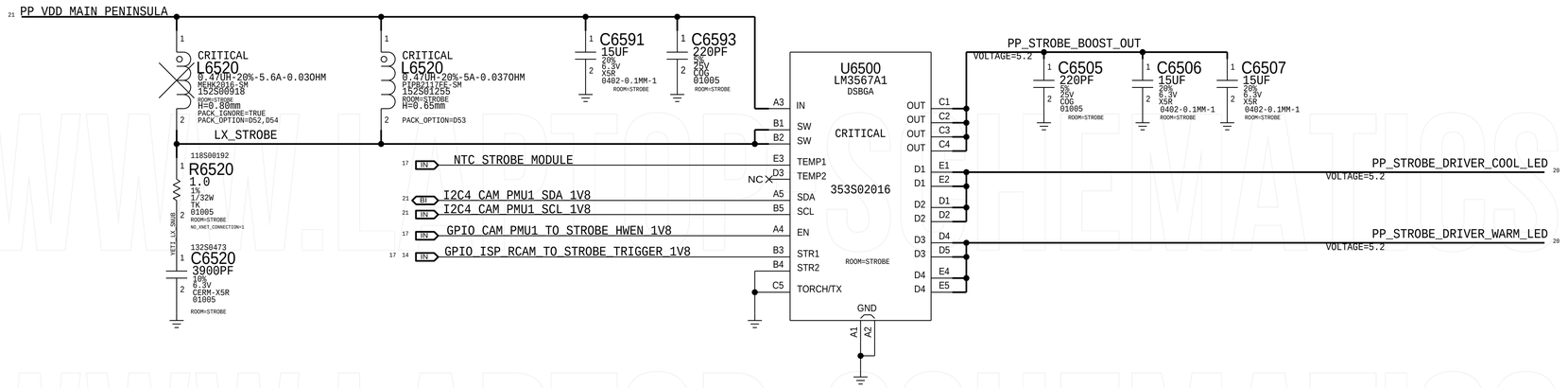
I2C Address (7-bit): 0x65



SYNCING: D52, D53, D54

PAGE TITLE	CAMERA: Strobe Driver
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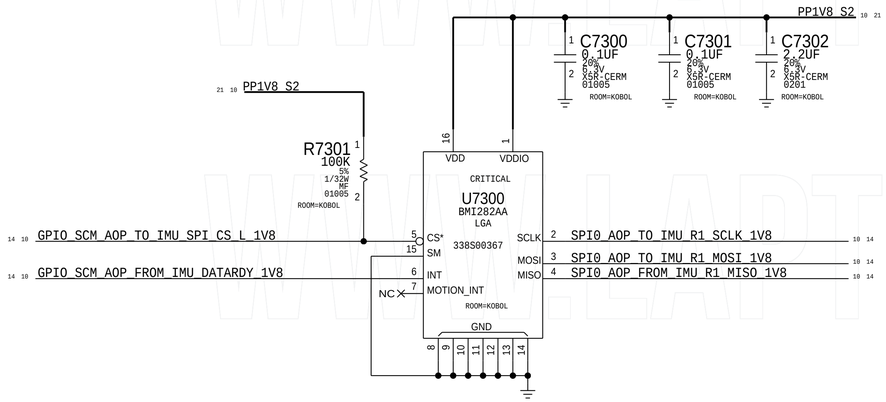
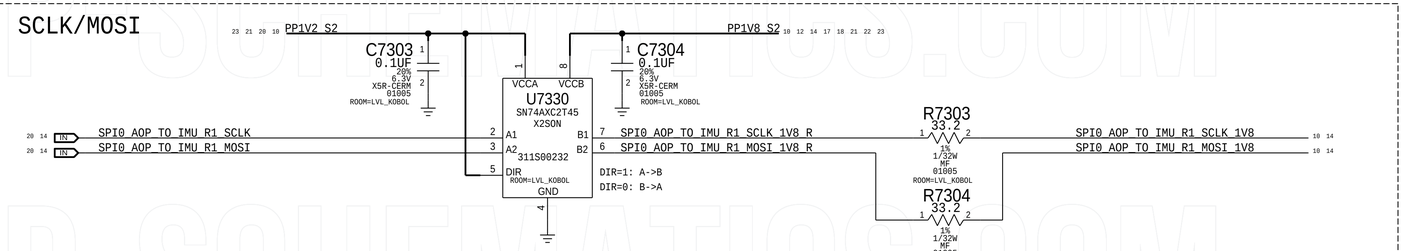
KOBOL - ACCEL & GYRO

IMU

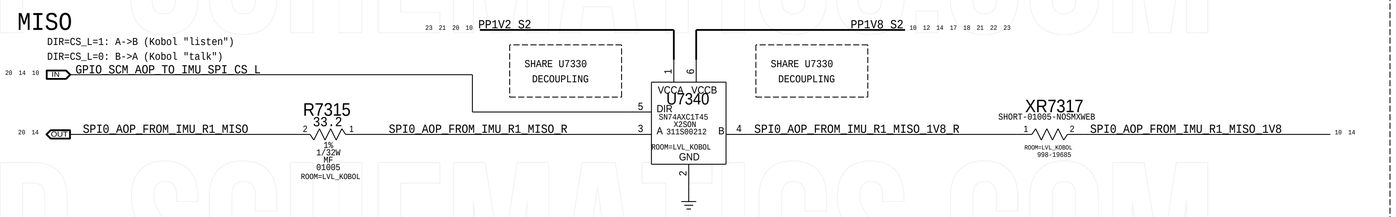


Level Translators

SCLK/MOSI



MISO



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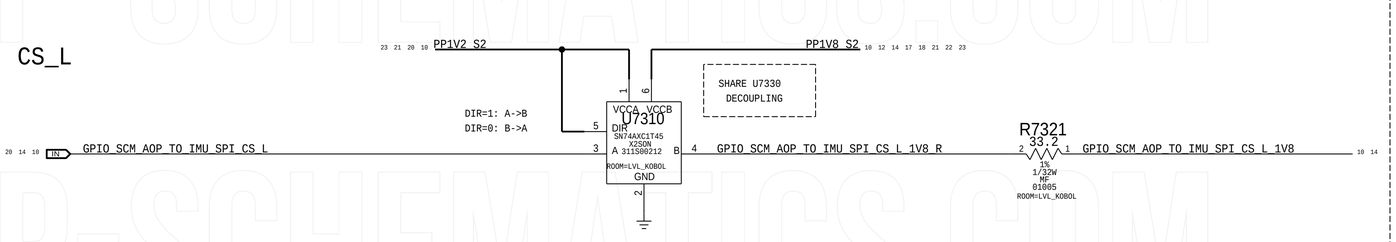

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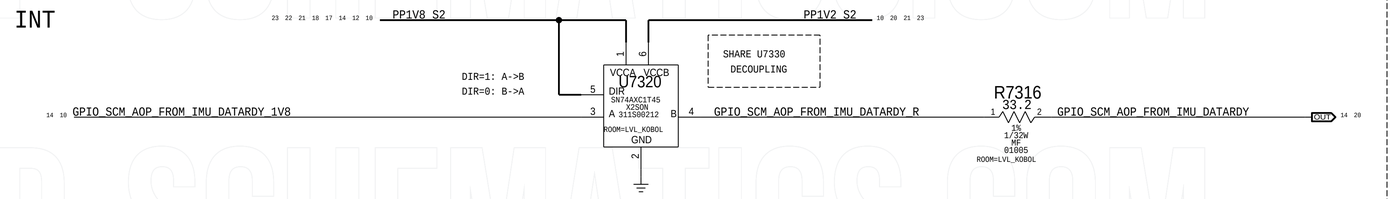

SYNCING: D52, D53, D54

PAGE TITLE: SENSORS: Accel / Gyro

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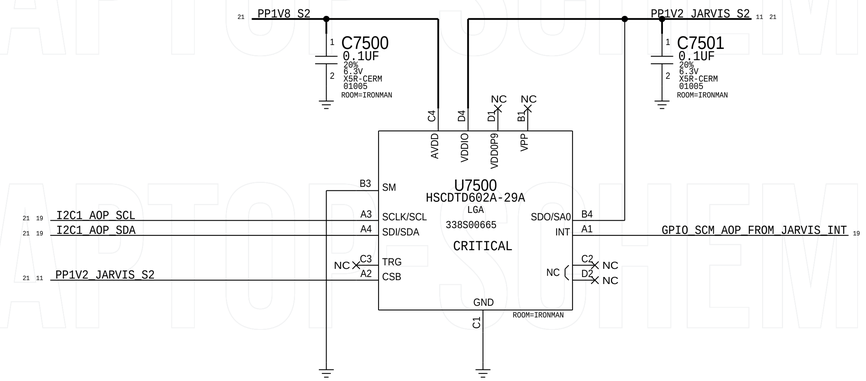
Jarvis (Bottom)



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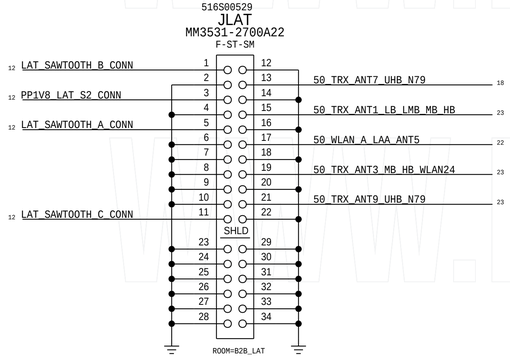
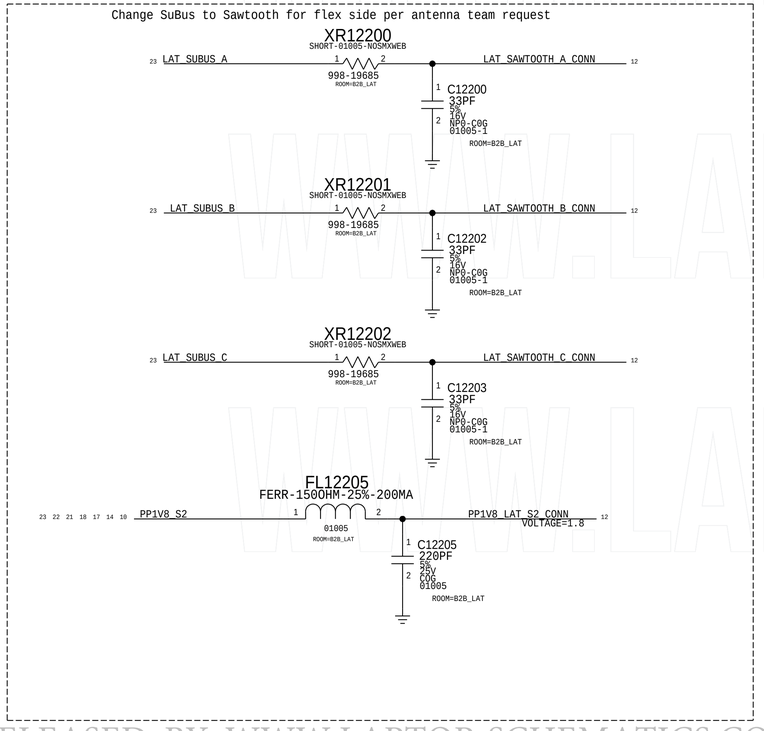
LAT B2B

Connector



SUBUS filtering



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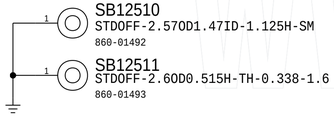
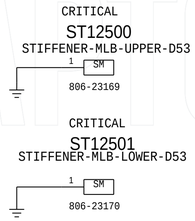
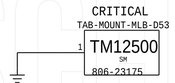
Standoffs



Stiffeners

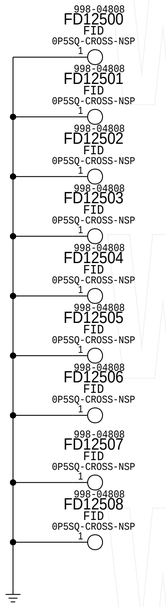


Mounts

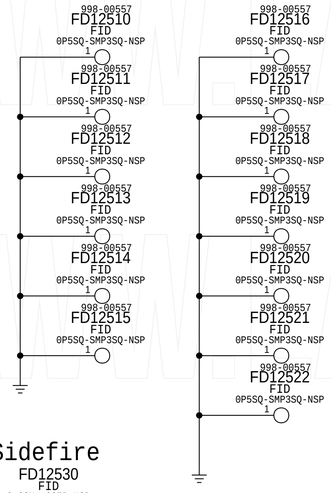


Fiducials

Crosses

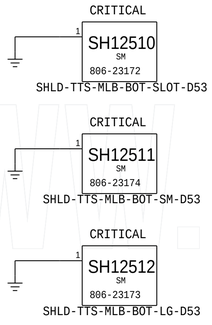


Squares



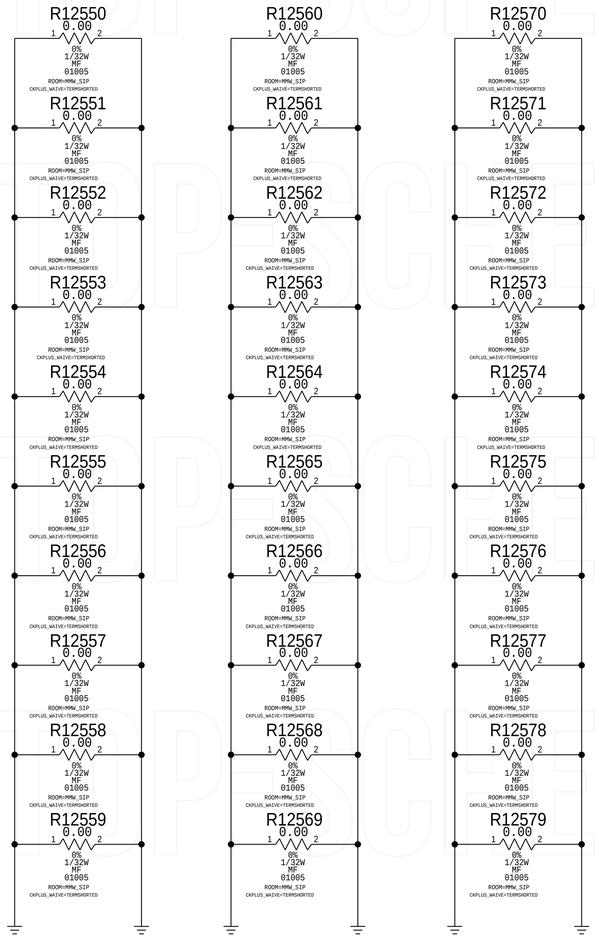
Sidefire

Shields

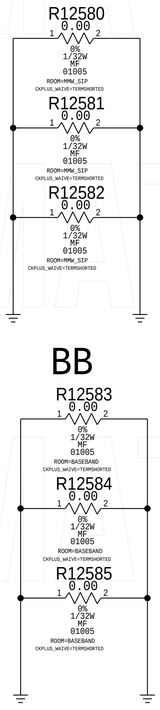


Tangier Underfill Dam

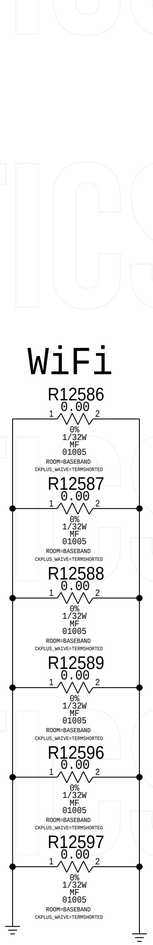
RefDes start at R12550 to avoid conflict w/ mlb_top



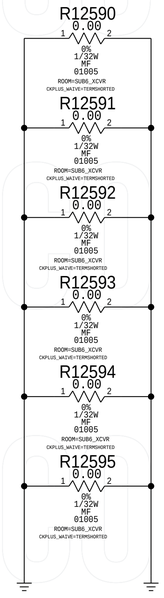
BB



WiFi



Sub6 XCVR Underfill Dam



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MECHANICAL: Standoffs, Shields, etc.

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Kobol

PP12800
998-01377
0.15MM SM
ROOM=TEST
10 GPIO_SCM_AOP_FROM_IMU_DATARDY_1V8

PP12801
998-01377
0.15MM SM
ROOM=TEST
20 10 GPIO_SCM_AOP_FROM_IMU_DATARDY

PP12802
998-01377
0.15MM SM
ROOM=TEST
10 SPI0_AOP_TO_IMU_R1_SCLK_1V8

PP12803
998-01377
0.15MM SM
ROOM=TEST
10 SPI0_AOP_TO_IMU_R1_MOSI_1V8

PP12804
998-01377
0.15MM SM
ROOM=TEST
20 10 SPI0_AOP_TO_IMU_R1_SCLK

PP12805
998-01377
0.15MM SM
ROOM=TEST
20 10 SPI0_AOP_TO_IMU_R1_MOSI

PP12806
998-01377
0.15MM SM
ROOM=TEST
20 10 GPIO_SCM_AOP_TO_IMU_SPI_CS_L

PP12807
998-01377
0.15MM SM
ROOM=TEST
10 GPIO_SCM_AOP_TO_IMU_SPI_CS_L_1V8

PP12808
998-01377
0.15MM SM
ROOM=TEST
10 SPI0_AOP_FROM_IMU_R1_MISO_1V8

PP12809
998-01377
0.15MM SM
ROOM=TEST
20 10 SPI0_AOP_FROM_IMU_R1_MISO

PP12811
998-01377
0.15MM SM
ROOM=TEST
23 22 21 18 17 12 10 PP1V8_S2

Yeti

PP12820
998-01377
0.15MM SM
PLACE_SIDE=BOTTOM
ROOM=TEST
17 9 GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8

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17	GND	1	IO1	IO91	91	GND	17
17	GND	2	IO2	IO92	92	PP_VDD_MAIN_PENINSULA	17
17	GND	3	IO3	IO93	93	GND	17
17	GND	4	IO4	IO94	94	PP_VDD_MAIN_PENINSULA	17
17	GND	5	IO5	IO95	95	GND	17
17	GND	6	IO6	IO96	96	PP_VDD_MAIN_PENINSULA	17
17	GPIO_AP_CANARY6_LEG2	7	IO7	IO97	97	GND	17
17	GND	8	IO8	IO98	98	GND	17
17	GND	9	IO9	IO99	99	GND	17
17	GPIO_AP_CANARY6_LEG2	10	IO10	IO100	100	GND	17
17	GND	11	IO11	IO101	101	GND	17
17	GND	12	IO12	IO102	102	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	17
17	GND	13	IO13	IO103	103	GND	17
17	GND	14	IO14	IO104	104	PP_VDD_BOOST_NORTH_PA	17
17	GPIO_AP_CANARY6_LEG1	15	IO15	IO105	105	GND	17
17	GPIO_AP_CANARY6_LEG1	16	IO16	IO106	106	PP1V2_S4	17
17	GND	17	IO17	IO107	107	GND	17
17	PP1V8_S2	18	IO18	IO108	108	GPIO_AOP_TO_WLAN_CONTEXT_A	17
17	GND	19	IO19	IO109	109	GND	17
17	GND	20	IO20	IO110	110	PP1V8_S4	17
17	GND	21	IO21	IO111	111	GND	17
17	GND	22	IO22	IO112	112	RFFE_WLAN_TO_UAT_2G_FEM_RST_L	17
17	GND	23	IO23	IO113	113	GND	17
17	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	24	IO24	IO114	114	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	17
17	GND	25	IO25	IO115	115	GND	17
17	GND	26	IO26	IO116	116	GPIO_SE_TO_BT_PKT_RDY	17
17	GND	27	IO27	IO117	117	GND	17
17	IO_R1_TO_BB_LAA_SW_CTRL	28	IO28	IO118	118	GND	17
17	GND	29	IO29	IO119	119	GND	17
17	IO_BT_TO_R1_WAKE	30	IO30	IO120	120	I2C_BT_TO_NFC_SCL	17
17	GND	31	IO31	IO121	121	GND	17
17	GND	32	IO32	IO122	122	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	17
17	GND	33	IO33	IO123	123	GND	17
17	PPVAR_RCAM_PVDD	34	IO34	IO124	124	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	17
17	GND	35	IO35	IO125	125	GND	17
17	GND	36	IO36	IO126	126	GND	17
17	GND	37	IO37	IO127	127	GND	17
17	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	38	IO38	IO128	128	I2C_BT_TO_NFC_SDA	17
17	GND	39	IO39	IO129	129	GND	17
17	GPIO_BB_TO_R1_CH9_REQ	40	IO40	IO130	130	GPIO_AP_FROM_WLAN_TIME_SYNC	17
17	GND	41	IO41	IO131	131	GND	17
17	NTC_STROBE_MODULE	42	IO42	IO132	132	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	17
17	GND	43	IO43	IO133	133	GND	17
17	GND	44	IO44	IO134	134	GND	17
17	GPIO_AP_CANARY5_LEG1	45	IO45	IO135	135	GND	17
17	GND	46	IO46	IO136	136	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	17
17	GPIO_AP_CANARY5_LEG1	47	IO47	IO137	137	GND	17
17	GND	48	IO48	IO138	138	GPIO_AP_TO_BB_PEAK_PWR_IND	17
17	GND	49	IO49	IO139	139	GND	17
17	GND	50	IO50	IO140	140	SWD_AP_BI_BB_SWDIO	17
17	GPIO_AP_CANARY5_LEG2	51	IO51	IO141	141	GND	17
17	GND	52	IO52	IO142	142	GND	17
17	GND	53	IO53	IO143	143	GND	17
17	GPIO_AP_CANARY5_LEG2	54	IO54	IO144	144	GPIO_AP_FROM_BB_RESET_DETECT_L	17
17	GND	55	IO55	IO145	145	GND	17
17	GND	56	IO56	IO146	146	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	17
17	GND	57	IO57	IO147	147	GND	17
17	GND	58	IO58	IO148	148	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	17
17	GND	59	IO59	IO149	149	GND	17
17	GND	60	IO60	IO150	150	GND	17
				IO151	151	GND	17
17	GND	62	IO62	IO152	152	GPIO_AP_FROM_BT_AUDIO_SYNC	17
17	GPIO_AP_CANARY5_LEG3	63	IO63	IO153	153	GND	17
17	GND	64	IO64	IO154	154	GPIO_AP_TO_BB_TIME_MARK	17
17	GND	65	IO65	IO155	155	GND	17
17	GND	66	IO66	IO156	156	NTC_RADIO_BB_P	17
17	GPIO_AP_CANARY5_LEG3	67	IO67	IO157	157	GND	17
17	GND	68	IO68	IO158	158	GND	17
17	GPIO_AP_CANARY5_LEG4	69	IO69	IO159	159	GND	17
17	GND	70	IO70	IO160	160	UART1_AOP_FROM_BB_RXD	17
17	GND	71	IO71	IO161	161	GND	17
17	GND	72	IO72	IO162	162	UART1_AOP_TO_BB_TXD	17
17	GND	73	IO73	IO163	163	GND	17
17	GND	74	IO74	IO164	164	GPIO_AOP_TO_BB_FORCE_PWM	17
17	GND	75	IO75	IO165	165	GND	17
17	GND	76	IO76	IO166	166	GND	17
17	GND	77	IO77	IO167	167	GND	17
17	GND	78	IO78	IO168	168	PP_VDD_RF_1V2	17
17	GND	79	IO79	IO169	169	GND	17
17	GND	80	IO80	IO170	170	GND	17
17	GND	81	IO81	IO171	171	GND	17
17	GND	82	IO82	IO172	172	GPIO_AOP_TO_WLAN_CONTEXT_B	17
17	GND	83	IO83	IO173	173	GND	17
17	GND	84	IO84	IO174	174	GND	17
17	GND	85	IO85	IO175	175	GND	17
17	GND	86	IO86	IO176	176	PP_VDD_BOOST_BBPMU	17
17	GPIO_AP_CANARY5_LEG4	87	IO87	IO177	177	GND	17
17	GND	88	IO88	IO178	178	GND	17
17	GND	89	IO89	IO179	179	GND	17
17	PP_VDD_MAIN_PENINSULA	90	IO90	IO180	180	PP_VDD_MAIN_QET_BBPMU_APTL	17

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18	GND	181	IO181	IO271	271	50_TRX_LB_PAD_ANT1	18
18	PP_VDD_MAIN_QET_BBPMU_APTL	182	IO182	IO272	272	GND	18
18	GND	183	IO183	IO273	273	GND	18
18	PP_VDD_MAIN_QET_BBPMU_APTL	184	IO184	IO274	274	GND	18
18	GND	185	IO185	IO275	275	GND	18
18	PP_VDD_MAIN_QET_BBPMU_APTL	186	IO186	IO276	276	50_TRX_IN_LMB_PAD_2G_MB_OUT_M	18
18	GND	187	IO187	IO277	277	GND	18
18	GND	188	IO188	IO278	278	GND	18
18	GND	189	IO189	IO279	279	GND	18
18	PP3V0_S2	190	IO190	IO280	280	50_TRX_IN_LMB_PAD_LMB_ANT_M	18
18	GND	191	IO191	IO281	281	GND	18
18	GND	192	IO192	IO282	282	GND	18
18	GND	193	IO193	IO283	283	GND	18
18	GND	194	IO194	IO284	284	GND	18
18	GND	195	IO195	IO285	285	50_TRX_WLAN_G_BT_ANT3_NPLXR	18
18	GND	196	IO196	IO286	286	GND	18
18	GND	197	IO197	IO287	287	GND	18
18	GND	198	IO198	IO288	288	GND	18
18	GND	199	IO199				
18	GPIO_BT_TO_BOT_SPKR_TRIG	200	IO200	IO290	290	GND	18
18	GND	201	IO201	IO291	291	50_TX_IN_XCVR_TX0_MB2G	18
18	GND	202	IO202	IO292	292	GND	18
18	GND	203	IO203	IO293	293	GND	18
18	GND	204	IO204	IO294	294	GND	18
18	GND	205	IO205				
18	GND	206	IO206	IO296	296	GND	18
18	GND	207	IO207	IO297	297	50_TRX_ANT7_UHB_N79	18
18	GND	208	IO208	IO298	298	GND	18
18	GND	209	IO209	IO299	299	GND	18
18	RFFE_WLAN_TO_LAT_2G_FEM_RST_L	210	IO210	IO300	300	GND	18
18	GND	211	IO211	IO301	301	50_TX_IN_XCVR_TX0_LMB	18
18	GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	212	IO212	IO302	302	GPIO_AOP_CANARY7_LEG3	18
18	GND	213	IO213	IO303	303	GND	18
18	ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	214	IO214	IO304	304	GND	18
18	GND	215	IO215	IO305	305	GND	18
18	PP_LDO6_VIO_1V8	216	IO216	IO306	306	PP_VDD_MAIN_5GFEML	18
18	GND	217	IO217	IO307	307	PP_VDD_MAIN_5GFEML	18
18	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	218	IO218	IO308	308	GND	18
18	GND	219	IO219	IO309	309	GND	18
18	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	220	IO220	IO310	310	GPIO_AOP_CANARY7_LEG2	18
18	GND	221	IO221	IO311	311	GND	18
18	PP1V8_S2	222	IO222	IO312	312	GND	18
18	GND	223	IO223	IO313	313	GND	18
18	GND	224	IO224	IO314	314	GND	18
18	GND	225	IO225	IO315	315	GND	18
18	50_RX_LMB_PAD_LMB_PRX_OUT_M	226	IO226	IO316	316	GND	18
18	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	227	IO227	IO317	317	GND	18
18	GND	228	IO228	IO318	318	GND	18
18	GND	229	IO229	IO319	319	GND	18
18	GND	230	IO230	IO320	320	GND	18
18	GND	231	IO231	IO321	321	GPIO_AOP_CANARY7_LEG2	18
18	50_TX_IN_XCVR_TX0_LB	232	IO232	IO322	322	GND	18
18	GND	233	IO233	IO323	323	GND	18
18	GND	234	IO234	IO324	324	GND	18
18	GND	235	IO235	IO325	325	GND	18
18	50_UHB_L_CPLR_OUT	236	IO236	IO326	326	GPIO_AOP_CANARY7_LEG1	18
18	50_RX_XCVR_PRX6_LB_A_RX0	237	IO237	IO327	327	GND	18
18	GND	238	IO238	IO328	328	GPIO_AOP_CANARY7_LEG1	18
18	GND	239	IO239	IO329	329	GND	18
18	GND	240	IO240	IO330	330	GND	18
18	GND	241	IO241	IO331	331	GND	18
18	PP_QET0_2G_PA	242	IO242	IO332	332	GND	18
18	GND	243	IO243	IO333	333	GND	18
18	PP_QET0_2G_PA	244	IO244	IO334	334	GND	18
18	GND	245	IO245	IO335	335	GND	18
18	PP_QET0_PA	246	IO246	IO336	336	50_TRX_PAUHBL_N79_ANT2_TO_ANT9	18
18	GND	247	IO247	IO337	337	GND	18
18	PP_QET0_PA	248	IO248	IO338	338	GND	18
18	GND	249	IO249	IO339	339	50_TRX_UHB_PAD_PORTB_TX_M	18
18	GND	250	IO250	IO340	340	GND	18
18	GND	251	IO251	IO341	341	GND	18
18	50_WLAN_G_C1_TXRX_FEM_M	252	IO252	IO342	342	50_TRX_UHB_PAD_N79_PORTB_TX_M	18
18	GND	253	IO253	IO343	343	GND	18
18	GND	254	IO254	IO344	344	GND	18
18	GND	255	IO255	IO345	345	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	18
18	SHIELD_RFFE1_SCLK_SDR	256	IO256	IO346	346	GND	18
18	GND	257	IO257	IO347	347	GND	18
18	GND	258	IO258	IO348	348	50_TRX_LB_PORTB_RX1_M	18
18	GND	259	IO259	IO349	349	GND	18
18	SHIELD_RFFE1_SDATA_SDR	260	IO260	IO350	350	GND	18
18	GND	261	IO261				
18	GND	262	IO262	IO352	352	GND	18
18	GPIO_AOP_CANARY7_LEG4	263	IO263				
18	GND	264	IO264	IO354	354	GND	18
18	GPIO_AOP_CANARY7_LEG4	265	IO265	IO355	355	50_TX_IN_XCVR_TX0_LB2G	18
18	GND	266	IO266	IO356	356	GND	18
18	GPIO_AOP_CANARY7_LEG3	267	IO267	IO357	357	50_RX_XCVR_PRX10_LB_PRX_OUT2	18
18	GND	268	IO268	IO358	358	50_TRX_LB_PORTB_TX_M	18
18	GND	269	IO269	IO359	359	GND	18
18	GND	270	IO270	IO360	360	GND	18

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19	GND	361	IO361	IO451	451	GND	19
19	PP_APT_L_PA	362	IO362	IO452	452	GND	19
19	PP_APT_L_PA	363	IO363	IO453	453	GND	19
19	GND	364	IO364	IO454	454	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	19
19	GND	365	IO365	IO455	455	GND	19
19	PP_QET1_PA	366	IO366	IO456	456	I2S2_AP_FROM_BB_BCLK	19
19	PP_QET1_PA	367	IO367	IO457	457	GND	19
19	GND	368	IO368	IO458	458	I2S2_AP_FROM_BB_LRCLK	19
19	GND	369	IO369	IO459	459	GND	19
19	GND	370	IO370	IO460	460	GND	19
19	50_RX_XCVR_PRX15_N79_RX_OUT2	371	IO371	IO461	461	GND	19
19	GND	372	IO372	IO462	462	I2S2_AP_FROM_BB_DIN	19
19	GND	373	IO373	IO463	463	GND	19
19	GND	374	IO374	IO464	464	I2S2_AP_TO_BB_DOUT	19
19	50_RX_XCVR_PRX17_UHB_RX_OUT2	375	IO375	IO465	465	GND	19
19	50_RX_XCVR_PRX14_N79_RX_OUT1	376	IO376	IO466	466	GND	19
19	GND	377	IO377	IO467	467	GND	19
19	GND	378	IO378				
19	GND	379	IO379	IO469	469	GND	19
19	GND	380	IO380	IO470	470	GND	19
19	50_RX_XCVR_PRX16_UHB_RX_OUT1	381	IO381	IO471	471	GND	19
19	SHIELD_RFFE2_SDATA_SDR	382	IO382	IO472	472	GND	19
19	GND	383	IO383	IO473	473	GND	19
19	SHIELD_RFFE2_SCLK_SDR	384	IO384	IO474	474	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	19
19	SHIELD_RFFE8_SDATA_SDR	385	IO385	IO475	475	GND	19
19	SHIELD_RFFE8_SCLK_SDR	386	IO386	IO476	476	GPIO_S4_PMU_TO_WLAN_REG_ON	19
19	PP_VDD_BOOST_SOUTH_PA	387	IO387	IO477	477	GND	19
19	GND	388	IO388	IO478	478	GPIO_PMU_FROM_WLAN_HOST_WAKE	19
19	GND	389	IO389	IO479	479	GND	19
19	GND	390	IO390	IO480	480	GND	19
19	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	391	IO391	IO481	481	GND	19
19	GND	392	IO392	IO482	482	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	19
19	GND	393	IO393	IO483	483	GND	19
19	GND	394	IO394	IO484	484	PCIE_GP1_AP_TO_WLAN_PERST_L	19
19	50_TX_IN_XCVR_TX1_LB_JB	395	IO395	IO485	485	GND	19
19	SHIELD_RFFE3_SDATA_SDR	396	IO396	IO486	486	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	19
19	GND	397	IO397	IO487	487	GND	19
19	SHIELD_RFFE3_SCLK_SDR	398	IO398	IO488	488	GND	19
19	GND	399	IO399	IO489	489	GND	19
19	GND	400	IO400	IO490	490	PCIE_GP2_AP_TO_BB_PERST_L	19
19	GND	401	IO401	IO491	491	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	402	IO402	IO492	492	PCIE_GP2_AP_BI_BB_CLKREQ_L	19
19	GND	403	IO403	IO493	493	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	404	IO404	IO494	494	SWD_AP_TO_MANY_SWCLK	19
19	GND	405	IO405	IO495	495	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	406	IO406	IO496	496	GPIO_AP_TO_BB_COREDUMP	19
19	GND	407	IO407	IO497	497	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	408	IO408				
19	GND	409	IO409	IO499	499	GND	19
19	GND	410	IO410	IO500	500	GND	19
19	GND	411	IO411	IO501	501	GND	19
19	GND	412	IO412	IO502	502	GND	19
19	GND	413	IO413	IO503	503	GND	19
19	PP1V2_JARVIS_S2	414	IO414	IO504	504	CLK_BBPMU_TO_NFC_38M4	19
19	GND	415	IO415	IO505	505	GND	19
19	GND	416	IO416	IO506	506	GND	19
19	GND	417	IO417	IO507	507	GND	19
19	GND	418	IO418	IO508	508	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	19
19	GND	419	IO419	IO509	509	GND	19
19	GPIO_SCM_AOP_FROM_JARVIS_INT	420	IO420	IO510	510	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	19
19	GND	421	IO421	IO511	511	GND	19
19	I2C1_AOP_SCL	422	IO422	IO512	512	GND	19
19	GND	423	IO423	IO513	513	GND	19
19	I2C1_AOP_SDA	424	IO424	IO514	514	90_PCIE_GP1_AP_FROM_WLAN_RX_N	19
19	GND	425	IO425	IO515	515	GND	19
19	GND	426	IO426	IO516	516	90_PCIE_GP1_AP_FROM_WLAN_RX_P	19
19	GND	427	IO427	IO517	517	GND	19
19	90_PCIE_GP2_AP_TO_BB_TX_N	428	IO428	IO518	518	GND	19
19	GND	429	IO429	IO519	519	GND	19
19	90_PCIE_GP2_AP_TO_BB_TX_P	430	IO430	IO520	520	90_PCIE_GP1_AP_TO_WLAN_TX_P	19
19	GND	431	IO431	IO521	521	GND	19
19	GND	432	IO432	IO522	522	90_PCIE_GP1_AP_TO_WLAN_TX_N	19
19	GND	433	IO433	IO523	523	GND	19
19	90_PCIE_GP2_AP_FROM_BB_RX_P	434	IO434	IO524	524	GND	19
19	GND	435	IO435	IO525	525	GND	19
19	90_PCIE_GP2_AP_FROM_BB_RX_N	436	IO436	IO526	526	CLK_BBPMU_TO_DOTARA_38M4	19
19	GND	437	IO437	IO527	527	GND	19
19	GND	438	IO438	IO528	528	GND	19
19	GND	439	IO439	IO529	529	GND	19
19	90_PCIE_GP2_AP_TO_BB_REFCLK_N	440	IO440	IO530	530	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	19
19	GND	441	IO441	IO531	531	GND	19
19	90_PCIE_GP2_AP_TO_BB_REFCLK_P	442	IO442	IO532	532	GND	19
19	GND	443	IO443	IO533	533	GND	19
19	GND	444	IO444	IO534	534	GND	19
19	GND	445	IO445	IO535	535	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	446	IO446				
19	GND	447	IO447	IO537	537	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	448	IO448	IO538	538	GND	19
19	GND	449	IO449	IO539	539	GND	19
19	PP_VDD_MAIN_QET_BBPMU_APTL	450	IO450	IO540	540	GND	19

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20	GND	541	IO541	IO631	631	GND	20
20	GND	542	IO542	IO632	632	SHIELD_RFFE5_SDATA_SDR	20
20	50_WLAN_A_C0_TXRX_FEM_M	543	IO543	IO633	633	GND	20
20	GND	544	IO544	IO634	634	GND	20
20	GND	545	IO545	IO635	635	GND	20
20	50_WLAN_G_C0_TXRX_FEM_M	546	IO546	IO636	636	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	20
20	GND	547	IO547	IO637	637	GND	20
20	GND	548	IO548	IO638	638	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	20
20	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	549	IO549	IO639	639	GND	20
20	GND	550	IO550	IO640	640	GND	20
20	GND	551	IO551	IO641	641	GND	20
20	50_TRX_PAUHBU_N79_ANT1_TO_ANT4	552	IO552	IO642	642	UAT_SUBUS_B	20
20	GND	553	IO553	IO643	643	GND	20
20	GND	554	IO554	IO644	644	UAT_SUBUS_A	20
20	GND	555	IO555	IO645	645	GND	20
20	GND	556	IO556	IO646	646	GND	20
20	GND	557	IO557	IO647	647	GND	20
20	GND	558	IO558	IO648	648	NTC_RADIO_PA_P	20
20	GND	559	IO559	IO649	649	GND	20
20	IO_NFC_TO_BBPMU_CLKREQ	560	IO560	IO650	650	UAT_TUNER_TO_R1_STATE	20
20	GND	561	IO561	IO651	651	GND	20
20	GND	562	IO562	IO652	652	GPIO_R1_TO_BB_CH9_COEX	20
20	GND	563	IO563	IO653	653	GND	20
20	GND	564	IO564	IO654	654	GND	20
20	GND	565	IO565	IO655	655	GND	20
20	GND	566	IO566	IO656	656	GPIO_R1_TO_WLAN_COEX	20
20	GND	567	IO567	IO657	657	GND	20
20	GND	568	IO568	IO658	658	PP1V2_S2	20
20	GND	569	IO569	IO659	659	GND	20
20	GND	570	IO570	IO660	660	GND	20
20	GND	571	IO571	IO661	661	GND	20
20	GND	572	IO572	IO662	662	GPIO_CAM_PMU1_TO_PVDD_RESET_L	20
20	GND	573	IO573	IO663	663	GND	20
20	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	574	IO574	IO664	664	I2C4_CAM_PMU1_SCL_1V8	20
20	GND	575	IO575	IO665	665	GND	20
20	GND	576	IO576	IO666	666	GND	20
20	GND	577	IO577	IO667	667	GND	20
20	GND	578	IO578	IO668	668	I2C4_CAM_PMU1_SDA_1V8	20
20	GND	579	IO579	IO669	669	GND	20
20	GND	580	IO580	IO670	670	GND	20
20	GND	581	IO581	IO671	671	GND	20
20	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	582	IO582	IO672	672	GND	20
20	GND	583	IO583	IO673	673	GND	20
20	50_TRX_ANT8_UHB_N79	584	IO584	IO674	674	GND	20
20	GND	585	IO585	IO675	675	GPIO_SCM_AOP_FROM_IMU_DATARDY	20
20	GND	586	IO586	IO676	676	GPIO_AP_CANARY1_LEG3	20
20	GND	587	IO587	IO677	677	GPIO_AP_CANARY1_LEG3	20
20	GND	588	IO588	IO678	678	SPI0_AOP_FROM_IMU_R1_MISO	20
20	GND	589	IO589	IO679	679	PP_STROBE_DRIVER_COOL_LED	20
20	GND	590	IO590	IO680	680	GND	20
20	GPIO_AP_CANARY1_LEG1	591	IO591	IO681	681	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	20
20	GND	592	IO592	IO682	682	PP_STROBE_DRIVER_COOL_LED	20
20	GND	593	IO593	IO683	683	GPIO_AP_CANARY1_LEG4	20
20	GPIO_AP_CANARY1_LEG1	594	IO594	IO684	684	GND	20
20	GND	595	IO595	IO685	685	GND	20
20	GND	596	IO596	IO686	686	GND	20
20	GND	597	IO597	IO687	687	SPI0_AOP_TO_IMU_R1_MOSI	20
20	GND	598	IO598	IO688	688	PP_STROBE_DRIVER_WARM_LED	20
20	GND	599	IO599	IO689	689	GPIO_AP_CANARY1_LEG4	20
20	GND	600	IO600	IO690	690	SPI0_AOP_TO_IMU_R1_SCLK	20
20	GND	601	IO601	IO691	691	PP_STROBE_DRIVER_WARM_LED	20
20	GND	602	IO602	IO692	692	GND	20
20	GND	603	IO603	IO693	693	GND	20
20	GND	604	IO604	IO694	694	GND	20
20	GPIO_AP_CANARY1_LEG2	605	IO605	IO695	695	GND	20
20	GND	606	IO606	IO696	696	GND	20
20	GND	607	IO607	IO697	697	GND	20
20	GND	608	IO608	IO698	698	GND	20
20	GND	609	IO609	IO699	699	GND	20
20	GND	610	IO610	IO700	700	GND	20
20	GND	611	IO611	IO701	701	GND	20
20	GND	612	IO612	IO702	702	GND	20
20	GPIO_AP_CANARY1_LEG2	613	IO613	IO703	703	GND	20
20	PP_LDO6_VIO_1V8	614	IO614	IO704	704	GND	20
20	GND	615	IO615	IO705	705	GND	20
20	GPIO_BB_TO_R1_COEX	616	IO616	IO706	706	GND	20
20	GND	617	IO617	IO707	707	GND	20
20	IO_BT_TO_R1_TIME_SYNC	618	IO618	IO708	708	GND	20
20	GND	619	IO619	IO709	709	GND	20
20	GPIO_WLAN_TO_R1_COEX	620	IO620	IO710	710	GND	20
20	GND	621	IO621	IO711	711	GND	20
20	GND	622	IO622	IO712	712	GND	20
20	GND	623	IO623	IO713	713	GPIO_AP_CANARY6_LEG4	20
20	GND	624	IO624	IO714	714	GND	20
20	50_TRX_ANT2_LB_LMB_MB_HB_L1	625	IO625	IO715	715	GND	20
20	GND	626	IO626	IO716	716	GND	20
20	50_LAA_RX_XCVR_DRX10	627	IO627	IO717	717	GPIO_AP_CANARY6_LEG4	20
20	GND	628	IO628	IO718	718	GND	20
20	GND	629	IO629	IO719	719	GND	20
20	SHIELD_RFFE5_SCLK_SDR	630	IO630	IO720	720	GPIO_AP_CANARY6_LEG3	20
				IO721	721	GPIO_AP_CANARY6_LEG3	20
				IO722	722	GND	20
				IO723	723	GND	20
				IO724	724	GND	20
				IO725	725	GND	20
				IO726	726	GND	20
				IO727	727	GND	20

ROOM=INTERPOSER

PAGE TITLE
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Interposer Aliases (1/4)

GND		
GND		
GND		
GND		
GND		
GND		
GPIO_AP_CANARY6_LEG2	GPIO_AP_CANARY6_LEG2	21
GND		
GND		
GPIO_AP_CANARY6_LEG2	GPIO_AP_CANARY6_LEG2	21
GND		
GND		
GND		
GND		
GPIO_AP_CANARY6_LEG1	GPIO_AP_CANARY6_LEG1	21
GPIO_AP_CANARY6_LEG1	GPIO_AP_CANARY6_LEG1	21
GND		
PP1V8_S2	PP1V8_S2	10 12 14 18 21 22 23
GND		
GND		
GND		
GND		
GND		
GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	9 14
GND		
GND		
GND		
IO_R1_TO_BB_LAA_SW_CTRL	IO_R1_TO_BB_LAA_SW_CTRL	23
GND		
IO_BT_TO_R1_WAKE	IO_BT_TO_R1_WAKE	22
GND		
GND		
GND		
PPVAR_RCAM_PVDD	PPVAR_RCAM_PVDD	8
GND		
GND		
GND		
GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	9
GND		
GPIO_BB_TO_R1_CH9_REQ	GPIO_BB_TO_R1_CH9_REQ	23
GND		
NTC_STROBE_MODULE	NTC_STROBE_MODULE	9
GND		
GND		
GPIO_AP_CANARY5_LEG1	GPIO_AP_CANARY5_LEG1	21
GND		
GPIO_AP_CANARY5_LEG1	GPIO_AP_CANARY5_LEG1	21
GND		
GND		
GND		
GPIO_AP_CANARY5_LEG2	GPIO_AP_CANARY5_LEG2	21
GND		
GND		
GPIO_AP_CANARY5_LEG2	GPIO_AP_CANARY5_LEG2	21
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GPIO_AP_CANARY5_LEG3	GPIO_AP_CANARY5_LEG3	21
GND		
GND		
GPIO_AP_CANARY5_LEG3	GPIO_AP_CANARY5_LEG3	21
GND		
GPIO_AP_CANARY5_LEG4	GPIO_AP_CANARY5_LEG4	21
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GPIO_AP_CANARY5_LEG4	GPIO_AP_CANARY5_LEG4	21
GND		
GND		
PP_VDD_MAIN_PENINSULA	PP_VDD_MAIN_PENINSULA	17 21 22 23

MAKE_BASE=TRUE

GND		
PP_VDD_MAIN_PENINSULA	PP_VDD_MAIN_PENINSULA	17 21 22 23
GND		
PP_VDD_MAIN_PENINSULA	PP_VDD_MAIN_PENINSULA	17 21 22 23
GND		
PP_VDD_MAIN_PENINSULA	PP_VDD_MAIN_PENINSULA	17 21 22 23
GND		
GND	GND	21
GND		
GND		
GND		
CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	22
GND		
PP_VDD_BOOST_NORTH_PA	PP_VDD_BOOST_NORTH_PA	21 23
GND		
PP1V2_S4	PP1V2_S4	22 23
GND		
GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A	22
GND		
PP1V8_S4	PP1V8_S4	22 23
GND		
RFFE_WLAN_TO_UAT_2G_FEM_RST_L	RFFE_WLAN_TO_UAT_2G_FEM_RST_L	22
GND		
RFFE_WLAN_TO_UAT_5G_FEM_RST_L	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	22
GND		
GPIO_SE_TO_BT_PKT_RDY	GPIO_SE_TO_BT_PKT_RDY	22
GND		
GND		
GND		
I2C_BT_TO_NFC_SCL	I2C_BT_TO_NFC_SCL	22
GND		
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	22
GND		
GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	23
GND		
GND		
GND		
I2C_BT_TO_NFC_SDA	I2C_BT_TO_NFC_SDA	22
GND		
GPIO_AP_FROM_WLAN_TIME_SYNC	GPIO_AP_FROM_WLAN_TIME_SYNC	22
GND		
GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	22
GND		
GND		
GND		
GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	22
GND		
GPIO_AP_TO_BB_PEAK_PWR_IND	GPIO_AP_TO_BB_PEAK_PWR_IND	23
GND		
SWD_AP_BI_BB_SWDIO	SWD_AP_BI_BB_SWDIO	23
GND		
GND		
GND		
GPIO_AP_FROM_BB_RESET_DETECT_L	GPIO_AP_FROM_BB_RESET_DETECT_L	23
GND		
SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	22
GND		
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	22
GND		
GND		
GND		
GPIO_AP_FROM_BT_AUDIO_SYNC	GPIO_AP_FROM_BT_AUDIO_SYNC	22
GND		
GPIO_AP_TO_BB_TIME_MARK	GPIO_AP_TO_BB_TIME_MARK	23
GND		
NTC_RADIO_BB_P	NTC_RADIO_BB_P	7
GND		
GND		
GND		
UART1_AOP_FROM_BB_RXD	UART1_AOP_FROM_BB_RXD	23
GND		
UART1_AOP_TO_BB_TXD	UART1_AOP_TO_BB_TXD	23
GND		
GPIO_AOP_TO_BB_FORCE_PWM	GPIO_AOP_TO_BB_FORCE_PWM	23
GND		
GND		
GND		
PP_VDD_RF_1V2	PP_VDD_RF_1V2	23
GND		
GND		
GND		
GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B	22
GND		
GND		
GND		
PP_VDD_BOOST_BBPMU	PP_VDD_BOOST_BBPMU	21 23
GND		
GND		
GND		
PP_VDD_MAIN_QET_BBPMU_APTL	PP_VDD_MAIN_QET_BBPMU_APTL	18 19 21

MAKE_BASE=TRUE

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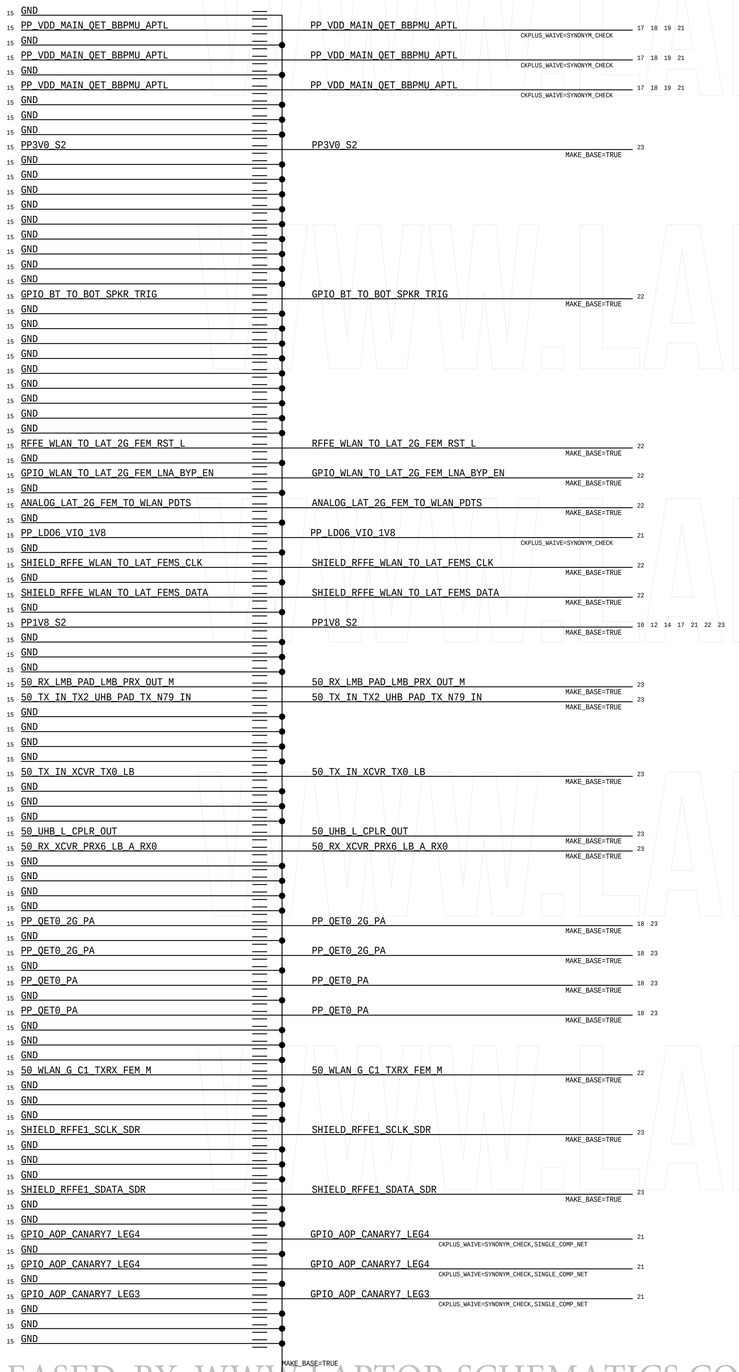

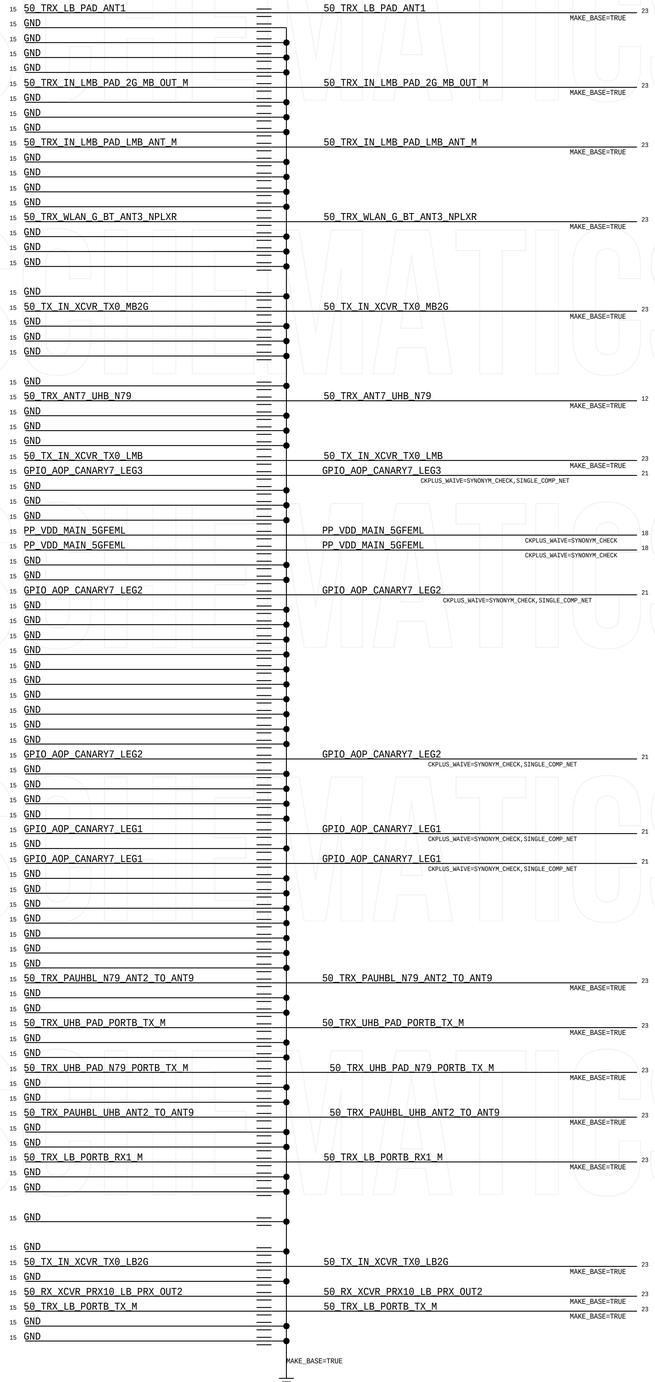

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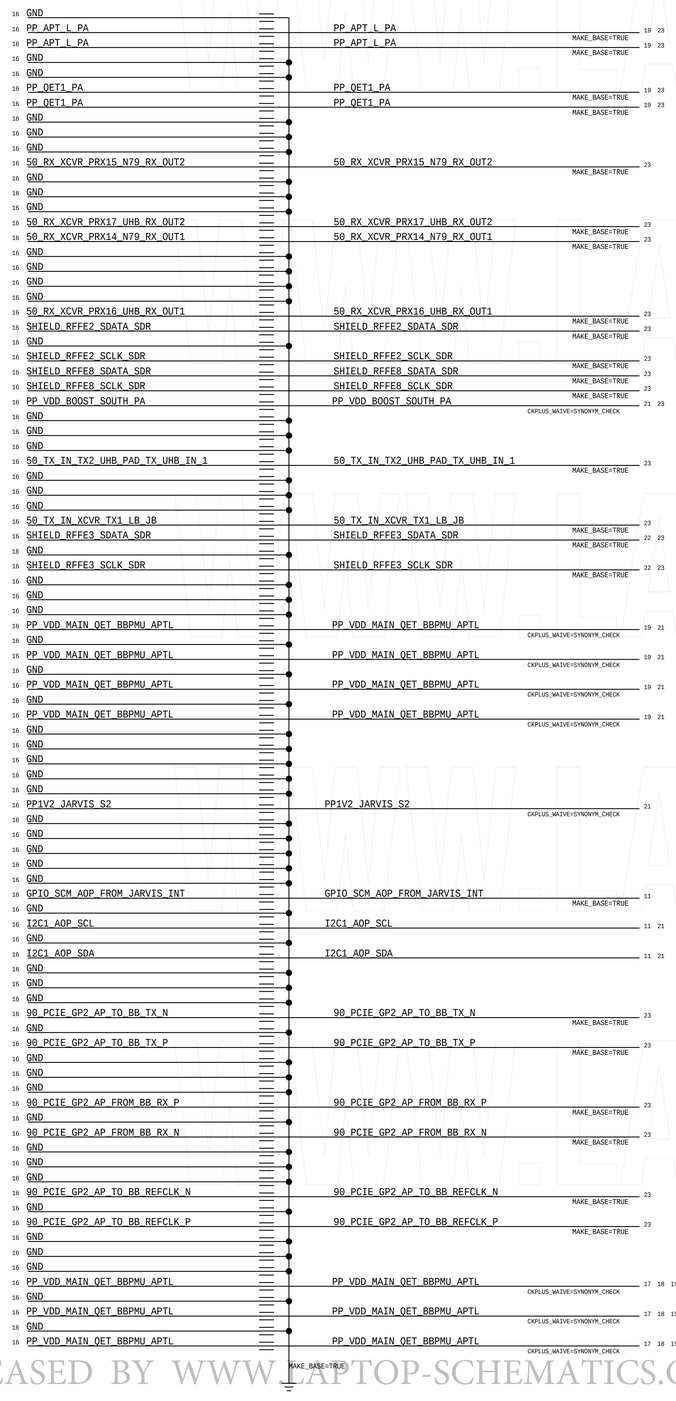

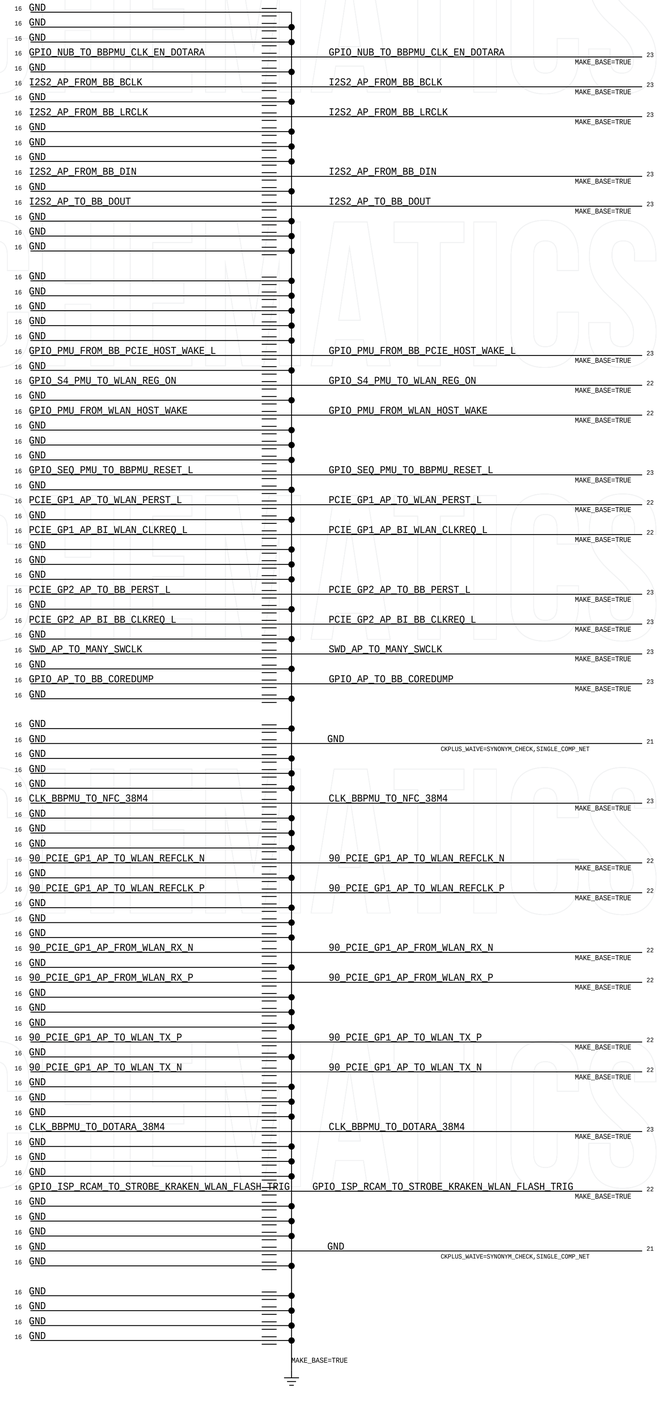

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Interposer Aliases (4/4)

GND		
GND		
50_WLAN_A_C0_TXRX_FEM_M	50_WLAN_A_C0_TXRX_FEM_M	MAKE_BASE=TRUE
GND		
GND		
50_WLAN_G_C0_TXRX_FEM_M	50_WLAN_G_C0_TXRX_FEM_M	MAKE_BASE=TRUE
GND		
GND		
50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	MAKE_BASE=TRUE
GND		
GND		
50_TRX_PAUHBU_N79_ANT1_TO_ANT4	50_TRX_PAUHBU_N79_ANT1_TO_ANT4	MAKE_BASE=TRUE
GND		
GND		
GND		
GND		
GND		
GND		
IO_NFC_TO_BBPMU_CLKREQ	IO_NFC_TO_BBPMU_CLKREQ	MAKE_BASE=TRUE
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE
GND		
GND		
GND		
GND		
GND		
GND		
GND		
50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	MAKE_BASE=TRUE
GND		
50_TRX_ANT8_UHB_N79	50_TRX_ANT8_UHB_N79	MAKE_BASE=TRUE
GND		
GND		
GND		
GND		
GND		
GND		
GPIO_AP_CANARY1_LEG1	GPIO_AP_CANARY1_LEG1	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GPIO_AP_CANARY1_LEG1	GPIO_AP_CANARY1_LEG1	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GPIO_AP_CANARY1_LEG2	GPIO_AP_CANARY1_LEG2	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GPIO_AP_CANARY1_LEG2	GPIO_AP_CANARY1_LEG2	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
PP_LDO6_VIO_1V8	PP_LDO6_VIO_1V8	CKPLUS_WAIVE=SYNONYM_CHECK
GND		
GPIO_BB_TO_R1_COEX	GPIO_BB_TO_R1_COEX	MAKE_BASE=TRUE
GND		
IO_BT_TO_R1_TIME_SYNC	IO_BT_TO_R1_TIME_SYNC	MAKE_BASE=TRUE
GND		
GPIO_WLAN_TO_R1_COEX	GPIO_WLAN_TO_R1_COEX	MAKE_BASE=TRUE
GND		
GND		
GND		
GND		
50_TRX_ANT2_LB_LMB_MB_HB_L1	50_TRX_ANT2_LB_LMB_MB_HB_L1	MAKE_BASE=TRUE
GND		
50_LAA_RX_XCVR_DRX10	50_LAA_RX_XCVR_DRX10	MAKE_BASE=TRUE
GND		
GND		
SHIELD_RFFE5_SCLK_SDR	SHIELD_RFFE5_SCLK_SDR	MAKE_BASE=TRUE

GND		
SHIELD_RFFE5_SDATA_SDR	SHIELD_RFFE5_SDATA_SDR	MAKE_BASE=TRUE
GND		
GND		
GND		
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	MAKE_BASE=TRUE
GND		
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	MAKE_BASE=TRUE
GND		
GND		
GND		
UAT_SUBUS_B	UAT_SUBUS_B	MAKE_BASE=TRUE
GND		
UAT_SUBUS_A	UAT_SUBUS_A	MAKE_BASE=TRUE
GND		
GND		
GND		
NTC_RADIO_PA_P	NTC_RADIO_PA_P	MAKE_BASE=TRUE
GND		
UAT_TUNER_TO_R1_STATE	UAT_TUNER_TO_R1_STATE	MAKE_BASE=TRUE
GND		
GPIO_R1_TO_BB_CH9_COEX	GPIO_R1_TO_BB_CH9_COEX	MAKE_BASE=TRUE
GND		
GND		
GND		
GPIO_R1_TO_WLAN_COEX	GPIO_R1_TO_WLAN_COEX	MAKE_BASE=TRUE
GND		
PP1V2_S2	PP1V2_S2	MAKE_BASE=TRUE
GND		
GND		
GND		
GPIO_CAM_PMU1_TO_PVDD_RESET_L	GPIO_CAM_PMU1_TO_PVDD_RESET_L	MAKE_BASE=TRUE
GND		
I2C4_CAM_PMU1_SCL_1V8	I2C4_CAM_PMU1_SCL_1V8	CKPLUS_WAIVE=SYNONYM_CHECK,I2C_PULLUP
GND		
GND		
GND		
I2C4_CAM_PMU1_SDA_1V8	I2C4_CAM_PMU1_SDA_1V8	CKPLUS_WAIVE=SYNONYM_CHECK,I2C_PULLUP
GND		
GND		
GND		
GND		
GND		
GND		
GPIO_SCM_AOP_FROM_IMU_DATARDY	GPIO_SCM_AOP_FROM_IMU_DATARDY	MAKE_BASE=TRUE
GPIO_AP_CANARY1_LEG3	GPIO_AP_CANARY1_LEG3	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GPIO_AP_CANARY1_LEG3	GPIO_AP_CANARY1_LEG3	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
SPI0_AOP_FROM_IMU_R1_MISO	SPI0_AOP_FROM_IMU_R1_MISO	MAKE_BASE=TRUE
PP_STROBE_DRIVER_COOL_LED	PP_STROBE_DRIVER_COOL_LED	VOLTAGE=5.2 MAKE_BASE=TRUE
GND		
GPIO_SCM_AOP_TO_IMU_SPI_CS_L	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	MAKE_BASE=TRUE
PP_STROBE_DRIVER_COOL_LED	PP_STROBE_DRIVER_COOL_LED	MAKE_BASE=TRUE
GPIO_AP_CANARY1_LEG4	GPIO_AP_CANARY1_LEG4	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
SPI0_AOP_TO_IMU_R1_MOSI	SPI0_AOP_TO_IMU_R1_MOSI	MAKE_BASE=TRUE
PP_STROBE_DRIVER_WARM_LED	PP_STROBE_DRIVER_WARM_LED	MAKE_BASE=TRUE
GPIO_AP_CANARY1_LEG4	GPIO_AP_CANARY1_LEG4	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
SPI0_AOP_TO_IMU_R1_SCLK	SPI0_AOP_TO_IMU_R1_SCLK	MAKE_BASE=TRUE
PP_STROBE_DRIVER_WARM_LED	PP_STROBE_DRIVER_WARM_LED	VOLTAGE=5.2 MAKE_BASE=TRUE
GND		
GND		
GND		
GND	GND	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND		
GND	GND	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
GND		
GPIO_AP_CANARY6_LEG4	GPIO_AP_CANARY6_LEG4	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
GPIO_AP_CANARY6_LEG4	GPIO_AP_CANARY6_LEG4	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GPIO_AP_CANARY6_LEG3	GPIO_AP_CANARY6_LEG3	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GPIO_AP_CANARY6_LEG3	GPIO_AP_CANARY6_LEG3	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND		
GND		
GND		
GND		
GND		
GND		

MAKE_BASE=TRUE

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Kobol Aliases (Bot Only)

23 22 21 18 17 14 12 10 — PP1V8_S2 — MAKE_BASE=TRUE — PP1V8_S2 — 10
23 20 10 — PP1V2_S2 — MAKE_BASE=TRUE — PP1V2_S2

Lex Aliases (Bot Only)

23 22 21 17 — PP_VDD_MAIN_PENINSULA — MAKE_BASE=TRUE — PP_VDD_MAIN_PENINSULA — 8
21 — I2C4_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C4_CAM_PMU1_SCL_1V8 — 8 20
21 — I2C4_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C4_CAM_PMU1_SDA_1V8 — 8 20
NC_AMUX_RCAM_PVDD — MAKE_BASE=TRUE — NC_AMUX_RCAM_PVDD — 8

AMUX tapped from top board interposer connection of PPVAR_RCAM_PVDD

Yeti Aliases (Bot Only)

9 — PP_VDD_MAIN_PENINSULA — PP_VDD_MAIN_PENINSULA — 17 21 22 23
MAKE_BASE=TRUE

9 — I2C4_CAM_PMU1_SDA_1V8 — I2C4_CAM_PMU1_SDA_1V8 — 21
MAKE_BASE=TRUE
CKPLUS_WAIVE=SYNONYM_CHECK,I2C_PULLUP

9 — I2C4_CAM_PMU1_SCL_1V8 — I2C4_CAM_PMU1_SCL_1V8 — 21
MAKE_BASE=TRUE
CKPLUS_WAIVE=SYNONYM_CHECK,I2C_PULLUP

Jarvis Aliases

11 — PP1V8_S2 — PP1V8_S2 — VOLTAGE=1.8 MAKE_BASE=TRUE — 10 12 14 17 18 21 22 23
11 — PP1V2_JARVIS_S2 — PP1V2_JARVIS_S2 — VOLTAGE=1.2 MAKE_BASE=TRUE — 19
19 11 — I2C1_AOP_SDA — I2C1_AOP_SDA — MAKE_BASE=TRUE
19 11 — I2C1_AOP_SCL — I2C1_AOP_SCL — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE
CKPLUS_WAIVE=I2C_PULLUP

Power Rail Splits (Bottom Board)

23 — PP_VDD_MAIN_QET_BBPMU_APTL — MAKE_BASE=TRUE — PP_VDD_MAIN_QET_BBPMU_APTL — 17 18 19
PP_VDD_MAIN_QET_BBPMU_APTL — 19

23 22 21 17 — PP_VDD_MAIN_PENINSULA — MAKE_BASE=TRUE — PP_VDD_MAIN_PENINSULA — 17 21 22 23

22 21 18 — PP_VDD_MAIN_5GFEML — MAKE_BASE=TRUE — PP_VDD_MAIN_5GFEML — 18 21 22

23 21 17 — PP_VDD_BOOST_NORTH_PA — MAKE_BASE=TRUE — PP_VDD_BOOST_NORTH_PA — 17 21 23

23 21 19 — PP_VDD_BOOST_SOUTH_PA — MAKE_BASE=TRUE — PP_VDD_BOOST_SOUTH_PA — 19 21 23

23 21 17 — PP_VDD_BOOST_BBPMU — MAKE_BASE=TRUE — PP_VDD_BOOST_BBPMU — 17 21 23

Power Rail Splits (Top Board)

23 22 — PP_LDO6_VIO_1V8 — MAKE_BASE=TRUE — PP_LDO6_VIO_1V8 — 18
PP_LDO6_VIO_1V8 — 20

Canary (single-pin)

19 — GND — CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
17 — GND — CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
19 — GND — CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET — MAKE_BASE=TRUE

Canary (daisy-chain)

21 — GPIO_AP_CANARY1_LEG1 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG1 — 20
21 — GPIO_AP_CANARY1_LEG1 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG1 — 20
21 — GPIO_AP_CANARY1_LEG2 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG2 — 20
21 — GPIO_AP_CANARY1_LEG2 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG2 — 20
21 — GPIO_AP_CANARY1_LEG3 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG3 — 20
21 — GPIO_AP_CANARY1_LEG3 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG3 — 20
21 — GPIO_AP_CANARY1_LEG4 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG4 — 20
21 — GPIO_AP_CANARY1_LEG4 — MAKE_BASE=TRUE — GPIO_AP_CANARY1_LEG4 — 20
GND — 20
MAKE_BASE=TRUE

21 — GPIO_AP_CANARY6_LEG1 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG1 — 17
21 — GPIO_AP_CANARY6_LEG1 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG1 — 17
21 — GPIO_AP_CANARY6_LEG2 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG2 — 17
21 — GPIO_AP_CANARY6_LEG2 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG2 — 17
21 — GPIO_AP_CANARY6_LEG3 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG3 — 20
21 — GPIO_AP_CANARY6_LEG3 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG3 — 20
21 — GPIO_AP_CANARY6_LEG4 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG4 — 20
21 — GPIO_AP_CANARY6_LEG4 — MAKE_BASE=TRUE — GPIO_AP_CANARY6_LEG4 — 20
GND — 20
MAKE_BASE=TRUE

21 — GPIO_AP_CANARY5_LEG1 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG1 — 17
21 — GPIO_AP_CANARY5_LEG1 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG1 — 17
21 — GPIO_AP_CANARY5_LEG2 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG2 — 17
21 — GPIO_AP_CANARY5_LEG2 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG2 — 17
21 — GPIO_AP_CANARY5_LEG3 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG3 — 17
21 — GPIO_AP_CANARY5_LEG3 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG3 — 17
21 — GPIO_AP_CANARY5_LEG4 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG4 — 17
21 — GPIO_AP_CANARY5_LEG4 — MAKE_BASE=TRUE — GPIO_AP_CANARY5_LEG4 — 17

21 — GPIO_AOP_CANARY7_LEG1 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG1 — 18
21 — GPIO_AOP_CANARY7_LEG1 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG1 — 18
21 — GPIO_AOP_CANARY7_LEG2 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG2 — 18
21 — GPIO_AOP_CANARY7_LEG2 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG2 — 18
21 — GPIO_AOP_CANARY7_LEG3 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG3 — 18
21 — GPIO_AOP_CANARY7_LEG3 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG3 — 18
21 — GPIO_AOP_CANARY7_LEG4 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG4 — 18
21 — GPIO_AOP_CANARY7_LEG4 — MAKE_BASE=TRUE — GPIO_AOP_CANARY7_LEG4 — 18

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WiFi Hierarchy

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Series-R

rdar://problem/53460687

R15000
33.2
1%
1/32W
MF
01005
ROOM=WLAN

17 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA — 1 — 2 — SPMI0_EVENTS_AOP_BI_WLAN_DATA_R 22 63

63 22 19 GPIO_S4_PMU_TO_WLAN_REG_ON

R15001
200K
1%
1/32W
MF
01005
ROOM=WLAN

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POWER

23 21 17 PP_VDD_MAIN_PENINSULA	PP_VDD_MAIN_PENINSULA	
64 21 18 PP_VDD_MAIN_5GFEML	PP_VDD_MAIN_5GFEML	
64 23 21 18 17 14 12 10 PP1V8_S2	PP1V8_S2	
63 23 17 PP1V8_S4	PP1V8_S4	
63 23 17 PP1V2_S4	PP1V2_S4	

R1

BT_TO_R1_TIME_SYNC	IO_BT_TO_R1_TIME_SYNC 20 63
BT_TO_R1_WAKE	IO_BT_TO_R1_WAKE 17 63
WLAN_TO_R1_COEX	GPIO_WLAN_TO_R1_COEX 20 63
R1_TO_WLAN_COEX	GPIO_R1_TO_WLAN_COEX 20 63

PMU

63 17 CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_PMU_TO_WLAN_R1_32K
63 22 19 GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO_PMU_TO_WLAN_REG_ON
63 19 GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE

SE

I2C_BT_TO_SE_SCL	I2C_BT_TO_NFC_SCL 17 63
I2C_BT_TO_SE_SDA	I2C_BT_TO_NFC_SDA 17 63
IO_SE_TO_BT_PKT_READY	GPIO_SE_TO_BT_PKT_RDY 17 63

PCIE

63 19 90_PCIE_GP1_AP_FROM_WLAN_RX_P	90_PCIE_WLAN_TO_AP_TX_P
63 19 90_PCIE_GP1_AP_FROM_WLAN_RX_N	90_PCIE_WLAN_TO_AP_TX_N
63 19 90_PCIE_GP1_AP_TO_WLAN_TX_P	90_PCIE_AP_TO_WLAN_TX_P
63 19 90_PCIE_GP1_AP_TO_WLAN_TX_N	90_PCIE_AP_TO_WLAN_TX_N
63 19 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	90_PCIE_AP_TO_WLAN_REFCLK_P
63 19 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	90_PCIE_AP_TO_WLAN_REFCLK_N
63 19 PCIE_GP1_AP_TO_WLAN_PERST_L	PCIE_AP_TO_WLAN_PERST_1V2_L
63 19 PCIE_GP1_AP_BI_WLAN_CLKREQ_L	PCIE_AP_BI_WLAN_CLKREQ_L

WLAN_UAT

50_WLAN_A_C0_TXRX_FEM_M	50_WLAN_A_C0_TXRX_FEM_M 20 63
RFFE_WLAN_TO_UAT_5G_FEM_RST_L	RFFE_WLAN_TO_UAT_5G_FEM_RST_L 17 63
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK 20 23 63
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA 20 23 63
GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN 17 63
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS 17 63

SPMI

63 22 SPMI0_EVENTS_AOP_BI_WLAN_DATA_R	SPMI_EVENTS_AOP_TO_WLAN_NFC_DATA
63 17 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	SPMI_EVENTS_AOP_TO_WLAN_NFC_CLK

LAA_LAT

PP_VIO_RFFE0_XCVR_1V8	PP_LDO6_VIO_1V8 21 23 64
RFFE0_XCVR_SCLK	SHIELD_RFFE3_SCLK_SDR 19 23 64
RFFE0_XCVR_SDATA	SHIELD_RFFE3_SDATA_SDR 19 23 64
50_LAA_RX_XCVR_PRX12	50_RX_LAA_XCVR_PRX12 23 64

ANT

50_WLAN_A_LAA_ANT5	50_WLAN_A_LAA_ANT5 12 64

2.4 GHZ UAT

50_WLAN_G_C0_TXRX_FEM_M	50_WLAN_G_C0_TXRX_FEM_M 20 63
RFFE_WLAN_TO_UAT_2G_FEM_RST_L	RFFE_WLAN_TO_UAT_2G_FEM_RST_L 17 63
GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN 17 63
ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS 20 63

CONTEXT

63 19 GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	WLAN_TO_AP_TIME_SYNC_1V2
63 17 GPIO_AP_FROM_WLAN_TIME_SYNC	BT_TO_AP_AUDIO_SYNC
63 17 GPIO_AP_FROM_BT_AUDIO_SYNC	BT_TO_ISP_STROBE_SYNC

2.4 GHZ LAT

50_WLAN_G_C1_TXRX_FEM_M	50_WLAN_G_C1_TXRX_FEM_M 18 63
RFFE_WLAN_TO_LAT_2G_FEM_RST_L	RFFE_WLAN_TO_LAT_2G_FEM_RST_L 18 63
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK 18 63
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA 18 63
GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN 18 63
ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	ANALOG_LAT_2G_FEM_TO_WLAN_PDTS 18 63

BOT_SPK

63 17 GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B
63 17 GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A

COEX

63 18 GPIO_BT_TO_BOT_SPKR_TRIG	BT_TO_BOT_SPK_TRIG

UART_BB_TO_WLAN_COEX_1V2	UART_COEX_BB_TO_WLAN_TXD 23 63
UART_WLAN_TO_BB_COEX_1V2	UART_COEX_BB_FROM_WLAN_RXD 23 63

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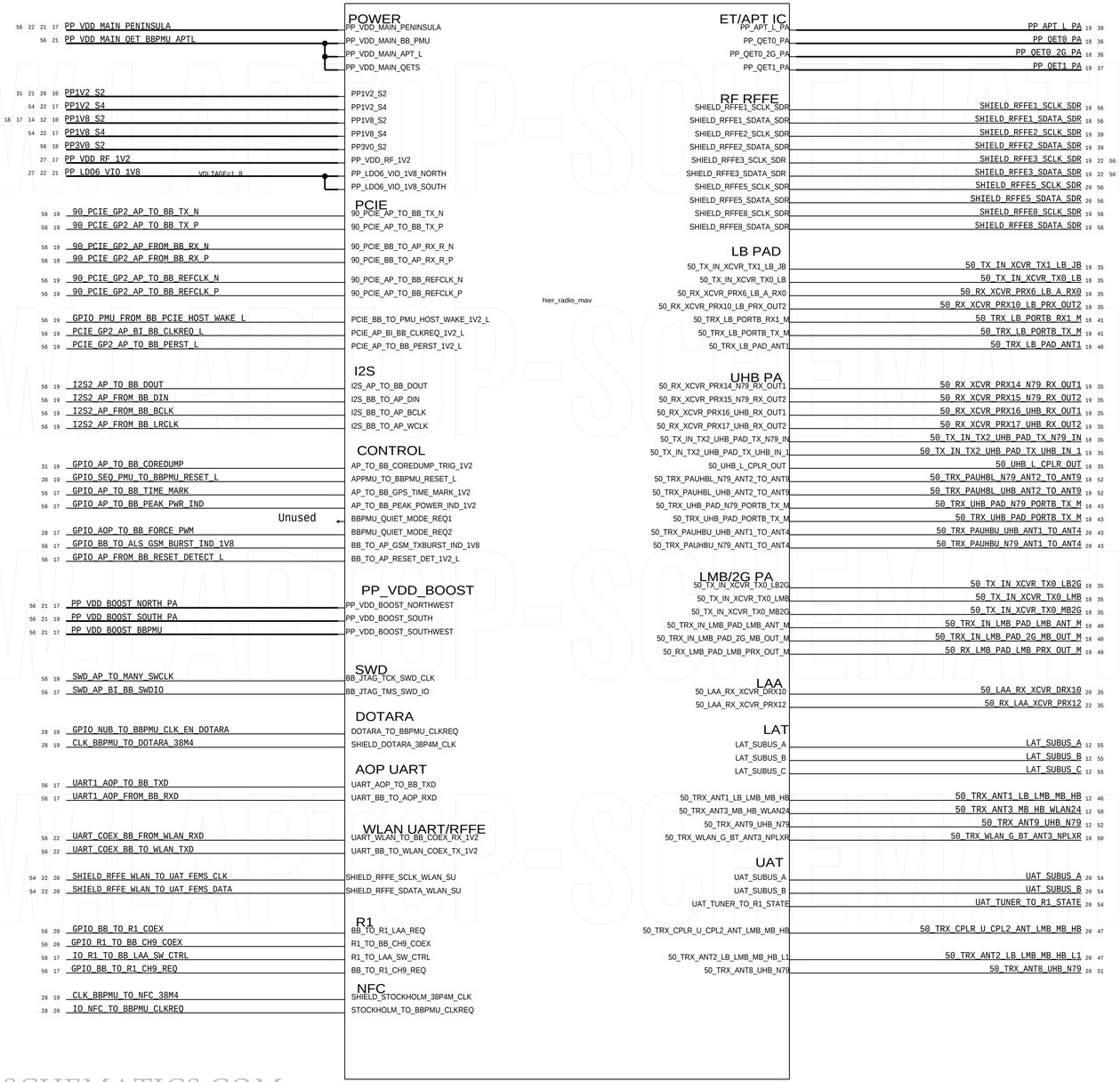

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28	6	PMIC: CLOCKS & CONTROL		07/30/2019
29	7	BB: POWER		08/22/2019
30	8	BB: GND		07/30/2019
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POWER

PP_VDD_MAIN_PENINSULA	IN	23 56 57
PP_VDD_MAIN_QET_BBPMU_APTL	IN	23 56 57
PP_VDD_MAIN_QET_BBPMU_APTL	IN	23 57
PP_VDD_MAIN_QET_BBPMU_APTL	IN	23 56 57 58
PP_VDD_BOOST_NORTH_PA	IN	23 56 57
PP_VDD_BOOST_BBPMU	IN	23 56 57
PP_VDD_BOOST_SOUTH_PA	IN	23 56 57
PP1V2_S2	IN	23 31
PP1V2_S4	IN	23 54
PP1V8_S2	IN	23 55 58
PP1V8_S4	IN	23 54
PP3V0_S2	IN	23 35 56 58
PP_LDO6_VIO_1V8	OUT	57
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PCIE

GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	OUT	23 31 56 58
PCIE_GP2_AP_TO_BB_PERST_L	IN	23 31 56
PCIE_GP2_AP_BI_BB_CLKREQ_L	IO	23 31 56 58
90_PCIE_GP2_AP_FROM_BB_RX_P	OUT	23 31 56
90_PCIE_GP2_AP_FROM_BB_RX_N	OUT	23 31 56
90_PCIE_GP2_AP_TO_BB_TX_P	IN	23 31 56
90_PCIE_GP2_AP_TO_BB_TX_N	IN	23 31 56
90_PCIE_GP2_AP_TO_BB_REFCLK_P	OUT	23 31 56
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I2S

I2S2_AP_FROM_BB_DIN	OUT	23 31 56
I2S2_AP_TO_BB_DOUT	IN	23 31 56
I2S2_AP_FROM_BB_BCLK	OUT	23 31 56
I2S2_AP_FROM_BB_LRCLK	OUT	23 31 56

CONTROL

GPIO_AP_FROM_BB_RESET_DETECT_L	OUT	23 31 56
GPIO_SEQ_PMU_TO_BBPMU_RESET_L	IN	23 28 56 58
GPIO_AP_TO_BB_COREDUMP	IN	23 31
GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	OUT	23 31 56
BBPMU_QUIET_MODE_REQ1	IN	28 56
GPIO_AOP_TO_BB_FORCE_PWM	IN	23 28 56
GPIO_AP_TO_BB_TIME_MARK	IN	23 31 56
GPIO_AP_TO_BB_PEAK_PWR_IND	IN	23 31 56

SWD

SWD_AP_TO_MANY_SWCLK	IN	23 31 56
SWD_AP_BI_BB_SWDIO	IO	23 31 56

DOTARA

GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	IN	23 28 56
CLK_BBPMU_TO_DOTARA_38M4	OUT	23 28 56

AOP UART

UART1_AOP_TO_BB_TXD	IN	23 31 56
UART1_AOP_FROM_BB_RXD	OUT	23 31 56

WLAN UART/RFFE

UART_COEX_BB_TO_WLAN_TXD	OUT	23 31 56
UART_COEX_BB_FROM_WLAN_RXD	IN	23 31 56
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	IN	23 54
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	IO	23 54

R1

GPIO_BB_TO_R1_COEX	OUT	23 31 56
GPIO_BB_TO_R1_CH9_REQ	OUT	23 31 56
GPIO_R1_TO_BB_CH9_COEX	IN	23 31 56
IO_R1_TO_BB_LAA_SW_CTRL	IN	23 31 56

NFC

CLK_BBPMU_TO_NFC_38M4	OUT	23 28 56
IO_NFC_TO_BBPMU_CLKREQ	IN	23 28 56

ET/APT IC

PP_APT_L_PA	VOLTAGE=5.5V	OUT	23 39
PP_QET0_PA	VOLTAGE=5	OUT	23 36 40
PP_QET0_2G_PA	VOLTAGE=5	OUT	23 36
PP_QET1_PA	VOLTAGE=5	OUT	23 37

RF RFFE

SHIELD_RFFE1_SCLK_SDR	OUT	23 35 36 40 46 56
SHIELD_RFFE1_SDATA_SDR	IO	23 35 36 40 46 56
SHIELD_RFFE2_SCLK_SDR	OUT	23 35 39 56
SHIELD_RFFE2_SDATA_SDR	IO	23 35 39 56
SHIELD_RFFE3_SCLK_SDR	OUT	23 35 40 44 56
SHIELD_RFFE3_SDATA_SDR	IO	23 35 40 44 56
SHIELD_RFFE5_SCLK_SDR	OUT	23 35 41 42 43 45 56
SHIELD_RFFE5_SDATA_SDR	IO	23 35 41 42 43 45 56
SHIELD_RFFE8_SCLK_SDR	OUT	23 35 37 56
SHIELD_RFFE8_SDATA_SDR	IO	23 35 37 56

LB PAD

50_RX_XCVR_PRX6_LB_A_RX0	IN	23 35
50_RX_XCVR_PRX10_LB_PRX_OUT2	IN	23 35
50_TX_IN_XCVR_TX1_LB_JB	OUT	23 35
50_TX_IN_XCVR_TX0_LB	OUT	23 35
50_TRX_LB_PORTB_RX1_M	IN	23 41
50_TRX_LB_PORTB_TX_M	IO	23 41
50_TRX_LB_PAD_ANT1	OUT	23 46

UHB PA (LAT)

50_RX_XCVR_PRX14_N79_RX_OUT1	IN	23 35
50_RX_XCVR_PRX15_N79_RX_OUT2	IN	23 35
50_RX_XCVR_PRX16_UHB_RX_OUT1	IN	23 35
50_RX_XCVR_PRX17_UHB_RX_OUT2	IN	23 35
50_TX_IN_TX2_UHB_PAD_TX_N79_IN	OUT	23 35
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	OUT	23 35
50_UHB_L_CPLR_OUT	IN	23 35
50_TRX_UHB_PAD_PORTB_TX_M	IO	23 43
50_TRX_UHB_PAD_N79_PORTB_TX_M	IO	23 43
50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	IO	23 52
50_TRX_PAUHBL_N79_ANT2_TO_ANT9	IO	23 52
50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	IO	23 43
50_TRX_PAUHBU_N79_ANT1_TO_ANT4	IO	23 43

LAA

50_LAA_RX_XCVR_DRX10	IN	23 35
50_RX_LAA_XCVR_PRX12	IN	23 35

LAT

LAT_SUBUS_A	OUT	23 55
LAT_SUBUS_B	OUT	23 55
LAT_SUBUS_C	OUT	23 55
50_TRX_ANT1_LB_LMB_MB_HB	IO	23 46
50_TRX_ANT3_MB_HB_WLAN24	IO	23 50
50_TRX_ANT9_UHB_N79	IO	23 52
50_TRX_WLAN_G_BT_ANT3_NPLXR	IO	23 50

UAT

UAT_SUBUS_A	OUT	23 54
UAT_SUBUS_B	OUT	23 54
UAT_TUNER_TO_R1_STATE	OUT	23 54
50_TRX_ANT2_LB_LMB_MB_HB_L1	OUT	23 47
50_TRX_ANT8_UHB_N79	IO	23 51
50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	OUT	23 47

LMB/2G PAD

50_TX_IN_XCVR_TX0_LB2G	OUT	23 35
50_TX_IN_XCVR_TX0_LMB	OUT	23 35
50_TX_IN_XCVR_TX0_MB2G	OUT	23 35
50_TRX_IN_LMB_PAD_LMB_ANT_M	OUT	23 40
50_TRX_IN_LMB_PAD_2G_MB_OUT_M	OUT	23 40
50_RX_LMB_PAD_LMB_PRX_OUT_M	IO	23 40

SCH #: 951-10914

FRONT PAGE

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BOM TABLES AND CONSTRAINTS

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ALT TABLES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00250	197S00249	?	Y601_E	TXC,38.4MHZ,8PF,1612

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01273	152S01227	?	L401_E	TAIYO,0.47UH,4.8A
152S01273	152S01227	?	L402_E	TAIYO,0.47UH,4.8A
152S01228	152S01120	?	L405_E	SEMCO,1.0UH,3.4A
152S01273	152S01227	?	L406_E	TAIYO,0.47UH,4.8A
152S01227	152S01273	?	L407_E	SEMCO,0.47UH,4.9A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00013	335S0894	?	EEPROM_E	EEPROM,8KBIT,I2C

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S00050	1	RES,MF,5.6K OHM,1%,1/32W,01005	R630_E	RF_SKU:WW+KOLKATA
118S0730	1	RES,MF,12K OHM,1%,1/32W,01005	R630_E	RF_SKU:WW
118S00088	1	RES,MF,19.1K OHM,1%,1/32W,01005	R630_E	RF_SKU:ROW
353S02396	1	IC,LB DSM,WW,MCD,LMRXFNJB-K79,DSLGA20	DSM_LB_E	RF_SKU:WW&RF_SKU:WW+KOLKATA
353S02397	1	IC,LB DSM,ROW,MCD,LMRXFNJB-K83,DSLGA20	DSM_LB_E	RF_SKU:ROW
353S02391	1	IC,HB TX DSM,WW,HFQTWLQFA-580,DSLGA61	DSM_HB_E	RF_SKU:WW&RF_SKU:WW+KOLKATA
353S02392	1	IC,HB TX DSM,ROW,HFQTWLQFA-583,DSLGA61	DSM_HB_E	RF_SKU:ROW
118S00122	1	RES,MF,27K OHM,1%,1/32W,01005	R631_E	BOARD_REV:PROTO2
118S00193	1	RES,MF,36.5K OHM,1%,1/32W,01005	R631_E	BOARD_REV:EVT
118S0868	1	RES,MF,47.5K OHM,1%,1/32W,01005	R631_E	BOARD_REV:CRB
118S00136	1	RES,MF,60.4K OHM,1%,1/32W,01005	R631_E	BOARD_REV:DVT
118S0768	1	RES,MF,75K OHM,1%,1/32W,01005	R631_E	BOARD_REV:PVT

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BB PMU: SMPS

SMPS INPUT CAPS

PP_VDD_MAIN_QET_BBPMU_APTL
MAKE_BASE=TRUE
C401_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU
C406_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU
C402_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU
C405_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU
C412_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU
C407_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU
C427_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU
C403_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU
C404_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU
GND
SHARE S7 INPUT POWER ROUTES WITH S5 CAP
C409_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU
C411_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU
C413_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU
C414_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU

PMX_REF_BYP
132S0316
C509_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=BBPMU
PMX_REF_BYP_GND
XW407_E SHORT-10L-0.1MM-SM ROOM=BBPMU

PART_NUMBER=338S00620
ROOM=BBPMU
UBBPMU_E
PMX55-0
FOWPSP
SYM 5 OF 6
VREG1

REF_BYP	32
REF_GND	49
VDD_S1	137, 138
VDD_S2	59, 68
VDD_S3	144, 145
VDD_S4	76, 77, 85
VDD_S5	1, 10
VDD_S6	78, 87
VDD_S7	3, 11
VDD_S8	61, 69

PART_NUMBER=338S00620
ROOM=BBPMU
UBBPMU_E
PMX55-0
FOWPSP
SYM 3 OF 6

GND	112, 121	GND_S1	
GND	42, 43	GND_S2	
GND	119, 127	GND_S3	
GND	110, 111	GND_S4	
GND	27, 28	GND_S5	
GND	103, 104	GND_S6	
GND	13, 21	GND_S7	
	35, 36	GND_S8	
	47, 56, 64, 65, 73, 81, 82, 90	CMN_GND	
VREG_S1_S6_SENSE_N	96, 88, 79	RMT_GND_S1, RMT_GND_S6, RMT_GND_S8	
	108	AVDD_BYP	AVDD_BYP_PMIC
	116	DVDD_BYP	DVDD_BYP_PMIC

C408_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BBPMU 138S0706
DVDD_BYP_GND
XW408_E SHORT-10L-0.1MM-SM ROOM=BBPMU
C410_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BBPMU 138S0706
AVDD_BYP_GND
XW406_E SHORT-10L-0.1MM-SM ROOM=BBPMU

VSW_S1	120, 129	VSW_SMPS1	L401_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM ROOM=BBPMU	VOLTAGE=0.752V	IPEAK: 7.8A
VFB_S1	70	VREG_S1_S6_SENSE_P			
VSW_S2	51, 60	VSW_SMPS2	L402_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM ROOM=BBPMU	VOLTAGE=1.224V	IPEAK: 3.19A
VFB_S2	34	PP_1V24_SMPS2_SNS	XW404_E SHORT-10L-0.1MM-SM ROOM=BBPMU		
VSW_S3	128, 136	VSW_SMPS3	L403_E 152S01273 0.47UH-20%-4.8A-0.027OHM MCFE2016-SM-1 ROOM=BBPMU	VOLTAGE=0.824V	IPEAK: 3.59A
VFB_S3	126	PP_0V82_SMPS3_SNS	XW402_E SHORT-10L-0.1MM-SM ROOM=BBPMU		
VSW_S4	93, 94, 102	VSW_SMPS4	L404_E 152S01120 1.0UH-3.4A-0.053OHM PIJF2016FE-SM ROOM=BBPMU	VOLTAGE=1.88V	IPEAK: 0.903A
VFB_S4	135	PP_1V9_SMPS4_SNS	XW403_E SHORT-10L-0.1MM-SM ROOM=BBPMU		
VSW_S5	18, 19	VSW_SMPS5	L405_E 152S01120 1.0UH-3.4A-0.053OHM PIJF2016FE-SM ROOM=BBPMU	VOLTAGE=0.752V	IPEAK: 2.39A
VFB_S5	45	PP_0V75_SMPS5_SNS	XW405_E SHORT-10L-0.1MM-SM ROOM=BBPMU		
VSW_S6	86, 95	VSW_SMPS6	L406_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM ROOM=BBPMU		
VFB_S6	62	VREG_S1_S6_SENSE_P			
VSW_S7	4, 12	VSW_SMPS7	L407_E 152S01273 0.47UH-20%-4.8A-0.027OHM MCFE2016-SM-1 ROOM=BBPMU	VOLTAGE=0.752V	IPEAK: 3.05A
VFB_S7	20	PP_0V75_SMPS7_SNS	XW401_E SHORT-10L-0.1MM-SM ROOM=BBPMU		
VSW_S8	44, 52	NC			
VFB_S8	53	NC			

PP_0V75_SMPS1_6
PP_0V22_SMPS2
PP_0V82_SMPS3
PP_0V9_SMPS4
PP_0V75_SMPS5
PP_0V75_SMPS1_6
PP_0V75_SMPS7
C429_E 20UF 20% 4V X5R 0402-0.1MM ROOM=BBPMU 138S00279
C430_E 20UF 20% 4V X5R 0402-0.1MM ROOM=BBPMU 138S00279
C434_E 20UF 20% 4V X5R 0402-0.1MM ROOM=BBPMU 138S00279
C431_E 20UF 20% 4V X5R 0402-0.1MM ROOM=BBPMU 138S00279
C432_E 20UF 20% 4V X5R 0402-0.1MM ROOM=BBPMU 138S00279
C433_E 20UF 20% 4V X5R 0402-0.1MM ROOM=BBPMU 138S00279
C435_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BBPMU
GND

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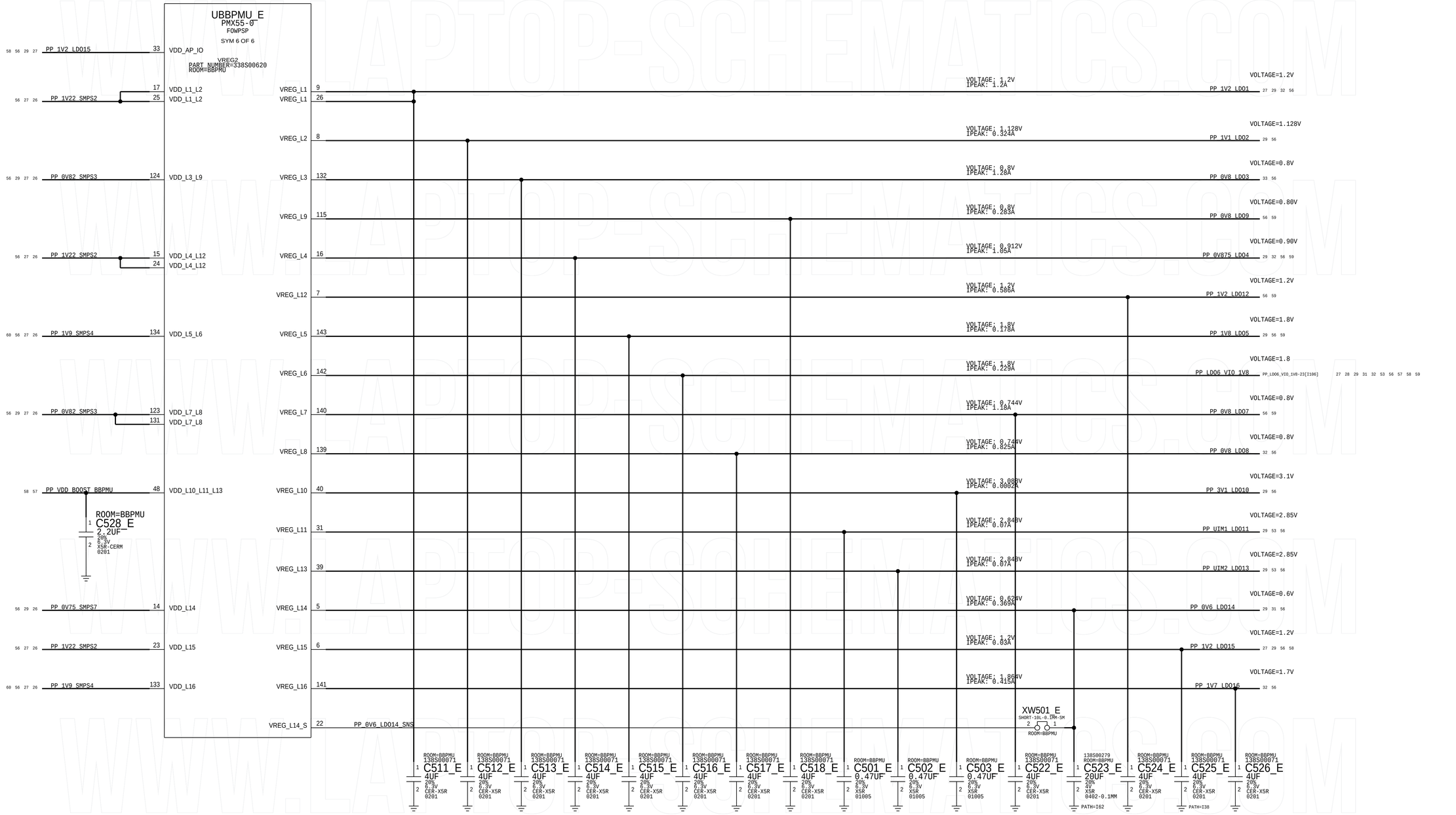
BB PMU: LDOS



PMX55 LDO CAPACITOR TABLE
N1200 (L1, L2, L3, L4, L7, L8, L9, L12, L14, L15) 4.7UF MIN, 22UF MAX N1200 (L14) 2X10UF OR 1X22UF MIN, 44UF MAX
MVP150 (L10, L11, L13) 0.47UF MIN, 5UF MAX
LVP600 (L5, L6, L16) 4.7UF MIN, 23.5UF MAX

XW502_E
SHORT-8L-0.25MM-SM
PP_1V2_LDO1 — PP_VDD_RF_1V2
MAKE_BASE=TRUE
PP_LDO6_VIO_1V8 — PP_LDO6_VIO_1V8

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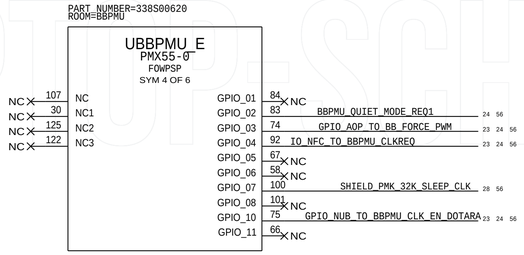
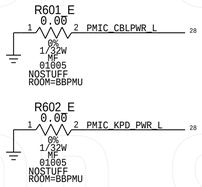
BB PMU: XTAL, CLK, ANALOG, IO

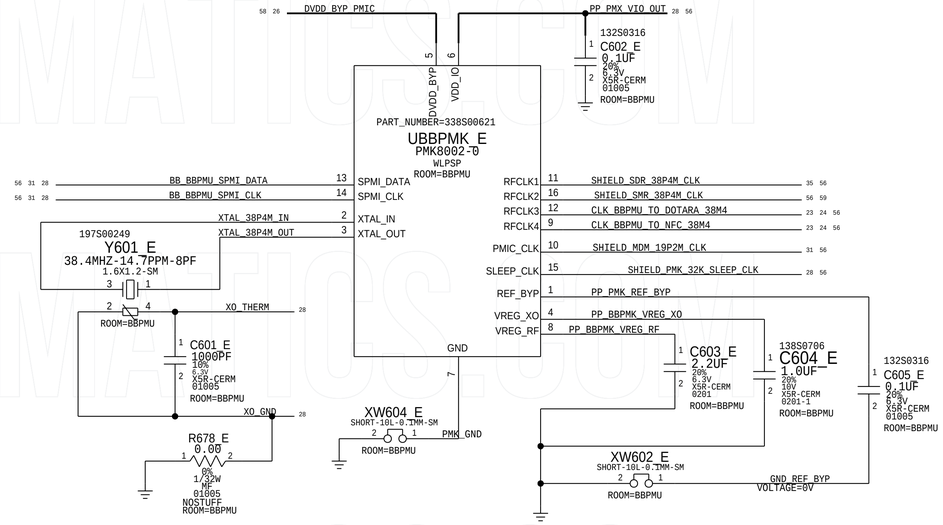
BOARD_ID	APN	R631_E	MLB/RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	PROTO0/DEV1	0X01
0.15V-0.25V	118S0730	12.0K	PROTO1/DEV2	0X02
0.25V-0.35V	118S00088	19.1K	PROTO1.5/DEV3	0X03
0.35V-0.45V	118S00122	27.0K	PROTO2/DEV4	0X04
0.45V-0.55V	118S00193	36.5K	EVT/DEV5	0X05
0.55V-0.65V	118S0868	47.5K	CARRIER/DEV6	0X06
0.65V-0.75V	118S0136	60.4K	DVT/DEV7	0X07
0.75V-0.85V	118S0768	75.0K	PVT	0X08
0.85V-0.95V	118S0626	100K	SPARE	0X09
0.95V-1.05V	118S0737	124K	SPARE	0X0A
1.05V-1.15V	118S0688	143K	SPARE	0X0B
1.15V-1.25V	TBD	TBD	SPARE	SPARE

PLATFORM_ID	APN	R632_E	MLB/RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	RADIO_DEV	0X1
0.15V-0.25V	118S0730	12.0K	DARWIN_FX	0X2
0.25V-0.35V	118S00088	19.1K	DARWIN_PG	0X3
0.35V-0.45V	118S00122	27.0K	RESERVED	0X4
0.45V-0.55V	118S00193	36.5K	MAV20.1	0X5
0.55V-0.65V	118S0868	47.5K	MAV20.2	0X6
0.65V-0.75V	118S0136	60.4K	RESERVED	0X7
0.75V-0.85V	118S0768	75.0K	RESERVED	0X8
0.85V-0.95V	118S0626	100K	RESERVED	0X9
0.95V-1.05V	118S0737	124K	RESERVED	0XA
1.05V-1.15V	118S0688	143K	DEV_BEERPONG	0XB
1.15V-1.25V	TBD	TBD	SPARE	SPARE

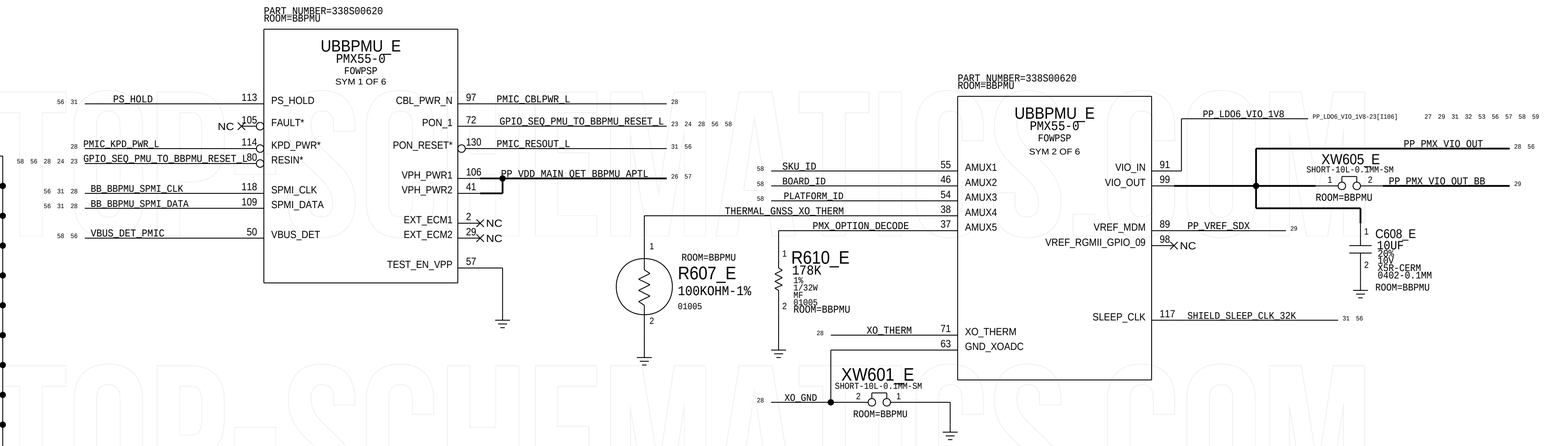
SKU_ID	APN	R630_E	MLB/RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	WW+KOLKATA	0X1
0.15V-0.25V	118S0730	12.0K	WW	0X2
0.25V-0.35V	118S00088	19.1K	ROW	0X3
0.35V-0.45V	118S00122	27.0K	SPARE	0X4
0.45V-0.55V	118S00193	36.5K	SPARE	0X5
0.55V-0.65V	118S0868	47.5K	SPARE	0X6
0.65V-0.75V	118S0136	60.4K	SPARE	0X7
0.75V-0.85V	118S0768	75.0K	SPARE	0X8
0.85V-0.95V	118S0626	100K	SPARE	0X9
0.95V-1.05V	118S0737	124K	SPARE	0XA
1.05V-1.15V	118S0688	143K	SPARE	0XB
1.15V-1.25V	TBD	TBD	SPARE	SPARE







MAKE SURE TO CONNECT GND PINS OF
C603_E AND C604_E TO MAIN GND IN LAYOUT
ROUTE KEEPOUT PROPERTY ALSO ADDED IN LAYOUT



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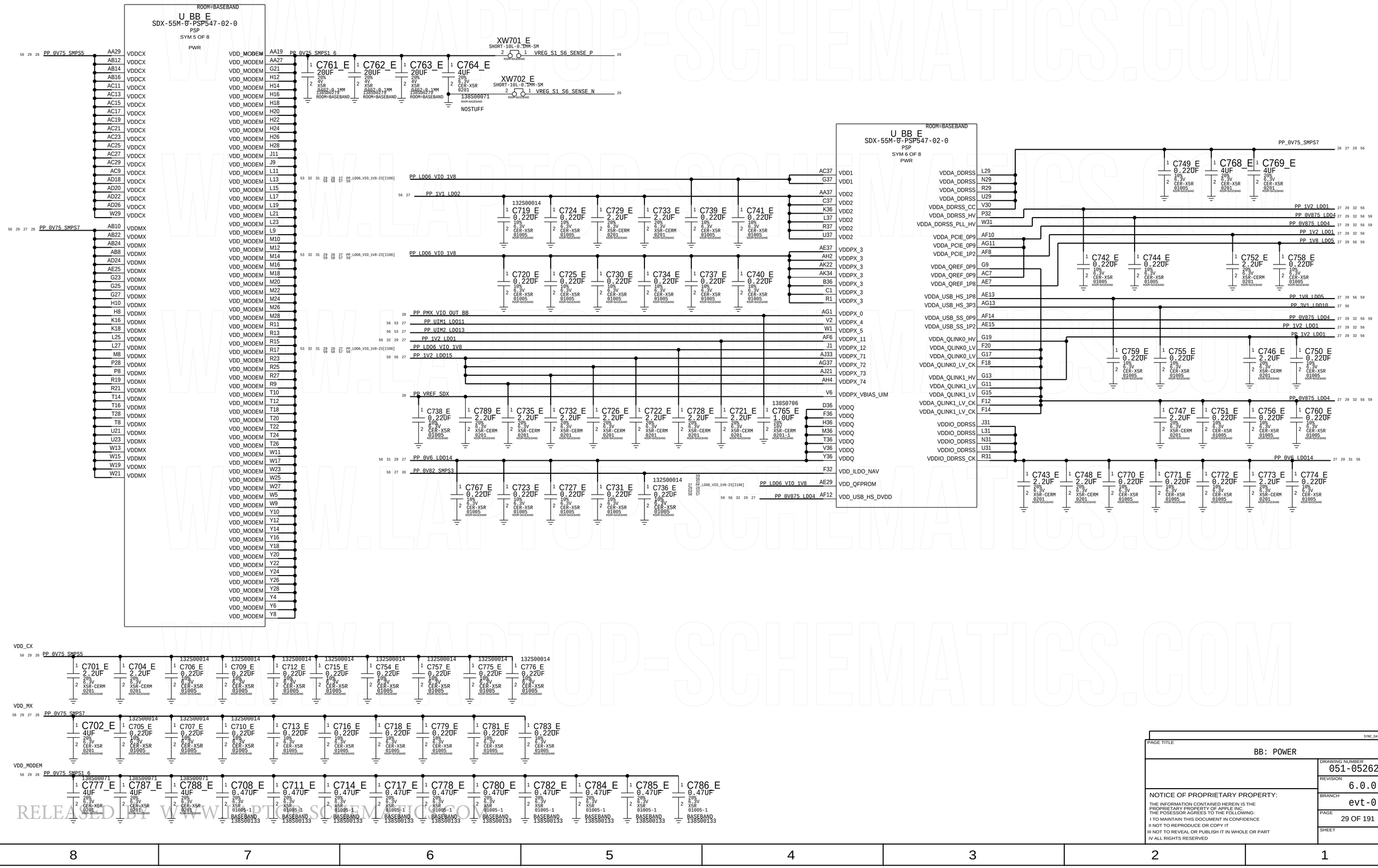

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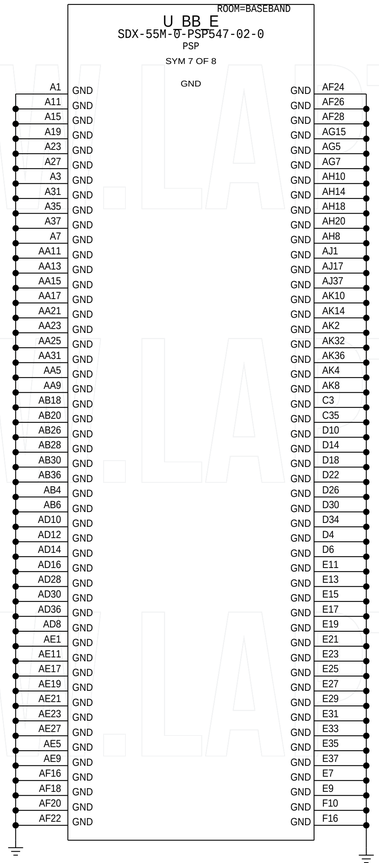

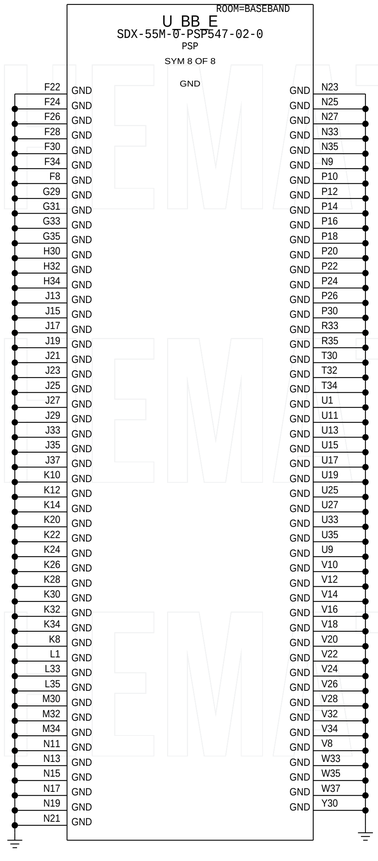

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BB:IO,MEM,SERDES,EEPROM

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BB EEPROM

59 58 57 56 53 32 31 29 28 27 PP_LDO6_VIO_1V8-23[I106]

PP_LDO6_VIO_1V8

R908_E 10K 5% 1/32W MF 01005 — ROOM=BASEBAND

C901_E 1.0UF 20% 10V X5R-CERM 0201-1 — ROOM=BASEBAND

R909_E 10K 5% 1/32W MF 01005 — ROOM=BASEBAND

EEPROM_E CAT24C08C4A WLCSP — ROOM=BASEBAND

A1	VCC		
BB_EEPROM_I2C_SCL	B1 SCL	SDA B2	BB_EEPROM_I2C_SDA
A2	VSS		

56 31 BB_EEPROM_I2C_SCL — 31 56 BB_EEPROM_I2C_SDA

U_BB_E

SDX-55M-0-PSP547-02-0 — PSP — SYM 2 OF 8 — QLINK — ROOM=BASEBAND

56 34 85_SUB6_QLINK_L0_P	C29	QLINK0_L0_P	QLINK1_L0_P	C11	85_MMW_QLINK_L0_P 56 59
56 34 85_SUB6_QLINK_L0_N	B28	QLINK0_L0_M	QLINK1_L0_M	D12	85_MMW_QLINK_L0_N 56 59
34 85_SUB6_QLINK_L1_P	D32	QLINK0_L1_P	QLINK1_L1_P	B14	85_MMW_QLINK_L1_P 59
34 85_SUB6_QLINK_L1_N	C31	QLINK0_L1_M	QLINK1_L1_M	A13	85_MMW_QLINK_L1_N 59
34 85_SUB6_QLINK_L2_P	C33	QLINK0_L2_P	QLINK1_L2_P	B18	85_MMW_QLINK_L2_P 59
34 85_SUB6_QLINK_L2_N	B32	QLINK0_L2_M	QLINK1_L2_M	A17	85_MMW_QLINK_L2_N 59
34 85_SUB6_QLINK_L3_P	D24	QLINK0_L3_P	QLINK1_L3_P	B8	85_MMW_QLINK_L3_P 59
34 85_SUB6_QLINK_L3_N	C23	QLINK0_L3_M	QLINK1_L3_M	C9	85_MMW_QLINK_L3_N 59
34 85_SUB6_QLINK_L4_P	D28	QLINK0_L4_P	QLINK1_L4_P	B6	85_MMW_QLINK_L4_P 59
34 85_SUB6_QLINK_L4_N	C27	QLINK0_L4_M	QLINK1_L4_M	A5	85_MMW_QLINK_L4_N 59
34 85_SUB6_QLINK_L5_P	C25	QLINK0_L5_P	QLINK1_L5_P	C17	85_MMW_QLINK_L5_P 59
34 85_SUB6_QLINK_L5_N	B24	QLINK0_L5_M	QLINK1_L5_N	B16	85_MMW_QLINK_L5_N 59
34 85_SUB6_QLINK_L6_P	B26	QLINK0_L6_P	QLINK1_L6_P	B20	85_MMW_QLINK_L6_P 59
34 85_SUB6_QLINK_L6_N	A25	QLINK0_L6_M	QLINK1_L6_M	C21	85_MMW_QLINK_L6_N 59
34 85_SUB6_QLINK_L7_P	B34	QLINK0_L7_P	QLINK1_L7_P	B12	85_MMW_QLINK_L7_P 59
34 85_SUB6_QLINK_L7_N	A33	QLINK0_L7_M	QLINK1_L7_M	C13	85_MMW_QLINK_L7_N 59
34 85_SUB6_QLINK_CLK_P	A29	QLINK0_CLK_P	QLINK1_L8_P	B10	85_MMW_QLINK_L8_P 59
34 85_SUB6_QLINK_CLK_N	B30	QLINK0_CLK_M	QLINK1_L8_M	A9	85_MMW_QLINK_L8_N 59
			QLINK1_L9_P	D8	85_MMW_QLINK_L9_P 59
			QLINK1_L9_M	C7	85_MMW_QLINK_L9_N 59
			QLINK1_L10_P	B22	85_MMW_QLINK_L10_P 59
			QLINK1_L10_M	A21	85_MMW_QLINK_L10_N 59
			QLINK1_L11_P	C19	85_MMW_QLINK_L11_P 59
			QLINK1_L11_M	D20	85_MMW_QLINK_L11_N 59
			QLINK1_L12_P	B4	85_MMW_QLINK_L12_P 59
			QLINK1_L12_M	C5	85_MMW_QLINK_L12_N 59
			QLINK1_CLK_P	C15	85_MMW_QLINK_CLK_P 59
			QLINK1_CLK_M	D16	85_MMW_QLINK_CLK_N 59

U_BB_E

SDX-55M-0-PSP547-02-0 — PSP — SYM 3 OF 8 — GPIO — ROOM=BASEBAND

53 BB_SIM2_DATA	AA3	GPIO_0	H2 NC
53 31 BB_SIM2_DETECT	AA1	GPIO_1	H4 NC
53 BB_SIM2_RESET	AB2	GPIO_2	AK28 NC
53 BB_SIM2_CLK	Y2	GPIO_3	Y32 NC
NC	T6	GPIO_4	AJ23 UART_COEX_BB_TO_WLAN_TXD 23 24 56
NC	U3	GPIO_5	AK24 UART_COEX_BB_FROM_WLAN_RXD 23 24 56
NC	V4	GPIO_6	AC33 NC
NC	U5	GPIO_7	AA35 GPIO_AP_TO_BB_RESET_DETECT_L 23 24 56
56 24 23 UART1_AOP_FROM_BB_RXD	AK26	GPIO_8	BB_TX AJ35 GPIO_AP_TO_BB_COREDUMP 23 24
56 24 23 UART1_AOP_TO_BB_TXD	AJ25	GPIO_9	BB_RX AH36 NC
56 31 BB_EEPROM_I2C_SDA	AH26	GPIO_10	AG35 NC
56 31 BB_EEPROM_I2C_SCL	AG25	GPIO_11	AF36 NC
56 24 23 I2S2_AP_FROM_BB_LRCLK	AF30	GPIO_12	AC31 NC
56 24 23 I2S2_AP_TO_BB_DOUT	AF32	GPIO_13	AE33 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L 23 24 56 58
56 24 23 I2S2_AP_FROM_BB_DIN	AG31	GPIO_14	AE35 NC
56 24 23 I2S2_AP_FROM_BB_BCLK	AH30	GPIO_15	AD34 NC
NC	AK30	GPIO_16	AF34 PCIE_GP2_AP_BI_BB_CLKREQ_L 23 24 56 58
NC	AG33	GPIO_17	AE31 PCIE_GP2_AP_TO_BB_PERST_L 23 24 56
NC	AH32	GPIO_18	AB34 BOOT_CFG1 56 58
BB_TO_DOTARA_COEX_1V2:NOT USED NC	AJ31	GPIO_19	AC35 NC
56 24 23 GPIO_R1_TO_BB_CH9_COEX	AJ27	GPIO_20	AB37 NC
56 24 23 IO_R1_TO_BB_LAA_SW_CTRL	AG27	GPIO_21	AD32 GPIO_AP_TO_BB_PEAK_PWR_IND 23 24 56
NC	AJ29	GPIO_22	AG29
NC	AB28	GPIO_23	AK6 NC
58 56 BOOT_CFG2	AA33	GPIO_24	L3 NC
NC	Y34	GPIO_25	L5 NC
NC	K2	GPIO_26	M5 NC
NC	K4	GPIO_27	AD2 BB_SIM1_DATA 53 56
56 34 BB_TO_SDR_WMSS_RESET_L	E1	GPIO_28	AC1 BB_SIM1_DETECT 31 53 56
59 56 35 SHIELD_RFFE4_SCLK_BB	G3	GPIO_29	AD4 BB_SIM1_RESET 53 56
59 56 35 SHIELD_RFFE4_SDATA_BB	F4	GPIO_30	AC3 BB_SIM1_CLK 53 56
NC	AG23	GPIO_31	AH34 NC
56 24 23 GPIO_AP_TO_BB_TIME_MARK	AH24	GPIO_32	E3 NC
56 24 23 GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	G1	GPIO_33	D2 QLINK_EN_BB_TO_SMR 56 59
56 34 QLINK_EN_BB_TO_SDR	F2	GPIO_34	D2 QLINK_REQ_SMR_TO_BB 56 59
QLINK_REQ_SDR_TO_BB	E5	GPIO_35	B2 BB_TO_SMR_WMSS_RESET_L 56 59
SHIELD_RFFE0_SDATA_BB	J5	GPIO_36	AH22 GPIO_BB_TO_R1_COEX 23 24 56
55 SHIELD_RFFE0_SCLK_BB	J3	GPIO_37	AG21 GPIO_BB_TO_R1_CH9_REQ 23 24 56
54 SHIELD_RFFE1_SDATA_BB	G5	GPIO_38	F6 NC
56 54 SHIELD_RFFE1_SCLK_BB	H6	GPIO_39	AF3 NC
		GPIO_79	AG3 NC

NOTE: TYPO IN SPEC

AP_TO_BB_DEV_WAKE : NOT USED
WAKE O/P WHEN BB IS END POINT

BOOT_CFG3 NOT NEEDED
GPIO_60 RESERVED FOR VFR_IRQ

DUAL-VOLTAGE IO PADS
VDD_PX71: GPIO8,9,12-23
VDD_PX72: GPIO46-57,59-61,71
VDD_PX73: GPIO31-32,44-45, 75-76
VDD_PX74: GPIO78-79

DUAL PSIM: SHORT SIM1_DET WITH SIM2_DET
PSIM AND ESIM: SIM2_DET STUFF PU

59 58 57 56 53 32 31 29 28 27 PP_LDO6_VIO_1V8-23[I106]

PP_LDO6_VIO_1V8

R905_E 100K 5% 1/32W MF 01005 — ROOM=BASEBAND

R907_E 100K 5% 1/32W MF 01005 — ROOM=BASEBAND

56 53 31 BB_SIM1_DETECT
53 31 BB_SIM2_DETECT

C906_E 0.2PF +/-0.05PF 16V CERM 01005 — ROOM=BASEBAND

NOTE:

ENSURE THAT THERE ARE NO UNINTENTIONAL EXTERNAL PULL-UPS ON THE FOLLOWING GPIOS AND THESE GPIOS ARE NOT LOGIC HIGH UNINTENTIONALLY BEFORE SDX55M COMES OUT OF RESET

(I.E. BEFORE SDX_RESOUT_N DE-ASSERTS TO LOGIC HIGH): GPIO_24, 54, 58, 59, AND 75.
SEE BOOT CONFIGURATION GPIOS PAGE OF SDX55M DESIGN GUIDELINES (80-PK565-5BM) FOR DETAILS.

U_BB_E

SDX-55M-0-PSP547-02-0 — PSP — SYM 1 OF 8 — CONTROL — ROOM=BASEBAND

56 28 SHIELD_SLEEP_CLK_32K	W3	SLEEP_CLK	EBI_ZQ P36 SHIELD_BB_BDM_ZQ
SHIELD_CXO_REXT	AJ3	QREFS_CXO_REXT	EBI_CA_CAL N37 SHIELD_BB_EBI1_CAL
56 28 SHIELD_MDM_19P2M_CLK	AD6	CXO	
56 BB_JTAG_RST_L	P6	SRST*	RESOUT* T2 NC
56 28 PMIC_RESOUT_L	AC5	RESIN*	PS_HOLD T4 PS_HOLD 28 56
NC	N3	MODE_0	DNC AG19 NC
NC	M4	MODE_1	DNC M6 NC
			DNC N5 NC
56 31 BB_JTAG_TCK_SWD_CLK_1V8_R	N1	TCK	DNC P34 NC
56 BB_JTAG_TRST_L	P2	TRST*	
56 31 BB_JTAG_TMS_SWD_IO_1V8_R	R3	TMS	REFGEN_REXT AK20 SHIELD_PCIE_CAL_RES
56 BB_JTAG_TDI	R5	TDI	
56 BB_JTAG_TDO	P4	TDO	PMIC_SPMI_CLK AF2 BB_BBPMU_SPMI_CLK 28 56
			PMIC_SPMI_DATA AE3 BB_BBPMU_SPMI_DATA 28 56

R904_E 3.0K 1% 1/32W MF 01005 — ROOM=BASEBAND

R902_E 240 1% 1/32W MF 01005 — ROOM=BASEBAND

R903_E 240 1% 1/32W MF 01005 — ROOM=BASEBAND

PP_0V6_LDO14 27 29 56

R901_E 100 1% 1/32W MF 01005 — ROOM=BASEBAND

C904_E 10PF 2% 25V C0G 01005 — ROOM=BASEBAND

C905_E 10PF 2% 25V C0G 01005 — ROOM=BASEBAND

U_BB_E

SDX-55M-0-PSP547-02-0 — PSP — SYM 4 OF 8 — USB_PCIE — ROOM=BASEBAND

		PCIE_REFCLK_P	AJ9 90_PCIE_GP2_AP_TO_BB_REFCLK_P 23 24 56
		PCIE_REFCLK_M	AG9 90_PCIE_GP2_AP_TO_BB_REFCLK_N 23 24 56
		PCIE_TX0_P	AJ13 90_PCIE_BB_TO_AP_RX_SDX_P
		PCIE_TX0_M	AH12 90_PCIE_BB_TO_AP_RX_SDX_N
		PCIE_TX1_P	AJ11 NC
		PCIE_TX1_M	AK12 NC
		PCIE_RX0_P	AJ5 90_PCIE_GP2_AP_TO_BB_TX_P 23 24 56
		PCIE_RX0_M	AK6 90_PCIE_GP2_AP_TO_BB_TX_N 23 24 56
		PCIE_RX1_P	AH6 NC
		PCIE_RX1_M	AJ7 NC
58 56 90_USB_BB_P	AJ15	USB_HS_DP	
58 56 90_USB_BB_N	AK16	USB_HS_DM	
NC	AG17	USB_SS_TX_P	
NC	AJ16	USB_SS_TX_M	
NC	AK18	USB_SS_RX_P	
NC	AJ19	USB_SS_RX_M	

C903_E 0.22UF 10% 6.3V CER-X5R 01005 — 132S00014 BASEBAND — 90_PCIE_GP2_AP_FROM_BB_RX_P 23 24 56

C902_E 0.22UF 10% 6.3V CER-X5R 01005 — 132S00014 BASEBAND — 90_PCIE_GP2_AP_FROM_BB_RX_N 23 24 56

24 23 PP1V2_S2

C907_E 0.1UF 20% 6.3V X6S-CERM 01005 — 132S0316 — ROOM=BASEBAND

R910_E 10K 5% 1/32W MF 01005 — ROOM=BASEBAND

VCCA VCCB — ROOM=BASEBAND

SWD_E NVT0202JK X2SON

C908_E 0.1UF 20% 6.3V X6S-CERM 01005 — 132S0316 — ROOM=BASEBAND

PP_LDO6_VIO_1V8 — PP_LDO6_VIO_1V8-23[I106] — 27 28 29 31 32 53 56 57 58 59

56 24 23 SWD_AP_TO_MANY_SWCLK

R912_E 0.00 0% 1/32W MF 01005 — ROOM=BASEBAND

56 24 23 SWD_AP_BI_BB_SWDIO — BB_JTAG_TMS_SWD_IO_R

SWD_OE 6 OE

5 A1

4 A2

NOSTUFF

R911_E 10K 5% 1/32W MF 01005 — ROOM=BASEBAND

GND 2

B1 8 — BB_JTAG_TCK_SWD_CLK_1V8

B2 1 — BB_JTAG_TMS_SWD_IO_1V8

R914_E 0.00 0% 1/32W MF 01005 — ROOM=BASEBAND — BB_JTAG_TCK_SWD_CLK_1V8_R 31 56

R913_E 0.00 0% 1/32W MF 01005 — ROOM=BASEBAND — BB_JTAG_TMS_SWD_IO_1V8_R 31 56

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NOTE: 1UF SHOULD BE AS CLOSE AS POSSIBLE TO CORRESPONDING PIN ON SDR

PP_1V2_LDO1 — 56 32 29 27
PP_1V7_LDO16 — 27 32 56
PP_0V8_LDO8 — 56 27
PP_0V875_LDO4 — 59 56 29 27
PP_LDO6_VIO_1V8 — 59 58 57 56 53 32 31 29 28 27

U_SDR_E
SDR865-0
PSP
SYM 6 OF 8
PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

A24	VDDAM_TP0	VDDAH_TP0	B25
AG26	VDDAM_TP1	VDDAH_TP1	AF25
B29	VDDAM_TX0	VDDAH_TX0	A30
AF29	VDDAM_TX1	VDDAH_TX1	AF31
AF23	VDDAM_TX2	VDDAH_TX2	AG22
E2	VDDAM_RP0	VDDAH_RP0	C2
F1	VDDAM_RP1	VDDAH_RP1	G2
P1	VDDAM_RP2	VDDAH_RP2	M1
V1	VDDAM_RP3	VDDAH_RP3	Y1
AB1	VDDAM_RP4	VDDAH_RP4	AG4
AF15	VDDAM_RP5	VDDAH_RP5_2	AF13
A16	VDDAM_RX0	VDDAH_RX0	A18
AG10	VDDAM_RX5		
D21	VDDAM_BBRX_TOP	VDDAH_TXDAC0	J32
AA22	VDDAM_BBRX_BOT	VDDAH_TXDAC1	W30
V35	VDD_CX	VDDAH_LVDS	T21
W36	VDD_CX		
L36	VDD_CX		
J34	VDD_MX0		
V33	VDD_MX1		
L34	VDD_PHY		
K35	VDD_PX		
K33	VDD_PXM		

STAR ROUTE

STAR ROUTE

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NOTE: 1UF SHOULD BE AS CLOSE AS POSSIBLE TO CORRESPONDING PIN ON SDR

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 5 OF 8

D1	VDDAL_RP0	A4	VDDAL_DIG_RP0
F3	VDDAL_RP1	K1	VDDAL_DIG_RP1
N2	VDDAL_RP2	L2	VDDAL_DIG_RP2
W2	VDDAL_RP3	AA2	VDDAL_DIG_RP3
AC2	VDDAL_RP4	AE2	VDDAL_DIG_RP4
AG16	VDDAL_RP5	AG14	VDDAL_DIG_RP5
B13	VDDAL_RX0	G24	VDDAL_DIG_TP0
C6	VDDAL_RX1	AA24	VDDAL_DIG_TP1
J6	VDDAL_RX2	B21	VDDAL_DIG1
L6	VDDAL_RX3	Y23	VDDAL_DIG2
W6	VDDAL_RX4	H21	VDDAL_FBRX
AC6	VDDAL_RX5	B17	VDDAL_GNSS
AG12	VDDAL_RX6	A20	VDDAL_ICON6
E12	VDDAL_RXLO0	T19	VDDAL_ICON32
N12	VDDAL_RXLO4	T1	VDDAL_XO
R12	VDDAL_RXLO5		
W12	VDDAL_RXLO7		
A26	VDDAL_TP0		
AF27	VDDAL_TP1		
A28	VDDAL_TX0		
AG30	VDDAL_TX1		
AE22	VDDAL_TX2		

XW1288_E SHORT-8L-0.5MM-SM — PP_0V8_LDO3 (56 33 27) — PP_0V8_LDO3_SDR_VDDAL_RP
XW1289_E SHORT-8L-0.5MM-SM — PP_0V8_LDO3_SDR_VDDAL_RX
XW1281_E SHORT-8L-0.25MM-SM — PP_0V8_LDO3_SDR_VDDAL_RXLO
XW1282_E SHORT-8L-0.1MM-SM — PP_0V8_LDO3_SDR_VDDAL_TP
XW1283_E SHORT-8L-0.1MM-SM — PP_0V8_LDO3_SDR_VDDAL_TX
XW1284_E SHORT-8L-0.1MM-SM — PP_0V8_LDO3 (56 33 27)

XW1202_E … XW1207_E SHORT-8L-0.1MM-SM — PP_LDO3_SDR_VDDAL_RP0 … RP5 57
XW1208_E … XW1218_E SHORT-8L-0.1MM-SM — PP_LDO3_SDR_VDDAL_RX0 67 … RX6 90; PP_LDO3_SDR_VDDAL_RXLO0 27 … RXLO7 27; PP_LDO3_SDR_VDDAL_TP0 30 … TP1 30; PP_LDO3_SDR_VDDAL_TX0 20 … TX2 20
XW1201_E SHORT-10L-0.1MM-SM — PP_LDO3_SDR_VDDAL_TP0 30

C1226_E 4UF 20% 6.3V CER-X5R 0805 (138S00071) — C1227_E 4UF 20% 6.3V CER-X5R 0805 (138S00071)

C1217_E … C1201_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1202_E … C1213_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1233_E … C1234_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1235_E … C1210_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1203_E … C1236_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1237_E … C1207_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1204_E … C1209_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1216_E … C1211_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)

XW1223_E … XW1228_E SHORT-8L-0.1MM-SM — PP_LDO3_SDR_VDDAL_DIG_RP0 6 … RP5 6
XW1286_E SHORT-8L-0.1MM-SM — PP_0V8_LDO3_SDR_VDDAL_DIG_RP — PP_0V8_LDO3 (27 33 56)
XW1229_E … XW1285_E SHORT-8L-0.1MM-SM — PP_LDO3_SDR_VDDAL_DIG_TP0 10 … TP1 10; PP_0V8_LDO3_SDR_VDDAL_DIG_TP
XW1230_E … XW1287_E SHORT-8L-0.25MM-SM — PP_LDO3_SDR_VDDAL_DIG1 171; PP_LDO3_SDR_VDDAL_DIG2 124
XW1233_E … XW1291_E SHORT-8L-0.1MM-SM — PP_LDO3_SDR_VDDAL_FBRX 20; PP_LDO3_SDR_VDDAL_GNSS 40; PP_LDO3_SDR_VDDAL_ICON6 5
XW1235_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR — PP_LDO3_SDR_VDDAL_ICON32 25
XW1236_E SHORT-8L-0.1MM-SM PATH=1106 — PP_LDO3_SDR_VDDAL_XO 18

C1218_E … C1225_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1221_E … C1224_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1231_E … C1232_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1238_E … C1230_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1239_E … C1229_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)
C1228_E 0.1UF 20% 6.3V X5R-CERM 01005 (132S0316)

SYNC_DATE=07/30/2019

PAGE TITLE	XCVR POWER_2
DRAWING NUMBER	051-05262
SIZE	D
REVISION	6.0.0
BRANCH	evt-0
PAGE	33 OF 191
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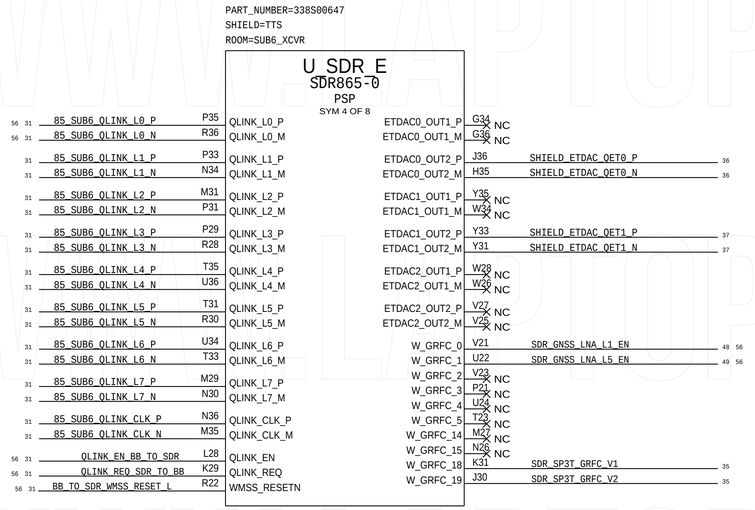

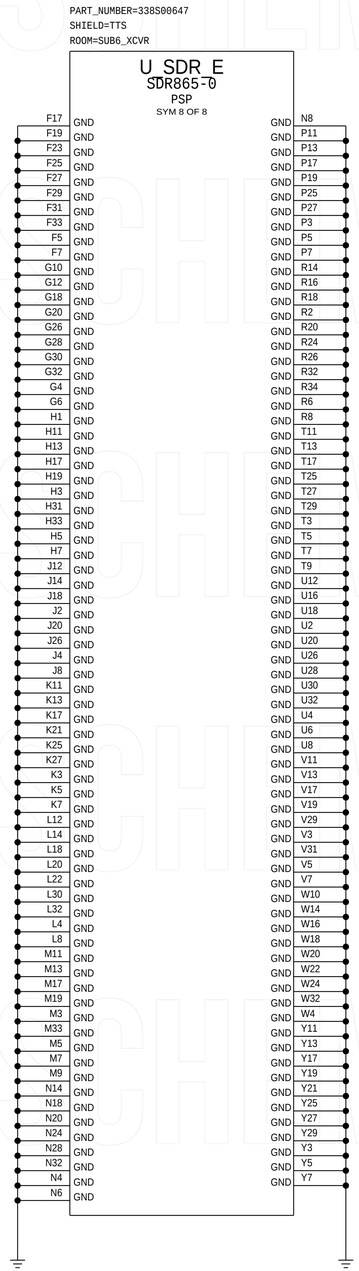

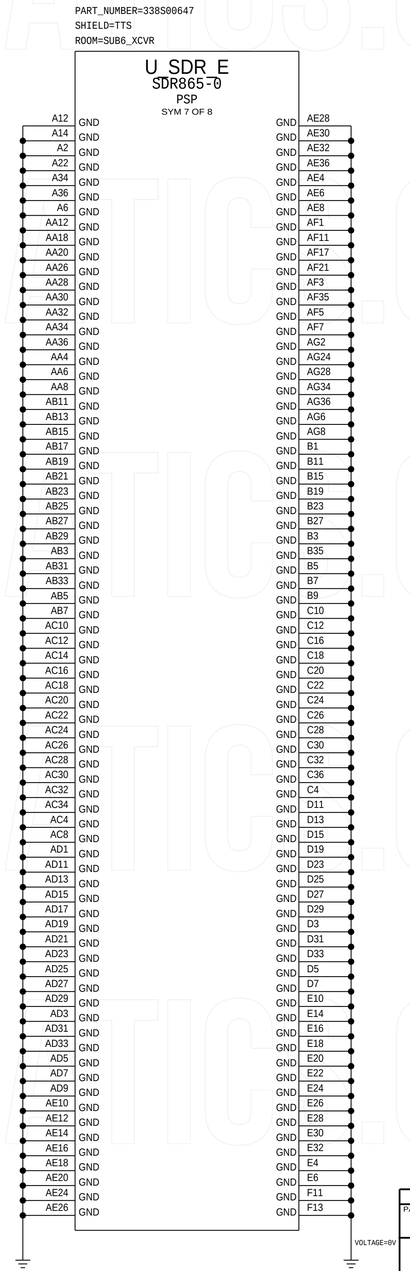

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PAGE TITLE: XCVR DIGITAL & GND

DRAWING NUMBER: 051-05262
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REVISION: 6.0.0
BRANCH: evt-0
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TRANSCEIVER: TX & RX

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PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 3 OF 8

QLINK BACKDOOR

59 56 31	SHIELD_RFFE4_SCLK_BB	F21	RFFE0_CLK			
59 56 31	SHIELD_RFFE4_SDATA_BB	G22	RFFE0_DATA			
56 46 40 36 24 23	SHIELD_RFFE1_SCLK_SDR	K23	RFFE1_CLK			
56 46 40 36 24 23	SHIELD_RFFE1_SDATA_SDR	J24	RFFE1_DATA			
56 39 24 23	SHIELD_RFFE2_SCLK_SDR	H25	RFFE2_CLK			
56 39 24 23	SHIELD_RFFE2_SDATA_SDR	H27	RFFE2_DATA			
56 44 40 24 23	SHIELD_RFFE3_SCLK_SDR	J28	RFFE3_CLK			
56 44 40 24 23	SHIELD_RFFE3_SDATA_SDR	H29	RFFE3_DATA			
56 45 43 42 41 24 23	SHIELD_RFFE5_SCLK_SDR	L26	RFFE5_CLK			
56 45 43 42 41 24 23	SHIELD_RFFE5_SDATA_SDR	M25	RFFE5_DATA			
56 47 43 42 38	SHIELD_RFFE7_SCLK_SDR	L24	RFFE7_CLK			
56 47 43 42 38	SHIELD_RFFE7_SDATA_SDR	M23	RFFE7_DATA			
56 37 24 23	SHIELD_RFFE8_SCLK_SDR	P23	RFFE8_CLK			
56 37 24 23	SHIELD_RFFE8_SDATA_SDR	N22	RFFE8_DATA			
NC		J22	RFFE9_CLK			
NC		G23	RFFE9_DATA			
56 28	SHIELD_SDR_38P4M_CLK	R4	XO_IN			

C1400_E
47PF
5%
16V
NP0-C0G
01005
ROOM=SUB6_XCVR
NOSTUFF

TX0_LB	B31	50_TX_IN_XCVR_TX0_LB	23 24	TO LBPAD_TX	
TX0_GSM_LB	A32	50_TX_IN_XCVR_TX0_LB2G	23 24	TO LMB/2G PAD_TX	
TX0_JB	B33	50_TX_IN_XCVR_TX0_LMB	23 24	TO LMB/2G PAD_TX	
TX0_MB	C34	50_TX_IN_XCVR_TX0_MB1	40	TO HBPAD_TX	
TX0_GSM_MB	D35	50_TX_IN_XCVR_TX0_MB2G	23 24	TO LMB/2G PAD_TX	
TX0_HB	E36	50_TX_IN_XCVR_TX0_HB1	40	TO HBPAD_TX	
TX0_UHB	E34	NC			
TX0_LAA_V2X	F35	NC			
TX1_LB_JB	AG32	50_TX_IN_XCVR_TX1_LB_JB	23 24	TO LBPAD_TX	
TX1_HB2	AE34	NC			
TX1_MB	AF33	NC			
TX1_HB1	AD35	50_TX_IN_XCVR_TX1_HB1	42	TO HBDSM TX	
TX1_UHB_5GLM	AB35	NC		50_TX_IN_XCVR_TX1_UHB DELETED ON P2	
TX1_5GH	AC36	NC		50_TX_IN_XCVR_TX1_N79 DELETED ON P2	
TX2_HB_V2X	AF19	NC			
TX2_UHB_5GLM	AG20	50_TX_IN_XCVR_TX2_UHB			
TX2_5GH	AG18	50_TX_IN_XCVR_TX2_N79			

R1402_E
0.00
5%
1/32W
MF
01005
ROOM=SUB6_XCVR

L1402_E
4.7NH-3%-0.270A
01005
NOSTUFF
ROOM=SUB6_XCVR

L1406_E
4.7NH-3%-0.270A
01005
NOSTUFF
ROOM=SUB6_XCVR

50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 23 24

TO UHBPAD LAT TX

TO UHBPAD LAT TX

R1403_E
0.00
5%
1/32W
MF
01005
ROOM=SUB6_XCVR

L1403_E
4.7NH-3%-0.270A
01005
NOSTUFF
ROOM=SUB6_XCVR

L1407_E
4.7NH-3%-0.270A
01005
NOSTUFF
ROOM=SUB6_XCVR

50_TX_IN_TX2_UHB_PAD_TX_N79_IN 23 24

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 2 OF 8
DRX_GNSS

FROM_HBDSM_RX	42	50_RX_XCVR_DRX0_HB_DSM_RXOUT_DRX4	G8	DRX0		
FROM_MIMODSM_RX_U	45	50_RX_XCVR_DRX1_MIMO2_RX_OUT_DRX4	G16	DRX1		
FROM_HBDSM_RX	42	50_RX_XCVR_DRX2_HB_DSM_RXOUT_DRX1	E8	DRX2		
FROM_MIMODSM_RX_U	45	50_RX_XCVR_DRX3_MIMO2_RX_OUT_DRX3	AA14	DRX3		
FROM_HBDSM_RX	42	50_RX_XCVR_DRX4_HB_DSM_RXOUT_DRX2	P9	DRX4		
FROM_MIMODSM_RX_U	45	50_RX_XCVR_DRX5_MIMO2_RX_OUT_DRX1	N16	DRX5		
FROM_LBDSM_RX	41	50_RX_XCVR_DRX6_LB_DSM_RXOUT1	H9	DRX6		
FROM_MIMODSM_RX_U	45	50_RX_XCVR_DRX7_MIMO2_RX_OUT_DRX2	F15	DRX7		
NC			F9	DRX8		
NC			G14	DRX9		
FROM_LAA_RX_U	23 24	50_LAA_RX_XCVR_DRX10	N10	DRX10		
NC			M15	DRX11		
FROM_UHBDSM_RX	43	50_RX_XCVR_DRX12_UHB_DSM_N79_RX_OUT1	AA10	DRX12		
FROM_UHBDSM_RX	43	50_RX_XCVR_DRX13_UHB_DSM_N79_RX_OUT2	AA16	DRX13		
FROM_UHBDSM_RX	43	50_RX_XCVR_DRX14_UHB_DSM_UHB_RX_OUT1	R10	DRX14		
FROM_UHBDSM_RX	43	50_RX_XCVR_DRX15_UHB_DSM_UHB_RX_OUT2	P15	DRX15		
NC			M21	DNC		
			AB9	DRXE	50_RX_XCVR_DRXE_HB_DSM_RXOUT_DRX3	42
			D9	DRXF	50_RX_XCVR_DRXF_LB_DSM_RXOUT2	41
			K19	FBRX_IN	50_TX_IN_XCVR_FBRX_1	
			C14	GNSS_IN_L1	50_RX_GNSS_L1	48
			D17	GNSS_IN_L5	50_RX_GNSS_L5	49

FROM_HBDSM_RX

FL1401_E
10-OHM-1.1A
01005
ROOM=SUB6_XCVR

58 56 24 23 PP3V0_S2

PP3V0_S2_SP3T

C1401_E
0.22UF
10%
6.3V
CER-X5R
01005
ROOM=SUB6_XCVR

U_SP3T_E
SP3T-MCD
LGA
PART_NUMBER=353S02417
ROOM=SUB6_XCVR

34	SDR_SP3T_GRFC_V1	2	CTL1		
34	SDR_SP3T_GRFC_V2	1	CTL2		
		9	VDD		
		10	ANT		
		3	PORT1	50_CPLR_L_CPL1_LAT_OUT	46
		5	PORT2	50_UHB_L_CPLR_OUT	23 24
		7	PORT3	50_CPLR_U_CPL1_UAT_OUT	47
		4 6 8	GND		

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 1 OF 8
PRX

FROM HBPAD_RX	40	50_RX_XCVR_PRX0_MB_HBT_PRX_OUT4	K9	PRX0		
FROM MIMODSM_L	44	50_RX_XCVR_PRX1_MIMO1_RX_OUT_DRX4	H15	PRX1		
FROM HBPAD_RX	40	50_RX_XCVR_PRX2_LMB_MBT_HBT_PRX_OUT1	A10	PRX2		
FROM MIMODSM_L	44	50_RX_XCVR_PRX3_MIMO1_RX_OUT_DRX3	V15	PRX3		
FROM HBPAD_RX	40	50_RX_XCVR_PRX4_MBT_HB_PRX_OUT2	V9	PRX4		
FROM MIMODSM_L	44	50_RX_XCVR_PRX5_MIMO1_RX_OUT_DRX1	U14	PRX5		
FROM LBPAD_RX	24 23	50_RX_XCVR_PRX6_LB_A_RX0	J10	PRX6		
FROM MIMODSM_L	44	50_RX_XCVR_PRX7_MIMO1_RX_OUT_DRX2	K15	PRX7		
NC			C8	PRX8		
	24 23	50_RX_XCVR_PRX10_LB_PRX_OUT2	A8	PRX10		
NC			J16	PRX11		
FROM LAA_RX_L	23 24	50_RX_LAA_XCVR_PRX12	L10	PRX12		
NC			L16	PRX13		
FROM UHBPAD_RX	23 24	50_RX_XCVR_PRX14_N79_RX_OUT1	Y9	PRX14		
FROM UHBPAD_RX	23 24	50_RX_XCVR_PRX15_N79_RX_OUT2	Y15	PRX15		
FROM UHBPAD_RX	23 24	50_RX_XCVR_PRX16_UHB_RX_OUT1	U10	PRX16		
FROM UHBPAD_RX	23 24	50_RX_XCVR_PRX17_UHB_RX_OUT2	T15	PRX17		
			W8	PRXE	50_RX_XCVR_PRXE_HB_PRX_OUT3	40

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PAGE TITLE: XCVR RF

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HB/LMB-2G

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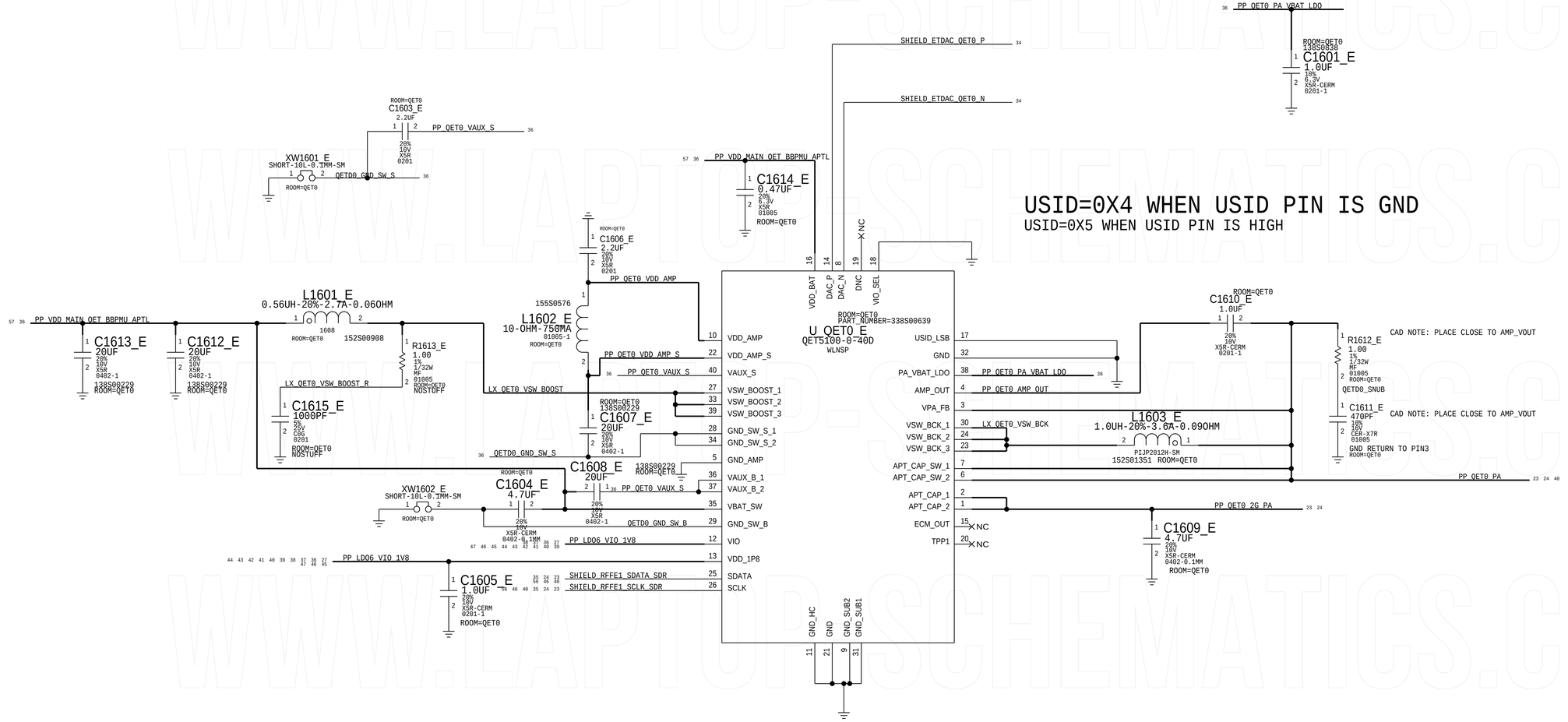
USID=0X4 WHEN USID PIN IS GND
USID=0X5 WHEN USID PIN IS HIGH



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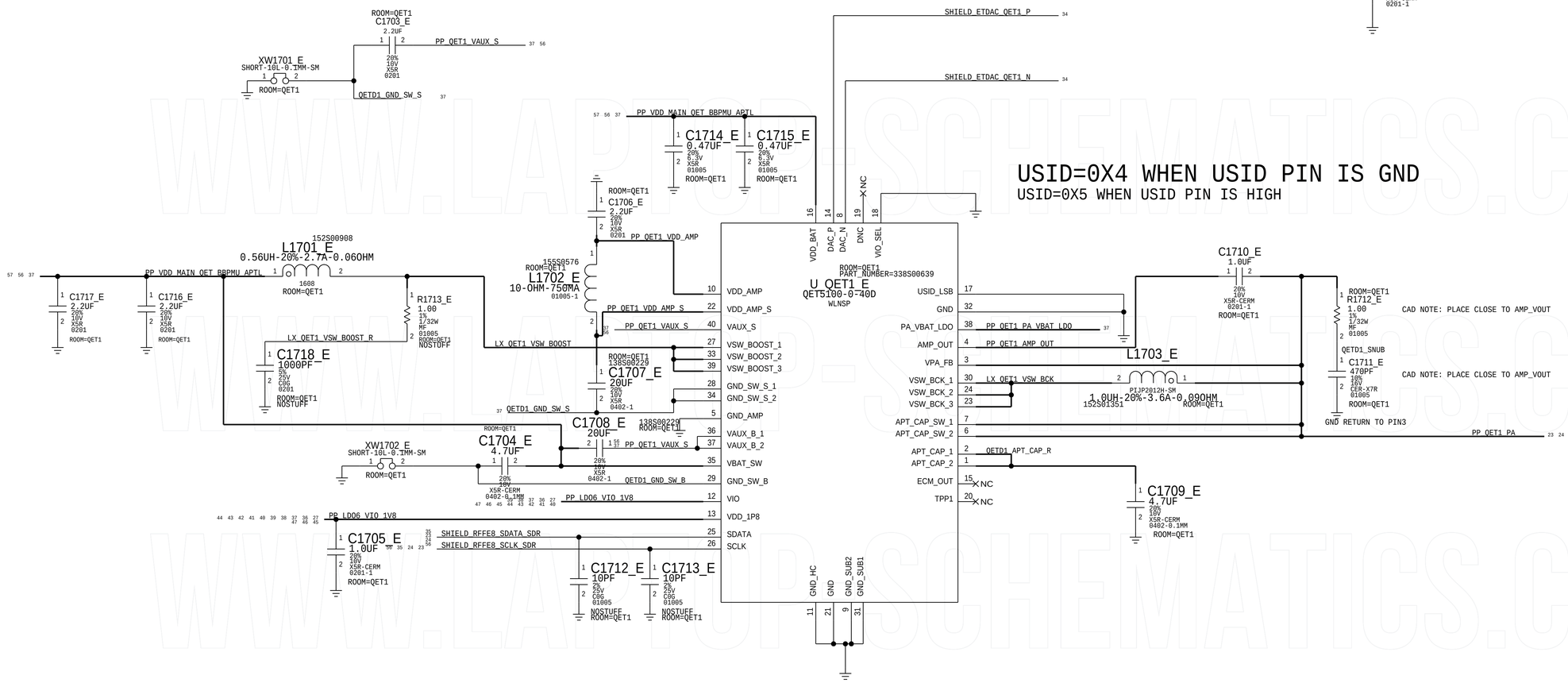

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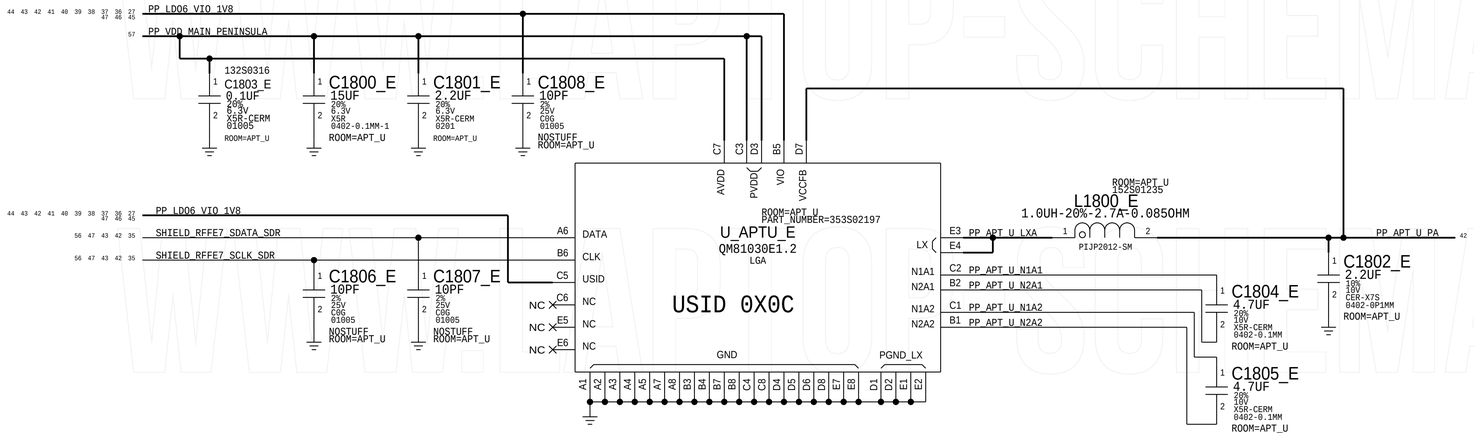

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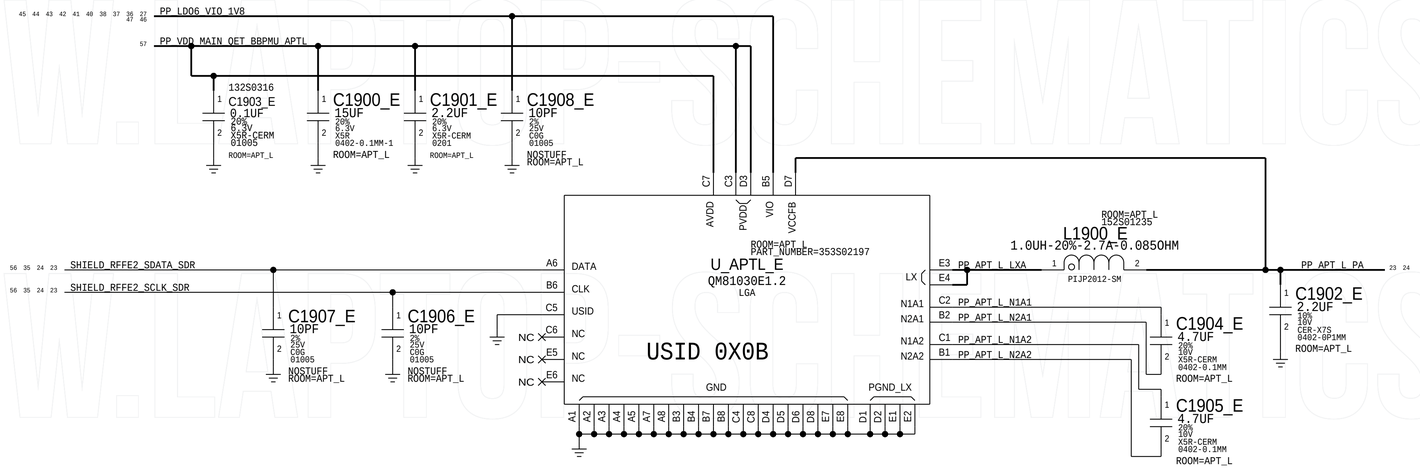

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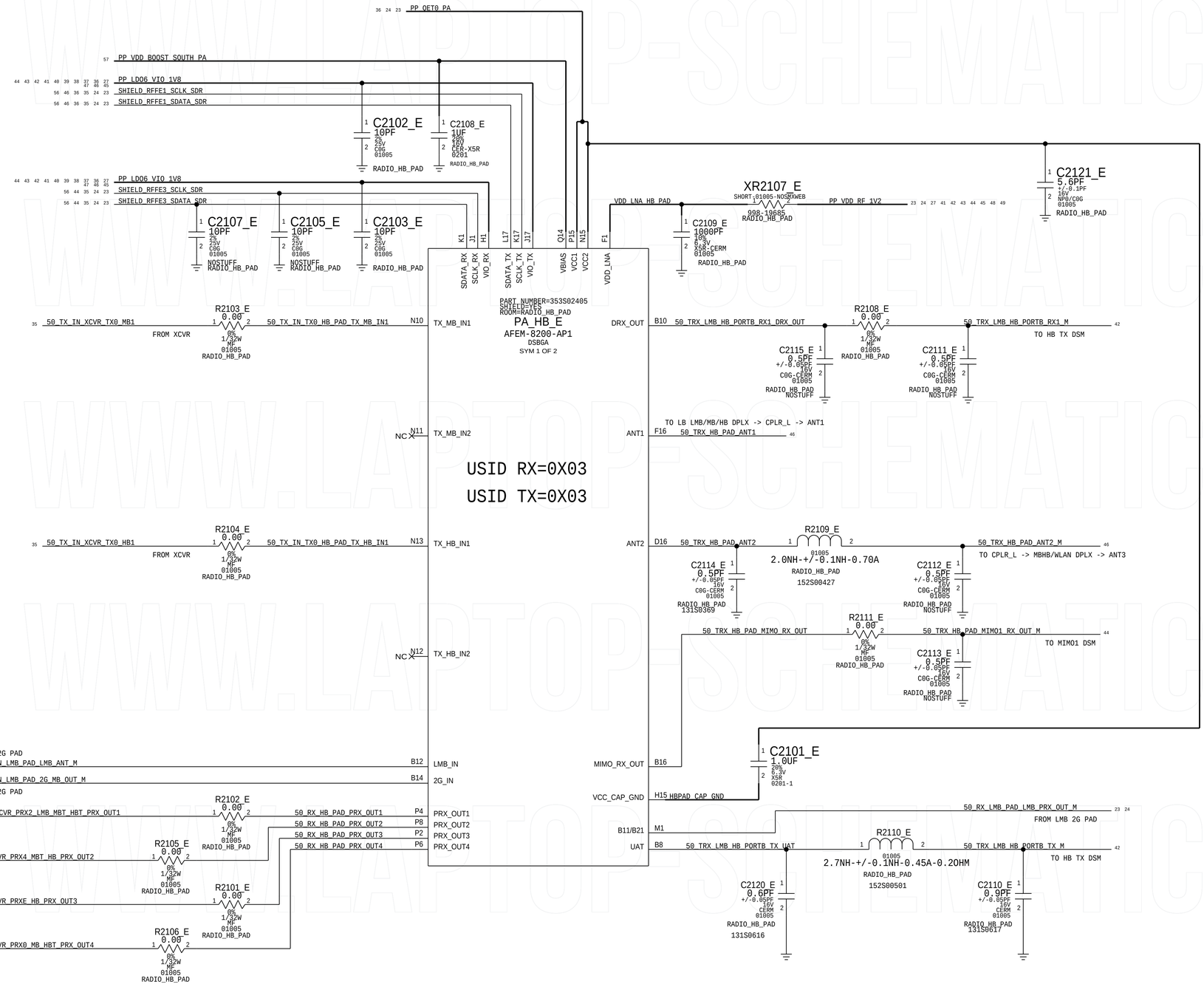
HB PAD



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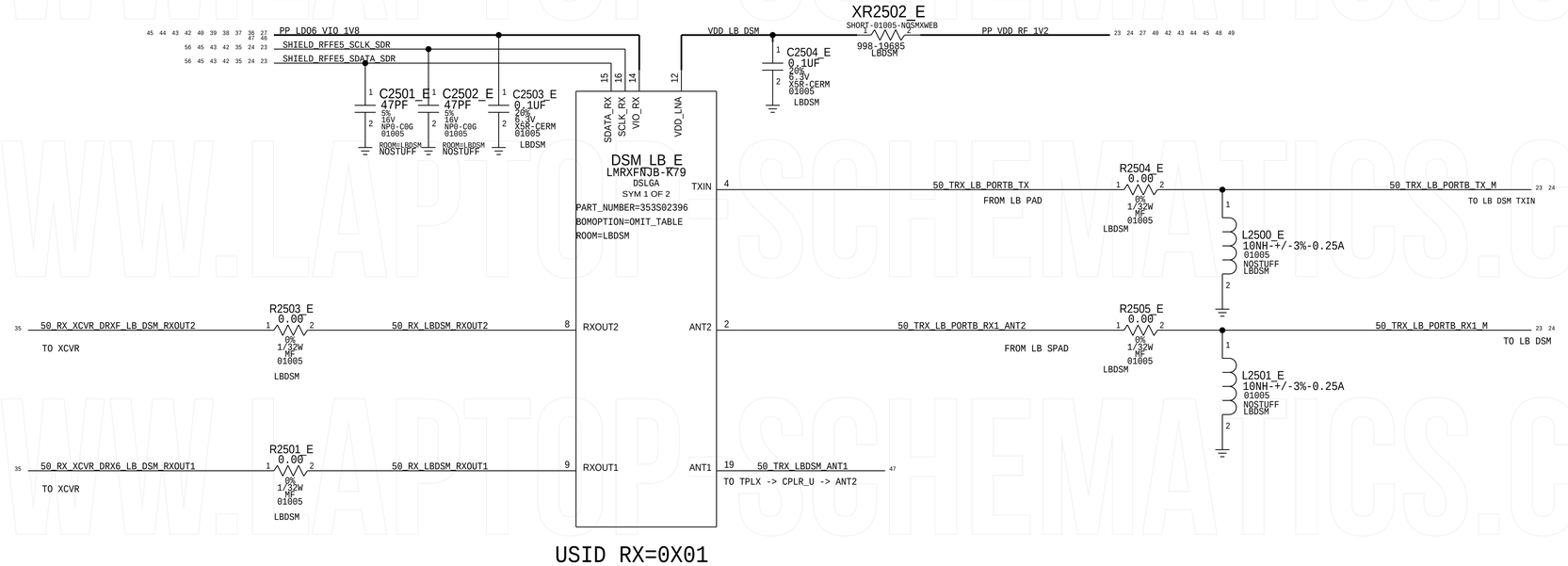
LB DIVERSITY MODULE



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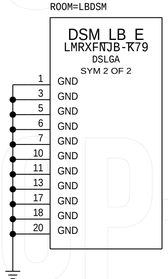
BOMOPTION=OMIT_TABLE
ROOM=LBDSM



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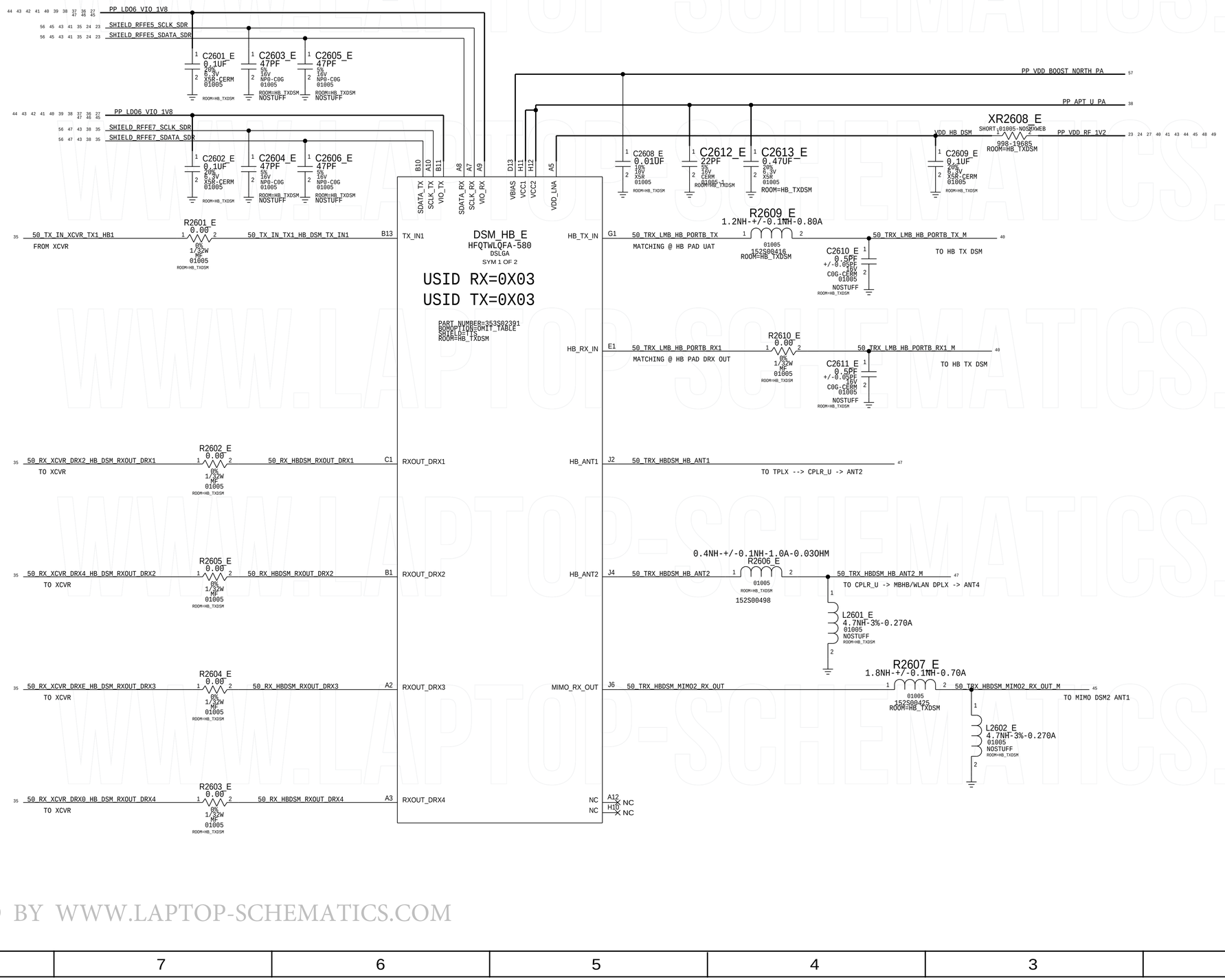
HB RECEIVE DIVERSITY & TX MODULE



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SYNC_DATE=07/30/2019

PAGE TITLE: HB TXDSM

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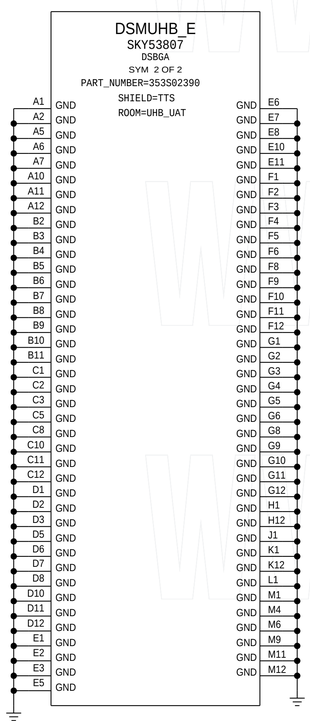
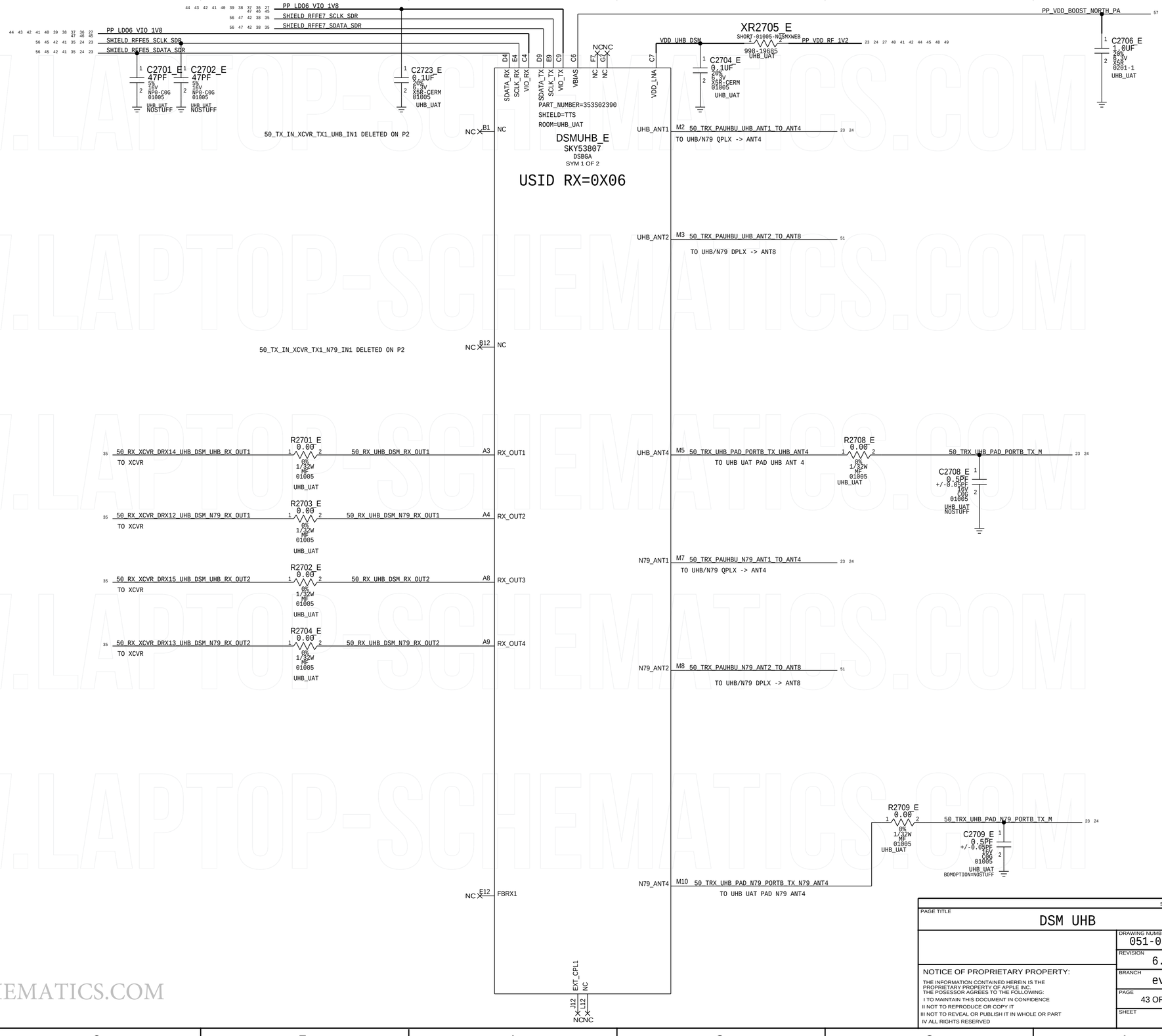
UHB DIVERSITY MODULE





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PAGE TITLE
DSM UHB

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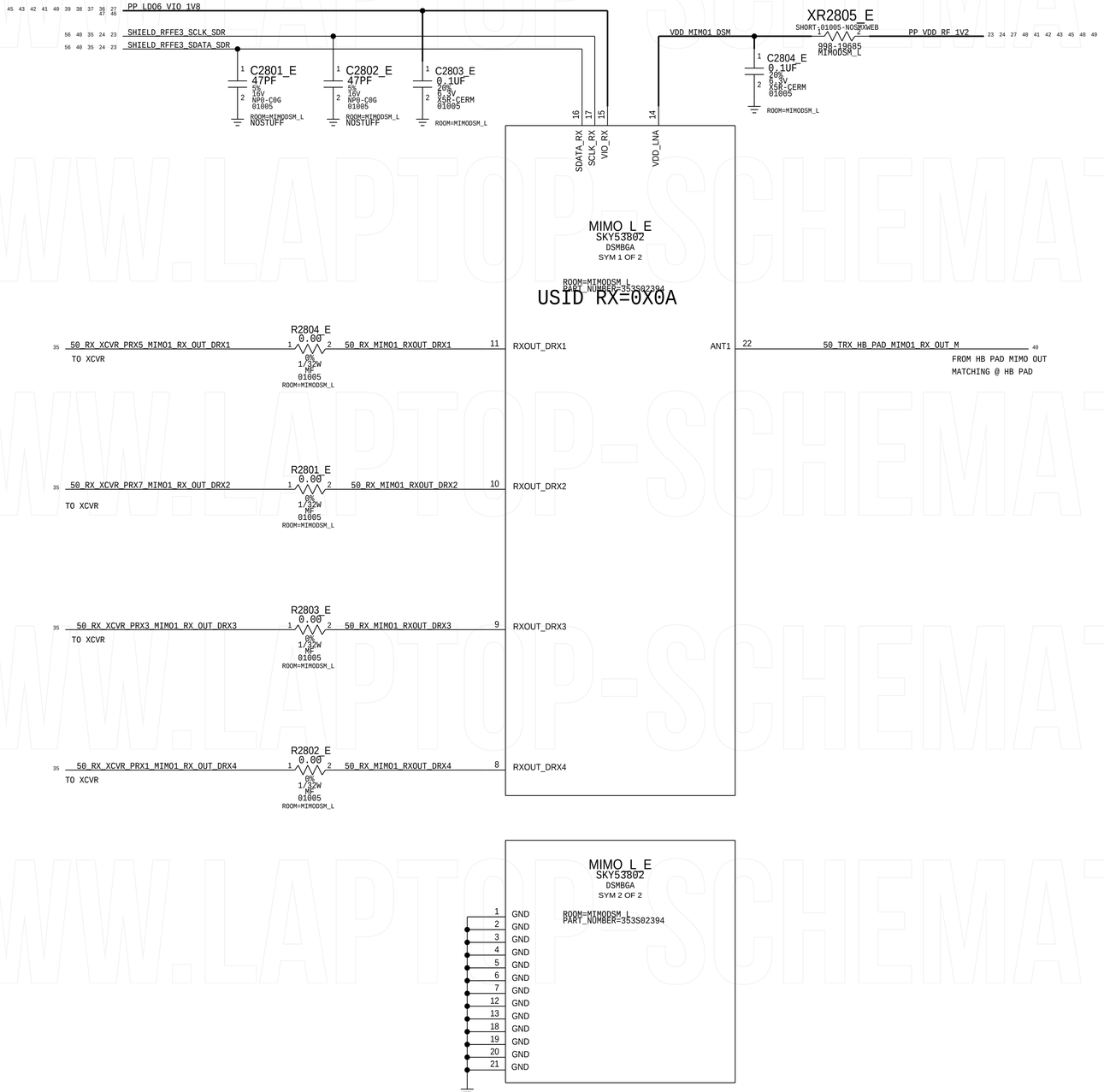
LOWER MIMO DIVERSITY MODULE



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PAGE TITLE

MIMO DSM LOWER

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UPPER MIMO DIVERSITY MODULE

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MIMO_U_E
SKY53802
DSMBGA
SYM 2 OF 2
ROOM=MIMODSM_U
PART_NUMBER=353S02394

1	GND
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
12	GND
13	GND
18	GND
19	GND
20	GND
21	GND

44 43 42 41 40 39 38 37 36 27 47 46 PP_LDO6_VIO_1V8

56 43 42 41 35 24 23 SHIELD_RFFE5_SCLK_SDR

56 43 42 41 35 24 23 SHIELD_RFFE5_SDATA_SDR

XR2905_E
SHORT-01005-NOSMXWEB
998-19605
MIMODSM_U

VDD_MIMO2_DSM — PP_VDD_RF_1V2 — 23 24 27 40 41 42 43 44 48 49

C2904_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MIMODSM_U

MIMO_U_E
SKY53802
DSMBGA
SYM 1 OF 2
ROOM=MIMODSM_U
PART_NUMBER=353S02394

16	SDATA_RX
17	SCLK_RX
15	VIO_RX
14	VDD_LNA
11	RXOUT_DRX1
10	RXOUT_DRX2
9	RXOUT_DRX3
8	RXOUT_DRX4
22	ANT1

USID RX=0X0A

R2904_E 0.00 0% 1/32W MF 01005 ROOM=MIMODSM_U

35 50_RX_XCVR_DRX5_MIMO2_RX_OUT_DRX1 — TO XCVR

50_RX_MIMO2_RXOUT_DRX1

R2901_E 0.00 0% 1/32W MF 01005 ROOM=MIMODSM_U

35 50_RX_XCVR_DRX7_MIMO2_RX_OUT_DRX2 — TO XCVR

50_RX_MIMO2_RXOUT_DRX2

R2903_E 0.00 0% 1/32W MF 01005 ROOM=MIMODSM_U

35 50_RX_XCVR_DRX3_MIMO2_RX_OUT_DRX3 — TO XCVR

50_RX_MIMO2_RXOUT_DRX3

R2902_E 0.00 0% 1/32W MF 01005 ROOM=MIMODSM_U

35 50_RX_XCVR_DRX1_MIMO2_RX_OUT_DRX4 — TO XCVR

50_RX_MIMO2_RXOUT_DRX4

ANT1 22 — 50_TRX_HBDSM_MIMO2_RX_OUT_M 42

FROM HB DSM MIMO OUT
MATCHING @ HB DSM

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MIMO DSM UPPER

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LOWER COUPLER

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PP_LDO6_VIO_1V8

SHIELD_RFFE1_SCLK_SDR

SHIELD_RFFE1_SDATA_SDR

C3003_E
47PF
5%
16V
NP0-C0G
01005
CPLR_L

PP_VDD_BOOST_SOUTH_PA

C3004_E
47PF
5%
16V
NP0-C0G
01005
CPLR_L

LB LMB/MB/HB DPLX -> CPLR_L -> ANT1

1.0NH-+/-0.1NH-0.9A-0.05OHM

R3004_E
01005
CPLR_L
152S00492

50_TRX_LB_PAD_ANT1

50_TRX_LB_PAD_ANT1_M

L3001_E
10NH-+/-3%-0.25A
01005
NOSTUFF
CPLR_L

TO LB LMB/MB/HB DPLX -> CPLR_L -> ANT1

1.3NH-+/-0.05NH-0.7A

R3003_E
01005
CPLR_L
152S01110

50_TRX_HB_PAD_ANT1

50_TRX_HB_PAD_ANT1_M

C3010_E
0.2PF
+/-0.05PF
16V
C0G-CERM
01005
CPLR_L
131S0893

C3007_E
0.5PF
+/-0.05PF
16V
C0G-CERM
01005
CPLR_L
NOSTUFF

PART_NUMBER=155S00619
ROOM=CPLR_L

DPLX1_E
LFD21788MPAKF237
LGA

LB
MLB_MB_HB
ANT
GND

50_TRX_DPLX_LB_LMB_MB_HB_ANT1

1.6NH-+/-0.1NH-0.70A

R3005_E
01005
CPLR_L
152S00423

C3008_E
0.5PF
+/-0.05PF
16V
C0G-CERM
01005
CPLR_L
131S0369

50_TRX_CPLR_L_CPL1_IN_LB_LMB_MB_HB

C3009_E
0.5PF
+/-0.05PF
16V
C0G-CERM
01005
CPLR_L
NOSTUFF

50_TRX_HB_PAD_ANT2_M

CPLR_L_E
MDFEXCGB-137
LGA
SYM 1 OF 2

PART_NUMBER=155S00618
ROOM=CPLR_L

USID=0X08

SDATA
SCLK
VIO
VDD
USID

CPL1_IN
CPL2_IN

CPL1_ANT

50_TRX_CPLR_L_CPL1_ANT_LB_LMB_MB_HB

0.8NH-+/-0.1NH-0.9A-0.05OHM

R3002_E
01005
152S00494
CPLR_L

50_TRX_ANT1_LB_LMB_MB_HB

C3005_E
0.5PF
+/-0.05PF
16V
C0G-CERM
01005
CPLR_L
NOSTUFF

C3006_E
0.5PF
+/-0.05PF
16V
C0G-CERM
01005
CPLR_L
NOSTUFF

TO LOWER ANT1

CPL2_ANT

50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB

TO WIFI/MBHB DPLX --> LOWER ANT3

CPL_OUT

50_CPLR_L_CPL1_LAT_OUT

TO SP3T

PART_NUMBER=155S00618
ROOM=CPLR_L

CPLR_L_E
MDFEXCGB-137
LGA
SYM 2 OF 2

4	GND	GND	19
5	GND	GND	20
7	GND	GND	21
8	GND	GND	22
9	GND	GND	23
13	GND	GND	24
14	GND	GND	25
16	GND	GND	26
17	GND	GND	27
18	GND	GND	30

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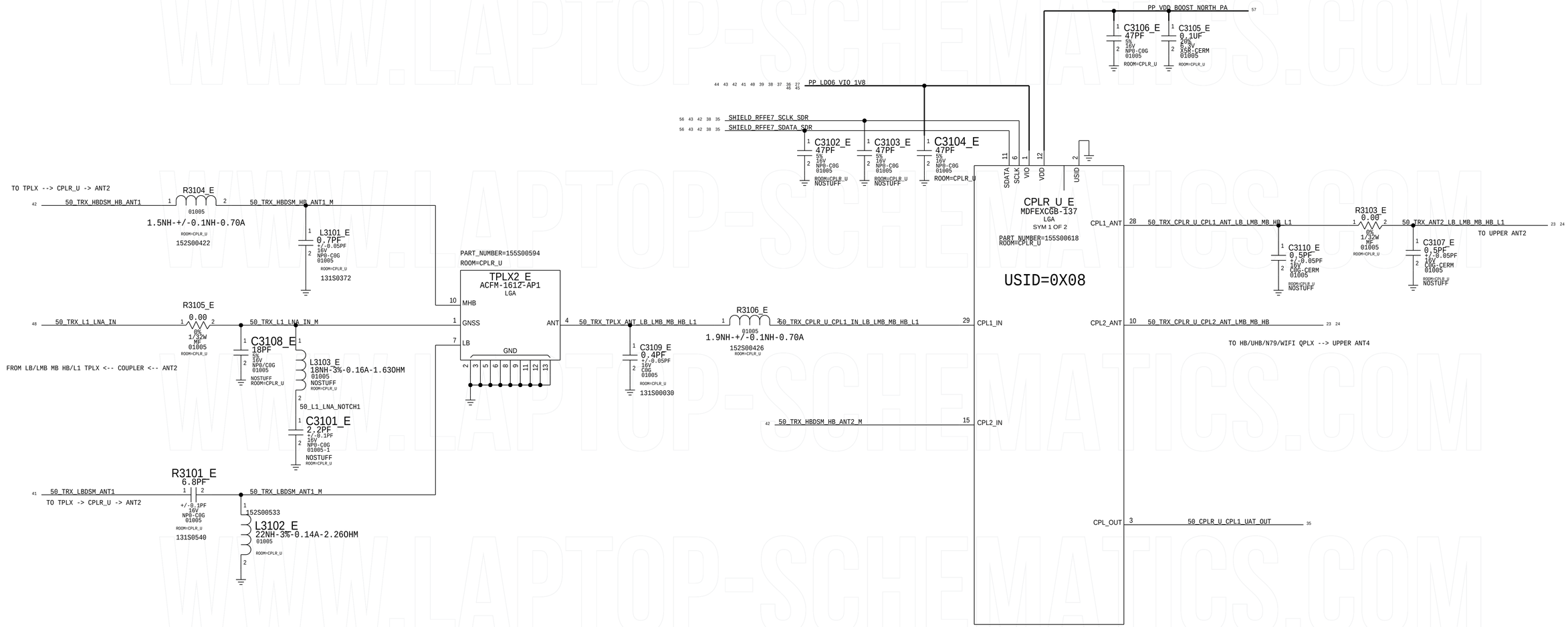
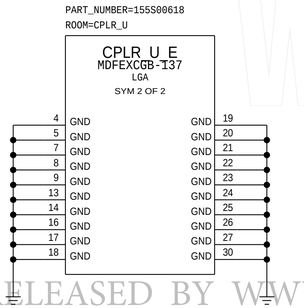
UPPER COUPLER





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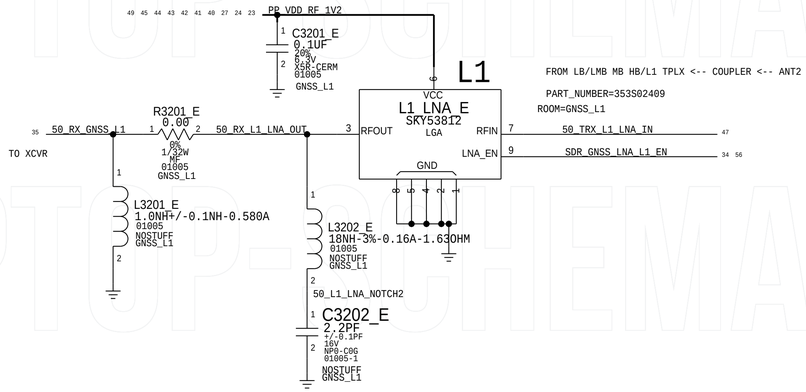
GNSS_L1



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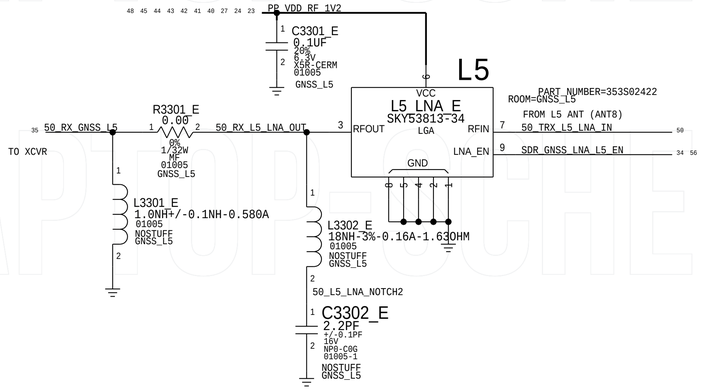
GNSS_L5



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LOWER ANTENNA FEEDS: ANT3

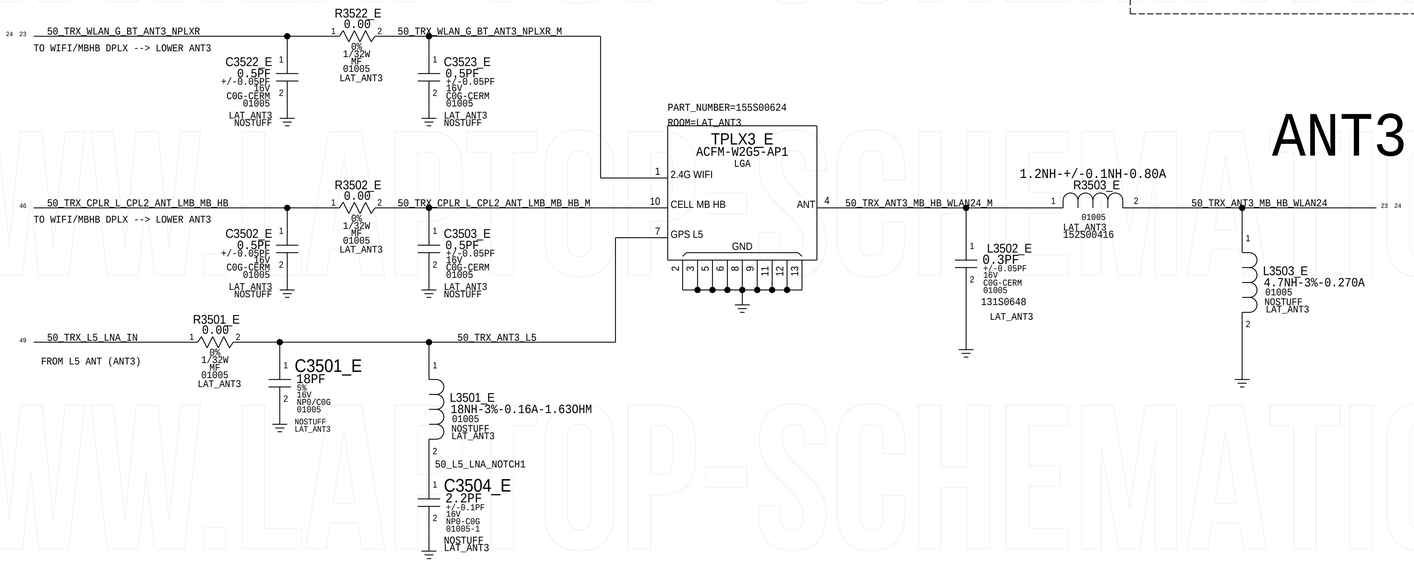
UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ L5 GNSS		N79	N79

ANT3



5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

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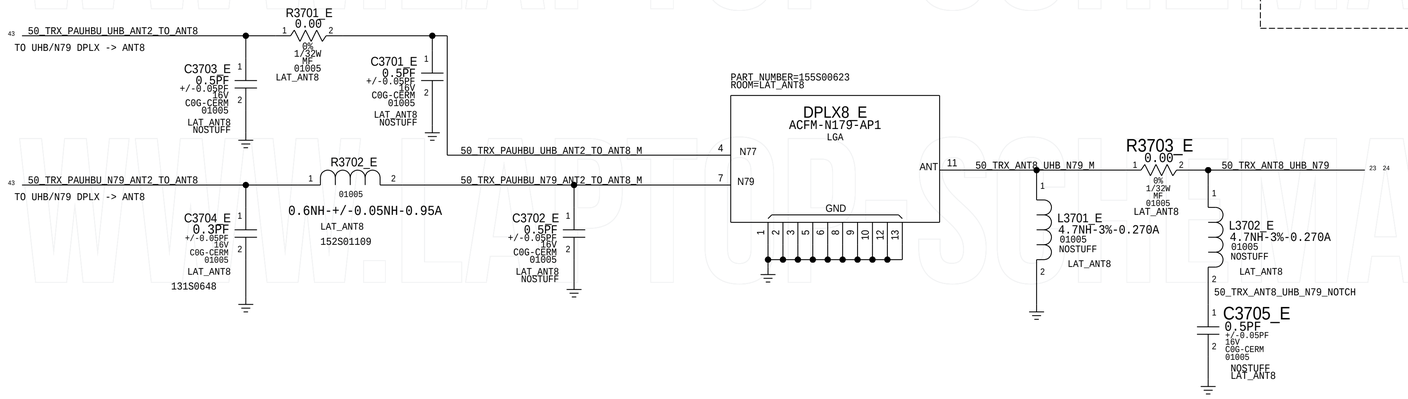
LOWER ANTENNA FEEDS: ANT8

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ L5 GNSS		N79	N79



ANT8

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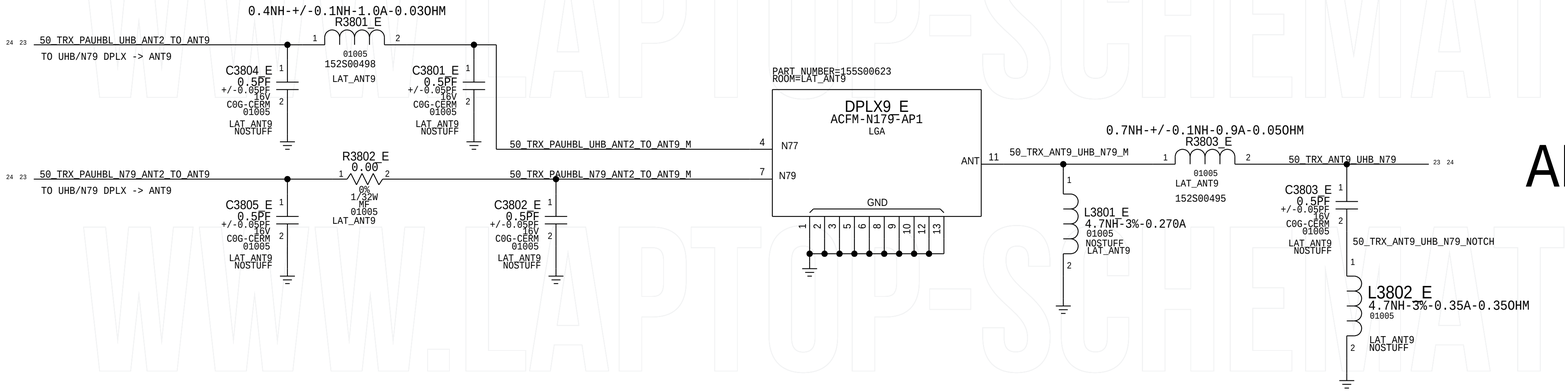
LOWER ANTENNA FEEDS: ANT9

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



ANT9

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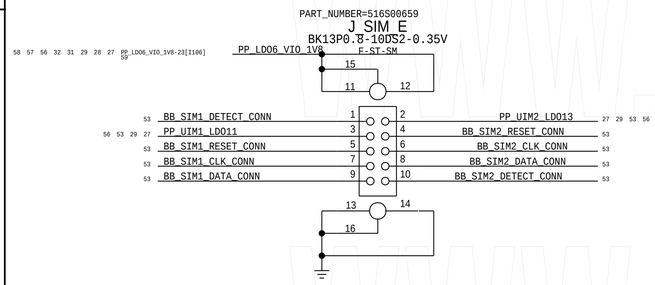
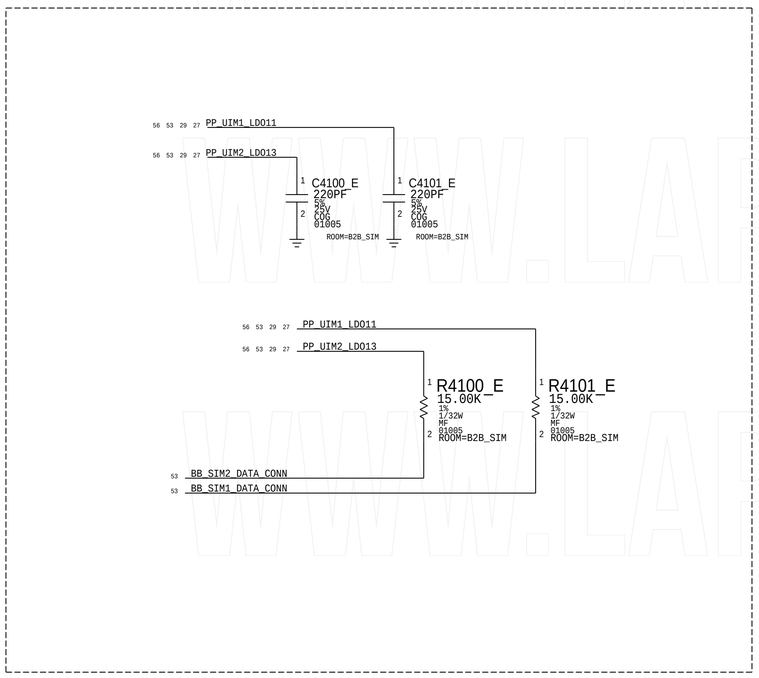
PSIM AND ESIM ARE ON FLEX
J_SIM_E (PLUG.APN:516S00659) ON MLB_BOT_MAV



Power Filters & Pull-ups



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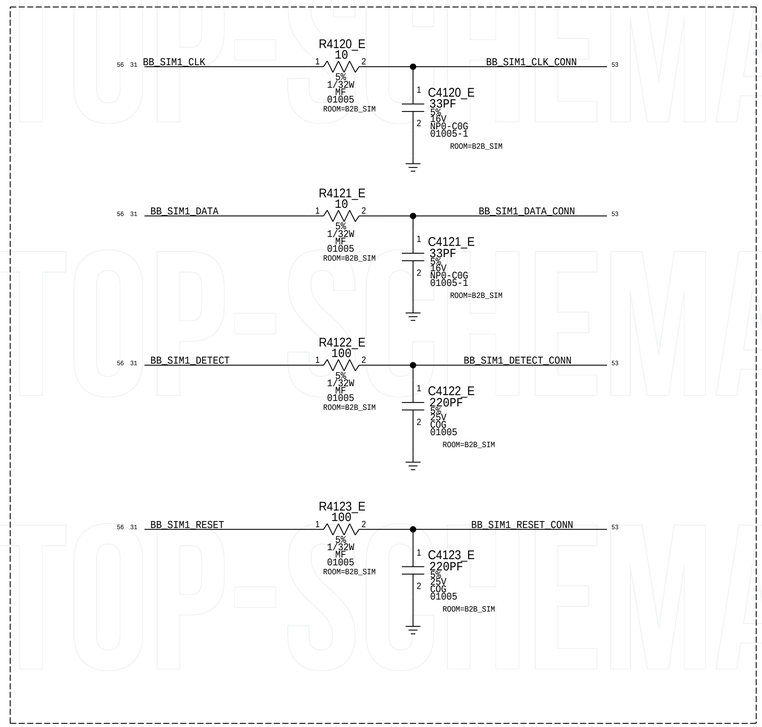
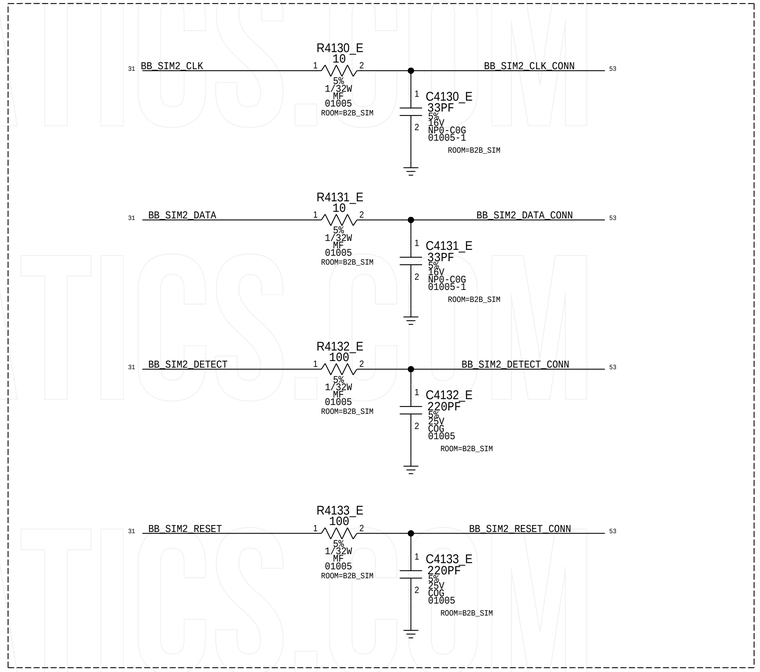
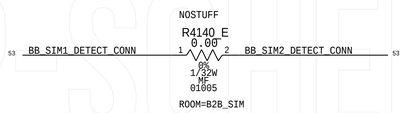


SIM2 IO Filters





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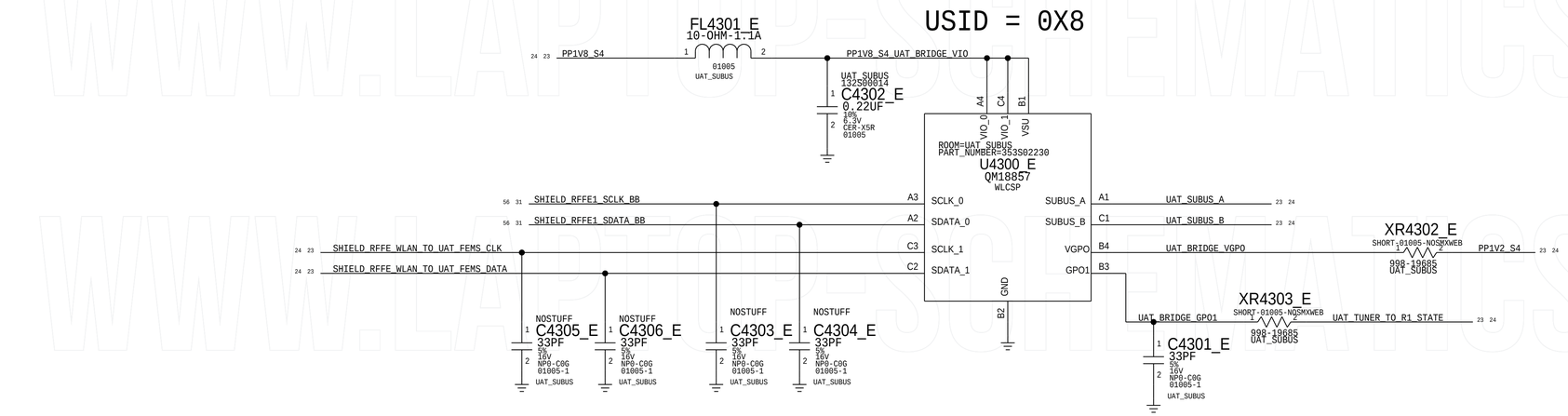
ANTENNA SYSTEM UAT



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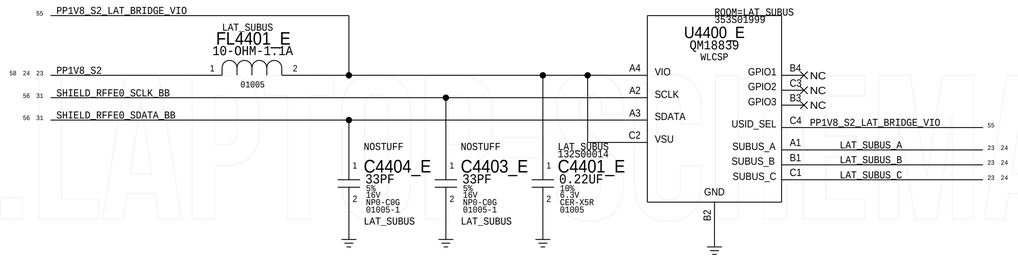
ANTENNA SYSTEM LAT

USID = 0X8 (SEL=VIO)
USID = 0XF (SEL=GND)



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DEBUG & BB PROBE POINTS

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NOSTUFF
ROOM=DEBUG
PART_NUMBER=516S00280

JDEBUG_E
BM29P-24DP-2-0.35V
M-ST-SM

57 56	PP_VDD_MAIN_PENINSULA	2	1	PP_VDD_MAIN_PENINSULA	56 57
58 28 24 23	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	4	3	PP3V0_DEBUG	58
		6	5	BB_JTAG_TDI	31
58 31	90_USB_BB_N	8	7	BB_JTAG_TDO	31
58 31	90_USB_BB_P	10	9	BB_JTAG_TRST_L	31
		12	11	BB_JTAG_RST_L	31
58 28	VBUS_DET_PMIC	14	13	UART_COEX_BB_TO_WLAN_TXD	23 24 31
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31	BB_JTAG_TMS_SWD_IO_1V8_R	18	17	UART1_AOP_TO_BB_TXD	23 24 31
53 31	BB_SIM1_RESET	20	19	UART1_AOP_FROM_BB_RXD	23 24 31
53 31	BB_SIM1_DETECT	22	21	BB_SIM1_CLK	31 53
56 53 29 27	PP_UIM1_LDO11	24	23	BB_SIM1_DATA	31 53
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PP4611_E	SHIELD_RFFE1_SDATA_SDR	23 24 35 36 40 46
PP4625_E		
PP4612_E	SHIELD_RFFE2_SCLK_SDR	23 24 35 39
PP4626_E		
PP4613_E	SHIELD_RFFE2_SDATA_SDR	23 24 35 39
PP4627_E		
PP4614_E	SHIELD_RFFE3_SCLK_SDR	23 24 35 40 44
PP4628_E		
PP4615_E	SHIELD_RFFE3_SDATA_SDR	23 24 35 40 44
PP4629_E		
PP4616_E	SHIELD_RFFE5_SCLK_SDR	23 24 35 41 42 43 45
PP4633_E		
PP4617_E	SHIELD_RFFE5_SDATA_SDR	23 24 35 41 42 43 45
PP4642_E		
PP4618_E	SHIELD_RFFE7_SCLK_SDR	35 38 42 43 47
PP4657_E		
PP4619_E	SHIELD_RFFE7_SDATA_SDR	35 38 42 43 47
PP4659_E		
PP4620_E	SHIELD_RFFE8_SCLK_SDR	23 24 35 37
PP4643_E		
PP4621_E	SHIELD_RFFE8_SDATA_SDR	23 24 35 37
PP4644_E		

BB RFFE

PP4645_E	SHIELD_RFFE0_SCLK_BB	31 55
PP4646_E		
PP4647_E	SHIELD_RFFE0_SDATA_BB	31 55
PP4648_E		
PP4652_E	SHIELD_RFFE1_SCLK_BB	31 54
PP4653_E		
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QLINK RFFE

PP4640_E	SHIELD_RFFE4_SCLK_BB	31 35 59
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QET DEBUG

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PP4699_E	PP_VDD_MAIN_QET_BBPMU_APTL	37

AP POWER

PP4675_E	PP_VDD_MAIN_PENINSULA	23 24 57
PP4676_E	PP_VDD_MAIN_QET_BBPMU_APTL	23 24 57
PP4678_E	PP_VDD_MAIN_QET_BBPMU_APTL	23 24 57 58
PP4679_E	PP_VDD_BOOST_NORTH_PA	23 24 57
PP4671_E	PP_VDD_BOOST_BBPMU	23 24 57
PP4672_E	PP_VDD_BOOST_SOUTH_PA	23 24 57
PP4698_E	PP3V0_S2	23 24 35 58

BB POWER

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PP4701_E	PP_1V22_SMPS2	26 27
PP4702_E	PP_0V82_SMPS3	26 27 29
PP4703_E	PP_1V9_SMPS4	26 27 60
PP4704_E	PP_0V75_SMPS5	26 29
PP4705_E	PP_0V75_SMPS7	26 27 29
PP4706_E	PP_1V2_LDO1	27 29 32
PP4707_E	PP_1V1_LDO2	27 29
PP4708_E	PP_0V8_LDO3	27 33
PP4709_E	PP_0V875_LDO4	27 29 32 59
PP4710_E	PP_1V8_LDO5	27 29 59
PP4711_E	PP_LDO6_VIO_1V8	PP_LDO6_VIO_1V8-23[I106]
PP4712_E	PP_0V8_LDO7	27 59
PP4713_E	PP_0V8_LDO8	27 32
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PP4715_E	PP_3V1_LDO10	27 29
PP4716_E	PP_UIM1_LDO11	27 29 53 56
PP4717_E	PP_1V2_LDO12	27 59
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PP4719_E	PP_0V6_LDO14	27 29 31
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PCIE

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PP4635_E	90_PCIE_GP2_AP_TO_BB_REFCLK_N	23 24 31
PP4636_E	90_PCIE_GP2_AP_TO_BB_TX_P	23 24 31
PP4637_E	90_PCIE_GP2_AP_TO_BB_TX_N	23 24 31
PP4638_E	90_PCIE_GP2_AP_FROM_BB_RX_P	23 24 31
PP4639_E	90_PCIE_GP2_AP_FROM_BB_RX_N	23 24 31
PP4684_E	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	23 24 31 58
PP4685_E	PCIE_GP2_AP_TO_BB_PERST_L	23 24 31
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PP4608_E	SHIELD_SMR_38P4M_CLK	28 59
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PP4610_E	CLK_BBPMU_TO_NFC_38M4	23 24 28
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DOTARA

27 28 29 31 32 53 57 58 59

PP4632_E	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	23 24 28

BASEBAND

PP4658_E	GPIO_AP_TO_BB_TIME_MARK	23 24 31

UART_BB_TO_AOP_RXD ON DEBUG CONNECTOR

UART_AOP_TO_BB_TXD ON DEBUG CONNECTOR

UART_BB_TO_WLAN_COEX_TX_1V2 ON DEBUG CONNECTOR

UART_WLAN_TO_BB_COEX_RX_1V2 ON DEBUG CONNECTOR

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PP4654_E	GPIO_AOP_TO_BB_FORCE_PWM	23 24 28
PP4687_E	GPIO_AP_FROM_BB_RESET_DETECT_L	23 24 31

APPMU_TO_BBPMU_RESET_L ON DEBUG CONNECTOR

PP4680_E	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	23 24 31
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PP4660_E	PS_HOLD	28 31
PP4673_E	PMIC_RESOUT_L	28 31
PP4649_E	BB_EEPROM_I2C_SCL	31
PP4650_E	BB_EEPROM_I2C_SDA	31
PP4662_E	BB_BBPMU_SPMI_CLK	28 31
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PP4665_E	BOOT_CFG1	31 58
PP4666_E	BOOT_CFG2	31 58
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SWD

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PP4604_E	85_MMW_QLINK_L0_N	31 59

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PP4674_E	GPIO_BB_TO_R1_CH9_REQ	23 24 31
PP4668_E	GPIO_R1_TO_BB_CH9_COEX	23 24 31
PP4669_E	IO_R1_TO_BB_LAA_SW_CTRL	23 24 31

STOCKHOLM

PP4670_E	IO_NFC_TO_BBPMU_CLKREQ	23 24 28

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PP4630_E	SDR_GNSS_LNA_L1_EN	34 48
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PP4694_E	I2S2_AP_FROM_BB_BCLK	23 24 31
PP4695_E	I2S2_AP_FROM_BB_DIN	23 24 31
PP4696_E	I2S2_AP_FROM_BB_LRCLK	23 24 31

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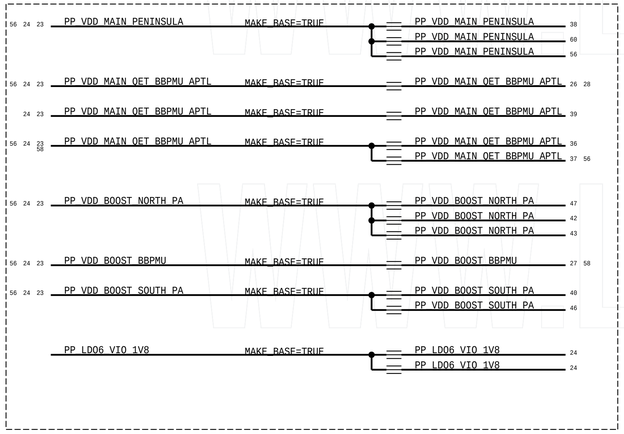

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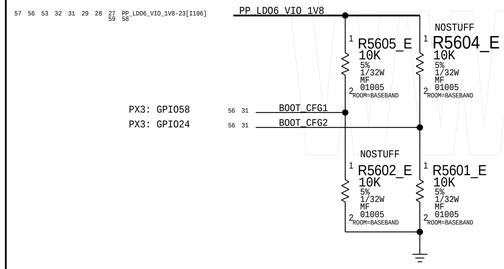
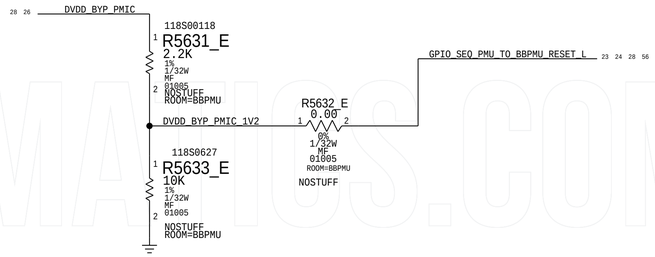
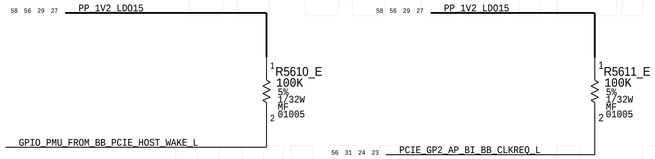


BOOT SEQ	BOOT_CFG3	BOOT_CFG2	BOOT_CFG1	CONFIG
NAND>HSUSB	0	0	0	
PCIE	0	0	1	POR
USB	0	1	0	EUREKA
EMMC>USB	0	1	1	

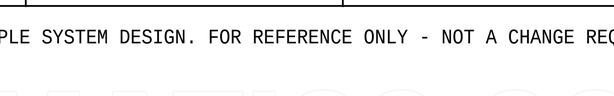
POR PCIE BOOT: BOOT_CFG1 PU, BOOT_CFG2 PD
EUREKA CONFIG USB BOOT: BOOT_CFG1 PD, BOOT_CFG2 PU

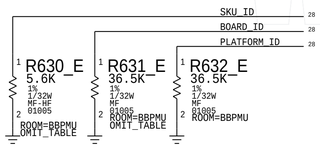
AUTO POWER ON FOR EUREKA CONFIG



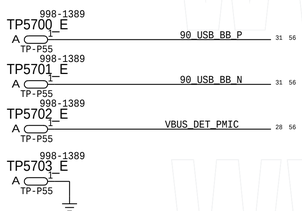


STUFF ONLY FOR VENDOR CONFIG





USB TP FOR TEXT FIXTURE



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MMW IF TRANSCEIVER IC

1.2A VDD_CX MAX CURRENT

56 27 PP_0V8_LDO7

138S00071
C5901_E
4UF
20%
6.3V
CER-X5R
0201
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5804_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5807_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5809_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5830_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

338S00651
BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 2 OF 3

B12	VDD_CX	VDDAH_1	A7
F12	VDD_CX	VDDAH_2	H4
M14	VDD_CX	VDDAH_3	P2
R7	VDD_CX	VDDAH_4	H8
P10	VDD_PX	VDDAL_1	C5
P12	VDD_MX	VDDAL_2	B4
H18	VDDA_PHY	VDDAL_3	F4
		VDDAL_4	R5
		VDDAL_5	B10
		VDDAL_6	E11
		VDDAL_7	R9
		VDDAM_1	B6
		VDDAM_2	G5
		VDDAM_3	P4
		VDDAM_4	A9
		VDDAM_5	P8

XW5801_E
SHORT-8L-0.1MM-SM

58 57 56 53 32 31 29 28 27 PP_LDO6_VIO_1V8-23[I106]

PP_LDO6_VIO_1V8

138S00071
C5802_E
4UF
20%
6.3V
CER-X5R
0201
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

PP_LDO6_SMR_VDD_PX_20

132S0316
C5805_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

XW5824_E
SHORT-8L-0.25MM-SM

56 32 29 27 PP_0V875_LDO4

138S00071
C5803_E
4UF
20%
6.3V
CER-X5R
0201
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

PP_LDO4_SMR_MX_115

XW5825_E
SHORT-8L-0.25MM-SM

PP_LDO4_SMR_PHY_152

132S0316
C5806_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5808_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

XW5802_E
SHORT-8L-0.1MM-SM

PP_LDO5_SMR_VDDAH_1_10

PP_1V8_LDO5 27 29 56

XW5803_E
SHORT-8L-0.25MM-SM

PP_LDO5_SMR_VDDAH_2_140

XW5804_E
SHORT-8L-0.1MM-SM

PP_LDO5_SMR_VDDAH_3_10

XW5805_E
SHORT-8L-0.1MM-SM

PP_LDO5_SMR_VDDAH_4_40

138S00071
C5823_E
4UF
20%
6.3V
CER-X5R
0201
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5812_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5814_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5818_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5820_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

XW5806_E
SHORT-8L-0.1MM-SM

PP_LDO9_SMR_VDDAL_1_50

PP_0V8_LDO9 27 56

XW5807_E
SHORT-8L-0.1MM-SM

PP_LDO9_SMR_VDDAL_2_10

138S00071
C5828_E
4UF
20%
6.3V
CER-X5R
0201
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

XW5809_E
SHORT-8L-0.1MM-SM

PP_LDO9_SMR_VDDAL_4_90

XW5810_E
SHORT-8L-0.1MM-SM

PP_LDO9_SMR_VDDAL_5_10

XW5811_E
SHORT-8L-0.1MM-SM

PP_LDO9_SMR_VDDAL_6_10

XW5812_E
SHORT-8L-0.1MM-SM

PP_LDO9_SMR_VDDAL_7_10

132S0316
C5810_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5813_E
0.47UF
20%
6.3V
X5R
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

PLACE C5813 CLOSE TO PIN B4

132S0316
C5816_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5819_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5822_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5825_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5826_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

XW5813_E
SHORT-8L-0.1MM-SM

PP_LDO12_SMR_VDDAM_1_70

XW5814_E
SHORT-8L-0.25MM-SM

PP_LDO12_SMR_VDDAM_2_120

XW5815_E
SHORT-8L-0.1MM-SM

PP_LDO12_SMR_VDDAM_3_70

PP_1V2_LDO12 27 56

VDD_AM MAX CURRENT 740 MA

138S00071
C5827_E
4UF
20%
6.3V
CER-X5R
0201
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5811_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5815_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5817_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5821_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

132S0316
C5824_E
0.1UF
20%
6.3V
X5R-CERM
01005
ROOM=MMW_IFIC
RF_SKU:WW+KOLKATA

338S00651
BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 1 OF 3

56 28 SHIELD_SMR_38P4M_CLK

	A3	XO_IN	XO	QLINK_L0_P	K14
	G9	XO_SEL		QLINK_L0_M	J15
	J1	IFH1	IF	QLINK_L1_P	G15
60 50_MMW_SMR526_IFH2	K2	IFH2		QLINK_L1_M	F14
60 50_MMW_SMR526_IFH3	L1	IFH3		QLINK_L2_P	E15
	M2	IFH4		QLINK_L2_M	D16
	F2	IFV1		QLINK_L3_P	L15
60 50_MMW_SMR526_IFV2	E1	IFV2		QLINK_L3_M	M16
60 50_MMW_SMR526_IFV3	D2	IFV3		QLINK_L4_P	P16
	C1	IFV4		QLINK_L4_M	R15
60 SMR_TO_FEZ_PON	P6	GRFC_1_QTM3_PON	QLINK PHY	QLINK_L5_P	D18
	G7	GRFC_2_QTM0_PON		QLINK_L5_M	E17
	K10	GRFC_3		QLINK_L6_P	B16
	J7	GRFC_4_QTM1_PON		QLINK_L6_M	A15
60 SMR_TO_TANGIER_PON	N5	GRFC_5_QTM2_PON		QLINK_L7_P	K18
	D12	GRFC_6	GRFC	QLINK_L7_M	J17
	M12	GRFC_7		QLINK_L8_P	L17
	N11	GRFC_8		QLINK_L8_M	M18
	H12	GRFC_9		QLINK_L9_P	P18
	J11	GRFC_10		QLINK_L9_M	R17
56 35 31 SHIELD_RFFE4_SDATA_BB	K12	RFFE0_DATA	RFFE	QLINK_L10_P	A13
56 35 31 SHIELD_RFFE4_SCLK_BB	L11	RFFE0_CLK		QLINK_L10_M	B14
	C11	DNC	DNC	QLINK_L11_P	B18
				QLINK_L11_M	A17
56 31 QLINK_REQ_SMR_TO_BB	D14	QLINK_REQ		QLINK_L12_P	R13
56 31 QLINK_EN_BB_TO_SMR	G13	QLINK_EN		QLINK_L12_M	P14
56 31 BB_TO_SMR_WMSS_RESET_L	J13	WMSS_RESET*		QLINK_CLK_P	G17
				QLINK_CLK_M	F18

QLINK_L0_P	31 56	85_MMW_QLINK_L0_P	
QLINK_L0_M	31 56	85_MMW_QLINK_L0_N	
QLINK_L1_P	31	85_MMW_QLINK_L1_P	
QLINK_L1_M	31	85_MMW_QLINK_L1_N	
QLINK_L2_P	31	85_MMW_QLINK_L2_P	
QLINK_L2_M	31	85_MMW_QLINK_L2_N	
QLINK_L3_P	31	85_MMW_QLINK_L3_P	
QLINK_L3_M	31	85_MMW_QLINK_L3_N	
QLINK_L4_P	31	85_MMW_QLINK_L4_P	
QLINK_L4_M	31	85_MMW_QLINK_L4_N	
QLINK_L5_P	31	85_MMW_QLINK_L5_P	
QLINK_L5_M	31	85_MMW_QLINK_L5_N	
QLINK_L6_P	31	85_MMW_QLINK_L6_P	
QLINK_L6_M	31	85_MMW_QLINK_L6_N	
QLINK_L7_P	31	85_MMW_QLINK_L7_P	
QLINK_L7_M	31	85_MMW_QLINK_L7_N	
QLINK_L8_P	31	85_MMW_QLINK_L8_P	
QLINK_L8_M	31	85_MMW_QLINK_L8_N	
QLINK_L9_P	31	85_MMW_QLINK_L9_P	
QLINK_L9_M	31	85_MMW_QLINK_L9_N	
QLINK_L10_P	31	85_MMW_QLINK_L10_P	
QLINK_L10_M	31	85_MMW_QLINK_L10_N	
QLINK_L11_P	31	85_MMW_QLINK_L11_P	
QLINK_L11_M	31	85_MMW_QLINK_L11_N	
QLINK_L12_P	31	85_MMW_QLINK_L12_P	
QLINK_L12_M	31	85_MMW_QLINK_L12_N	
QLINK_CLK_P	31	85_MMW_QLINK_CLK_P	
QLINK_CLK_M	31	85_MMW_QLINK_CLK_N	

338S00651
RF_SKU:WW+KOLKATA
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 3 OF 3

A1	GND	GND	H10
A5	GND	GND	H14
A11	GND	GND	H16
B2	GND	GND	J3
B8	GND	GND	J5
C3	GND	GND	J9
C7	GND	GND	K4
C9	GND	GND	K6
C13	GND	GND	K8
C15	GND	GND	K16
C17	GND	GND	L3
D4	GND	GND	L5
D6	GND	GND	L7
D8	GND	GND	L9
D10	GND	GND	L13
E3	GND	GND	M4
E5	GND	GND	M6
E7	GND	GND	M8
E9	GND	GND	M10
E13	GND	GND	N1
F6	GND	GND	N3
F8	GND	GND	N7
F10	GND	GND	N9
F16	GND	GND	N13
G1	GND	GND	N15
G3	GND	GND	N17
G11	GND	GND	R1
H2	GND	GND	R3
H6	GND	GND	R11

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SYNC_DATE=07/30/2019

PAGE TITLE
MMW

DRAWING NUMBER 051-05262
SIZE D
REVISION 6.0.0
BRANCH evt-0
PAGE 59 OF 191
SHEET

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TANGIER SIP

RELEASED BY WWW.LAPTOP-SCHEMATICS.COM

59 SMR_TO_TANGIER_PON — 79 V_ON

ROOM=MMW_SIP
C5932_E 56PF 5% 16V NP0/C0G 01005 NOSTUFF

PP5901_E P2MM-NSM SM 1 TANGIER_TP1 — 386 TP1
PP5902_E P2MM-NSM SM 1 TANGIER_TP2 — 379 TP2
PP5903_E P2MM-NSM SM 1 TANGIER_TP3 — 380 TP3
PP5904_E P2MM-NSM SM 1 TANGIER_TP4 — 319 TP4
PP5905_E P2MM-NSM SM 1 TANGIER_TP5 — 378 TP5
PP5906_E P2MM-NSM SM 1 TANGIER_TP6 — 375 TP6
PP5907_E P2MM-NSM SM 1 TANGIER_TP7 — 376 TP7
PP5908_E P2MM-NSM SM 1 TANGIER_RFFE_CLK — 358 RFFE_CLK
PP5909_E P2MM-NSM SM 1 TANGIER_RFFE_DATA — 377 RFFE_DATA
PP5910_E P2MM-NSM SM 1 50_TANGIER_TP11 — 298 TP11

59 50_MMW_SMR526_IFH2 — 373 50_IF1_H
59 50_MMW_SMR526_IFV3 — 382 50_IF2_V

60 57 PP_VDD_MAIN_PENINSULA — BOMOPTION=RF_SKU:WW+KOLKATA
C5901_E 100PF 20% 25V C0G-CERM 01005 ROOM=MMW_SIP
68 VBATT
69 VBATT
90 VBATT
91 VBATT
92 VBATT

60 56 27 26 PP_1V9_SMPS4 — MAKE_BASE=TRUE — PP_1V9_SMPS4 — 42 VDD_IO_1V85
C5902_E 100PF 20% 25V C0G-CERM 01005 ROOM=MMW_SIP

BOMOPTION=RF_SKU:WW+KOLKATA

BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_SIP
U_TAN_E
TANGIER-ES2
SIP
SYM 1 OF 4

50_RFH_Q1_39G_S1	209	50_MMW_SMR525_S1H_HPOL	61
50_RFH_Q1_28G_S1	208	50_MMW_SMR525_S1L_HPOL	61
50_RFH_Q1_39G_S2	210	50_MMW_SMR525_S2H_HPOL	61
50_RFH_Q1_28G_S2	211	50_MMW_SMR525_S2L_HPOL	61
50_RFH_Q1_39G_S3	335		
50_RFH_Q1_28G_S3	334		
50_RFH_Q1_39G_S4	336		
50_RFH_Q1_28G_S4	337		
50_RFH_Q2_39G_S5	206	50_MMW_SMR525_S5H_HPOL	61
50_RFH_Q2_28G_S5	207	50_MMW_SMR525_S5L_HPOL	61
50_RFH_Q2_39G_S6	205	50_MMW_SMR525_S6H_HPOL	61
50_RFH_Q2_28G_S6	204	50_MMW_SMR525_S6L_HPOL	61
50_RFH_Q2_39G_S7	332	50_MMW_SMR525_S7H_HPOL	60
50_RFH_Q2_28G_S7	333	50_MMW_SMR525_S7L_HPOL	60
50_RFH_Q2_39G_S8	331	50_MMW_SMR525_S8H_HPOL	60
50_RFH_Q2_28G_S8	330	50_MMW_SMR525_S8L_HPOL	60
50_RFV_Q3_39G_S9	216	50_MMW_SMR525_S9H_VPOL	61
50_RFV_Q3_28G_S9	217	50_MMW_SMR525_S9L_VPOL	61
50_RFV_Q3_39G_S10	215	50_MMW_SMR525_S10H_VPOL	61
50_RFV_Q3_28G_S10	214	50_MMW_SMR525_S10L_VPOL	61
50_RFV_Q3_39G_S11	342	50_MMW_SMR525_S11H_VPOL	60
50_RFV_Q3_28G_S11	343	50_MMW_SMR525_S11L_VPOL	60
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50_RFV_Q4_39G_S14	220	50_MMW_SMR525_S14H_VPOL	61
50_RFV_Q4_28G_S14	221	50_MMW_SMR525_S14L_VPOL	61
50_RFV_Q4_39G_S15	345		
50_RFV_Q4_28G_S15	344		
50_RFV_Q4_39G_S16	346		
50_RFV_Q4_28G_S16	347		

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BOMOPTION=RF_SKU:WW+KOLKATA
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MM3631-2701A16
F-ST-SM

50_MMW_SMR525_S11L_VPOL	60	2	21
50_MMW_SMR525_S7L_HPOL	60	4	11
50_MMW_SMR525_S12H_VPOL	60	6	23
50_MMW_SMR525_S8H_HPOL	60	8	24
		9	50_MMW_SMR525_S11H_VPOL 60
		18	22
		19	13
		20	15
		17	16
		25	35
		3	12
		26	34
		5	14
		27	33
		7	16
		28	36
		29	37
		30	38
		31	39
		32	40
		1	10
			50_MMW_SMR525_S7H_HPOL 60
			50_MMW_SMR525_S8L_HPOL 60
			50_MMW_SMR525_S12L_VPOL 60

BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_SIP
U_TAN_E
TANGIER-ES2
SIP
SYM 2 OF 4

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2	GND	67	GND	137	GND	201	GND
3	GND	70	GND	138	GND	202	GND
4	GND	71	GND	139	GND	203	GND
5	GND	72	GND	140	GND	212	GND
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63	GND	133	GND	197	GND	277	GND
64	GND	134	GND	198	GND	278	GND
65	GND	135	GND	199	GND	279	GND

BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_SIP
U_TAN_E
TANGIER-ES2
SIP
SYM 3 OF 4

1	GND	66	GND	136	GND	200	GND
2	GND	67	GND	137	GND	201	GND
3	GND	70	GND	138	GND	202	GND
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38	GND	109	GND	173	GND	253	GND
39	GND	110	GND	174	GND	254	GND
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46	GND	116	GND	180	GND	260	GND
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51	GND	121	GND	185	GND	265	GND
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BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_SIP
U_TAN_E
TANGIER-ES2
SIP
SYM 4 OF 4

280	GND	GND	323
281	GND	GND	324
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283	GND	GND	326
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287	GND	GND	338
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316	GND	GND	383
317	GND	GND	384
318	GND	GND	385
320	GND	GND	387
321	GND	GND	388
322	GND		

SIDE FIRE

BOMOPTION=RF_SKU:WW+KOLKATA
ROOM=MMW_SIP
FL5911_E 0 0% 1/8W TF 0402

60 57 PP_VDD_MAIN_PENINSULA — PP_VBAT_FEZ

C5911_E	330PF 10% 16V CER-X7R 01005	BOMOPTION=RF_SKU:WW+KOLKATA
C5912_E	220PF 5% 25V C0G 01005	BOMOPTION=RF_SKU:WW+KOLKATA
C5913_E	470PF 10% 16V CER-X7R 01005	BOMOPTION=RF_SKU:WW+KOLKATA
C5914_E	680PF 10% 16V X7R 01005	BOMOPTION=RF_SKU:WW+KOLKATA

ROOM=MMW_SIP
J_FEZ_E
SMT-FLEX-FEZ-3L-X1803
SMT-PAD

1	GND0	50_MMW_SMR526_IFV2	59
2	GND1	50_MMW_SMR526_IFH3	59
3	GND2		
4	PON		
5	GND3		
6	IFV		
7	GND4		
8	1P85V		
9	GND5		
10	GND6		
11	GND7		
12	VBAT0		
13	GND8		
14	GND9		
15	GND10		
16	VBAT1		
17	GND11		
18	IFH		
19	GND12		
20	VBAT2		
21	GND13		
22	GND14		
23	GND15		
24	VBAT3		

0R HOLDERS

ROOM=MMW_SIP
FL5921_E 0 0% 1/10W LF 0201
60 56 27 26 PP_1V9_SMPS4 — 1.85V PP_1V85_FEZ
BOMOPTION=RF_SKU:WW+KOLKATA

C5921_E	330PF 10% 16V CER-X7R 01005	ROOM=MMW_SIP
C5922_E	220PF 5% 25V C0G 01005	NOSTUFF

BOMOPTION=RF_SKU:WW+KOLKATA

ROOM=MMW_SIP
FL5931_E 0.00 0% 1/20W MF 01005
59 SMR_TO_FEZ_PON — V_PON_FEZ
BOMOPTION=RF_SKU:WW+KOLKATA

ROOM=MMW_SIP
C5931_E 56PF 5% 16V NP0/C0G 01005 NOSTUFF

50_MMW_SMR526_IFH3 NET CONNECTS TO 50_IF1_H AND
50_MMW_SMR526_IFV2 NET CONNECTS TO 50_IF2_V IN FEZ FLEX

SYNC_DATE=07/30/2019

PAGE TITLE
TANGIER SIP

DRAWING NUMBER 051-05262 SIZE D
REVISION 6.0.0
BRANCH evt-0
PAGE 60 OF 191
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SAISS FLEX SHOULD BE ASSEMBLED TO MLB
WITH APN 632-03618

BG1 ARRAY

ROOM=BG1
BOMOPTION=RF_SKU:WW+KOLKATA
PART_NUMBER=998-21064

U_BG1_E
ANTENNA-BG1-ES3
LGA
SYM 1 OF 3

60	50_MMW_SMR525_S6L_HPOL	244	50_LB1_H	50_HB1_H	235	50_MMW_SMR525_S6H_HPOL	60
60	50_MMW_SMR525_S14L_VPOL	236	50_LB1_V	50_HB1_V	243	50_MMW_SMR525_S14H_VPOL	60
60	50_MMW_SMR525_S1L_HPOL	309	50_LB2_H	50_HB2_H	298	50_MMW_SMR525_S1H_HPOL	60
60	50_MMW_SMR525_S9L_VPOL	299	50_LB2_V	50_HB2_V	307	50_MMW_SMR525_S9H_VPOL	60
60	50_MMW_SMR525_S5L_HPOL	278	50_LB3_H	50_HB3_H	266	50_MMW_SMR525_S5H_HPOL	60
60	50_MMW_SMR525_S13L_VPOL	267	50_LB3_V	50_HB3_V	277	50_MMW_SMR525_S13H_VPOL	60
60	50_MMW_SMR525_S2L_HPOL	338	50_LB4_H	50_HB4_H	328	50_MMW_SMR525_S2H_HPOL	60
60	50_MMW_SMR525_S10L_VPOL	300	50_LB4_V	50_HB4_V	308	50_MMW_SMR525_S10H_VPOL	60

ROOM=BG1
BOMOPTION=RF_SKU:WW+KOLKATA
PART_NUMBER=998-21064

U_BG1_E
ANTENNA-BG1-ES3
LGA
SYM 2 OF 3

1	GND	GND	97
2	GND	GND	98
3	GND	GND	99
4	GND	GND	100
5	GND	GND	101
6	GND	GND	102
7	GND	GND	103
8	GND	GND	104
9	GND	GND	105
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13	GND	GND	109
14	GND	GND	110
15	GND	GND	111
16	GND	GND	112
17	GND	GND	113
18	GND	GND	114
19	GND	GND	115
20	GND	GND	116
21	GND	GND	117
22	GND	GND	118
23	GND	GND	119
24	GND	GND	120
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92	GND	GND	188
93	GND	GND	189
94	GND	GND	190
95	GND	GND	191
96	GND	GND	192

ROOM=BG1
BOMOPTION=RF_SKU:WW+KOLKATA
PART_NUMBER=998-21064

U_BG1_E
ANTENNA-BG1-ES3
LGA
SYM 3 OF 3

193	GND	GND	293
194	GND	GND	294
195	GND	GND	295
196	GND	GND	296
197	GND	GND	297
198	GND	GND	301
199	GND	GND	302
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225	GND	GND	332
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227	GND	GND	334
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274	GND	GND	376
275	GND		
276	GND		
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287	GND		
288	GND		
289	GND		
290	GND		
291	GND		
292	GND		

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SYNC_DATE=07/30/2019

PAGE TITLE
BG1 ARRAY

DRAWING NUMBER 051-05262
SIZE D
REVISION 6.0.0
BRANCH evt-0
PAGE 61 OF 191
SHEET

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0022732381	ENGINEERING RELEASED	2020-03-28

D53 HIER_WIFI_BOT - EVT

LAST_MODIFICATION=Fri Mar 27 22:24:40 2020

PAGE	CSA	CONTENTS	SYNC	DATE
62	1	Table of Contents		
63	2	THELONIOUS	D52_WIFI_MASTER_0.21.0	
64	5	5G rFEM (LAT)	D52_WIFI_MASTER_0.21.0	

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/SOFT	SYNC_DATE/TIME
D52	WIFI_MASTER	2,5	0.21.0	S	2019_12_07_19:14:40

SYMBOL IO PORTS

POWER

MAKE_BASE=TRUE

22	IO	PP_VDD_MAIN_PENINSULA	VOLTAGE=4.2	=	=	PP_VDD_MAIN_PENINSULA	63
64	22 IO	PP_VDD_MAIN_5GFEML	VOLTAGE=4.2				
63	22 IO	PP1V8_S4	VOLTAGE=1.8				
64	22 IO	PP1V8_S2	VOLTAGE=1.8				
63	22 IO	PP1V2_S4	VOLTAGE=1.2				

ANTENNA

64 22 IO 50_WLAN_A_LAA_ANT5

RFEM CONNECTIONS

RF

63 22 IO 50_WLAN_A_C0_TXRX_FEM_M
63 22 IO 50_WLAN_G_C0_TXRX_FEM_M
63 22 IO 50_WLAN_G_C1_TXRX_FEM_M

ANALOG

63 22 IO ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
63 22 IO ANALOG_UAT_2G_FEM_TO_WLAN_PDTS
63 22 IO ANALOG_LAT_2G_FEM_TO_WLAN_PDTS

GPIO

63 22 IO GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
63 22 IO GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN
63 22 IO GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN

RFFE

63 22 IO RFFE_WLAN_TO_UAT_5G_FEM_RST_L
63 22 IO RFFE_WLAN_TO_UAT_2G_FEM_RST_L
63 22 IO SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
63 22 IO SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
63 22 IO RFFE_WLAN_TO_LAT_2G_FEM_RST_L
64 63 22 IO SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
64 63 22 IO SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA

AP CONNECTIONS

63 22 IO GPIO_AP_FROM_WLAN_TIME_SYNC
63 22 IO GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG
63 22 IO GPIO_AP_FROM_BT_AUDIO_SYNC

PCIE

63 22 IO PCIE_GP1_AP_TO_WLAN_PERST_L
63 22 IO PCIE_GP1_AP_BI_WLAN_CLKREQ_L
63 22 IO 90_PCIE_GP1_AP_TO_WLAN_TX_P
63 22 IO 90_PCIE_GP1_AP_TO_WLAN_TX_N
63 22 IO 90_PCIE_GP1_AP_FROM_WLAN_RX_P
63 22 IO 90_PCIE_GP1_AP_FROM_WLAN_RX_N
63 22 IO 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
63 22 IO 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N

AOP CONNECTIONS

63 22 IO SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
63 22 IO SPMI0_EVENTS_AOP_BI_WLAN_DATA_R
63 22 IO GPIO_AOP_TO_WLAN_CONTEXT_A
63 22 IO GPIO_AOP_TO_WLAN_CONTEXT_B

CELLULAR CONNECTIONS

63 22 IO UART_COEX_BB_TO_WLAN_TXD
63 22 IO UART_COEX_BB_FROM_WLAN_RXD
64 22 IO PP_LDO6_VIO_1V8
64 22 IO SHIELD_RFFE3_SCLK_SDR
64 22 IO SHIELD_RFFE3_SDATA_SDR
64 22 IO 50_RX_LAA_XCVR_PRX12

PMU CONNECTIONS

63 22 IO GPIO_S4_PMU_TO_WLAN_REG_ON
63 22 IO GPIO_PMU_FROM_WLAN_HOST_WAKE
63 22 IO CLK_GPIO_S4_PMU_TO_WLAN_R1_32K

SE CONNECTIONS

63 22 IO I2C_BT_TO_NFC_SCL
63 22 IO I2C_BT_TO_NFC_SDA
63 22 IO GPIO_SE_TO_BT_PKT_RDY

R1 CONNECTIONS

63 22 IO GPIO_R1_TO_WLAN_COEX
63 22 IO GPIO_WLAN_TO_R1_COEX
63 22 IO IO_BT_TO_R1_TIME_SYNC
63 22 IO IO_BT_TO_R1_WAKE

SPKR CONNECTIONS

63 22 RT GPIO_BT_TO_BOT_SPKR_TRIG

D53 SPECIFIC IMPLEMENTATION

- NONE

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DRAWING TITLE: SCH,MLB,BOT,MAV,D53

DRAWING NUMBER: 051-05262 | SIZE: D
REVISION: 6.0.0
BRANCH: evt-0
PAGE: 62 OF 191
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WIFI/BT THELONIOUS

5G INTERSTATE BPFS

FL_ISG_U_W
ACPF-7350-AP1
LGA

FL_ISG_L_W
ACPF-7350-AP1
LGA

U_WLAN_W
THELONIOUS-U-ES4.3
LGA
2103-601901-80
SYM 1 OF 2

U_WLAN_W
THELONIOUS-U-ES4.3
LGA
2103-601901-80
SYM 2 OF 2

SENSOR A = DOTARA
SENSOR B = SE
SENSOR C = R1

PAGE TITLE: THELONIOUS

DRAWING NUMBER: 051-05262
SIZE: D
REVISION: 6.0.0
BRANCH: evt-0
PAGE: 63 OF 191
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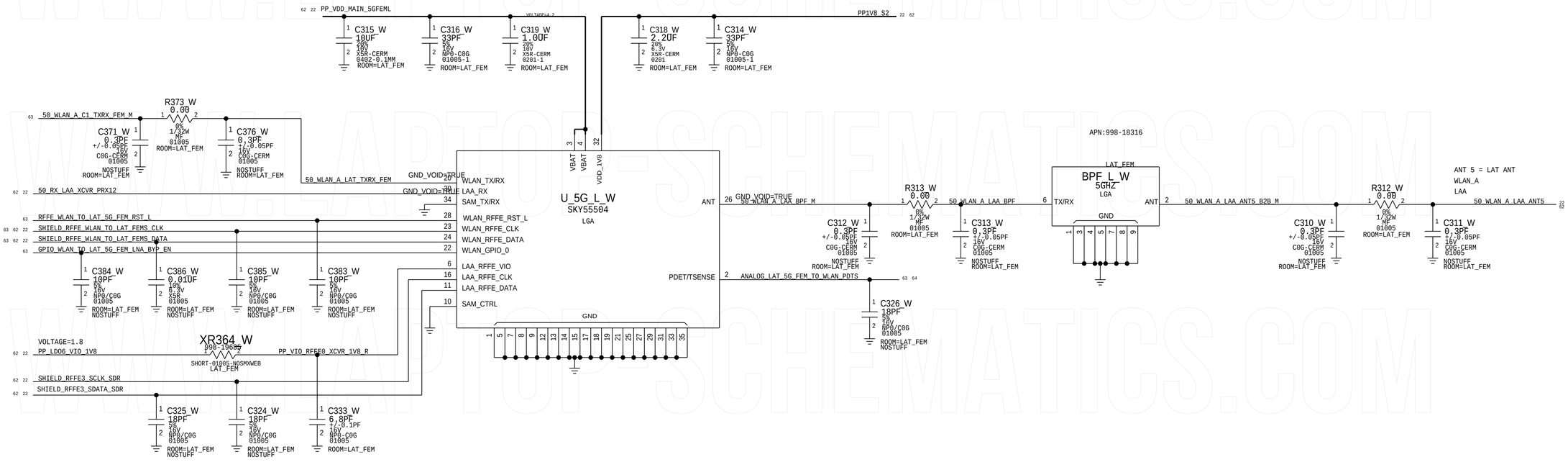
LAT 5GHZ RFEM



OMIT SM_PP208_W P2MM-NSM ROOM=WLAN — PP — ANALOG_LAT_5G_FEM_TO_WLAN_PDTS

OMIT SM_PP220_W P2MM-NSM ROOM=WLAN — PP — SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK

OMIT SM_PP221_W P2MM-NSM ROOM=WLAN — PP — SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA

PAGE TITLE	5G rFEM (LAT)
DRAWING NUMBER	051-05262
SIZE	D
REVISION	6.0.0
BRANCH	evt-0
PAGE	64 OF 191
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D53 Top MLB

EVT

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4			2020-04-03

LAST_MODIFICATION=Fri Apr 3 17:41:42 2020

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	TABLE OF CONTENTS		
2	2	SYSTEM: BOM Tables	D52_AP_MASTER_3.50.0	
3	3	CONSTRAINTS: Impedance Controlled		
4	4	CONSTRAINTS: Power		
5	5	CONSTRAINTS: Misc.		
6	6	CONSTRAINTS: Stackup/Misc. (FF-Specific)		
7	7	SYSTEM: Bootstrapping	D52_AP_MASTER_3.50.0	
8	10	SOC: NAND + USB & Misc	D52_AP_MASTER_3.50.0	
9	11	SOC: PCIE	D52_AP_MASTER_3.50.0	
10	12	SOC: ISP	D52_AP_MASTER_3.50.0	
11	13	SOC: Display	D52_AP_MASTER_3.50.0	
12	14	SOC: Serial	D52_AP_MASTER_3.50.0	
13	15	SOC: GPIO	D52_AP_MASTER_3.50.0	
14	16	SOC: AOP & SMC & NUB	D52_AP_MASTER_3.50.0	
15	17	SOC: Ocelot	D52_AP_MASTER_3.50.0	
16	18	SOC: Power (CPU/GPU & SRAM & SOC)	D52_AP_MASTER_3.50.0	
17	19	SOC: Power (Fixed & 1V2)	D52_AP_MASTER_3.50.0	
18	20	SOC: Power (DDR & AOP/AVE/ISP/USB)	D52_AP_MASTER_3.50.0	
19	21	SOC: Power (GND)	D52_AP_MASTER_3.50.0	
20	23	SOC: Aliases: I2C AP/ISP	D52_AP_MASTER_3.50.0	
21	24	SOC: Aliases: I2C AOP/SMC	D52_AP_MASTER_3.50.0	
22	25	SOC: Aliases: GPIOs	D52_AP_MASTER_3.50.0	
23	26	SOC: Aliases: Misc	D52_AP_MASTER_3.50.0	
24	27	SOC: Aliases: FF-Specific		
25	29	NAND	D52_AP_MASTER_3.50.0	
26	31	NAND: Aliases	D52_AP_MASTER_3.50.0	
27	33	SYS PWR: PMU: Bucks (1/5)	D52_AP_MASTER_3.50.0	
28	34	SYS PWR: PMU: Bucks (2/5)	D52_AP_MASTER_3.50.0	
29	35	SYS PWR: PMU: LDOs (3/5)	D52_AP_MASTER_3.50.0	
30	36	SYS PWR: PMU: GPIO (4/5)	D52_AP_MASTER_3.50.0	
31	37	SYS PWR: PMU: Misc (5/5)	D52_AP_MASTER_3.50.0	
32	38	SYS PWR: PMU: Aliases: GPIO	D52_AP_MASTER_3.50.0	
33	39	SYS PWR: PMU: Aliases: Misc.	D52_AP_MASTER_3.50.0	
34	40	SYS PWR: Charger	D52_AP_MASTER_3.50.0	
35	41	SYS PWR: VDD_MAIN Sense Resistor	D52_AP_MASTER_3.50.0	
36	42	SYS PWR: Boost	D52_AP_MASTER_3.50.0	
37	43	SYS PWR: WiFi FEM Load Switches	D52_AP_MASTER_3.50.0	
38	44	SYS PWR: Wireless Charger	D52_AP_MASTER_3.50.0	
39	45	SYS PWR: Wireless Charger: Level Shifters	D52_AP_MASTER_3.50.0	
40	46	SYS PWR: Wireless Charger: Boost	D52_AP_MASTER_3.50.0	
41	47	SYS PWR: Wireless Charger: Aliases	D52_AP_MASTER_3.50.0	
42	48	SYS PWR: Aliases: FF Specific		
43	49	SYS PWR: NTCs (Top)	D52_AP_MASTER_3.50.0	
44	50	SYS PWR: NTCs (Bottom)		
45	52	CAMERA: P/G Variant	D52_AP_MASTER_3.50.0	

LAST_MODIFICATION=Fri Apr 3 17:41:42 2020

PAGE	CSA	CONTENTS	SYNC	DATE
46	53	CAMERA: PMU 1: Power (1/2)	D52_AP_MASTER_3.50.0	
47	54	CAMERA: PMU 1: I/O (2/2)	D52_AP_MASTER_3.50.0	
48	55	CAMERA: PMU 1: Aliases	D52_AP_MASTER_3.50.0	
49	56	CAMERA: PMU 2: Power (1/2)	D52_AP_MASTER_3.50.0	
50	57	CAMERA: PMU 2: I/O (2/2)	D52_AP_MASTER_3.50.0	
51	58	CAMERA: PMU 2: Aliases	D52_AP_MASTER_3.50.0	
52	59	CAMERA: Discrete LDOs	D52_AP_MASTER_3.50.0	
53	64	CAMERA: Will	D52_AP_MASTER_3.50.0	
54	66	CAMERA: Will: Aliases	D52_AP_MASTER_3.50.0	
55	70	PEARL: VCSEL Driver	D52_AP_MASTER_3.50.0	
56	71	PEARL: Aliases	D52_AP_MASTER_3.50.0	
57	78	AUDIO: Codec: Analog (1/2)	D52_AP_MASTER_3.50.0	
58	79	AUDIO: Codec: Power & I/O (2/2)	D52_AP_MASTER_3.50.0	
59	80	AUDIO: Bot Speaker Amp	D52_AP_MASTER_3.50.0	
60	81	AUDIO: Top Speaker Amp	D52_AP_MASTER_3.50.0	
61	83	HAPTIC: Haptic Amp	D52_AP_MASTER_3.50.0	
62	84	HAPTIC: Sakonnet	D52_AP_MASTER_3.50.0	
63	89	TOP MODULE: Touch Power	D52_AP_MASTER_3.50.0	
64	91	TOP MODULE: Display Power	D52_AP_MASTER_3.50.0	
65	93	LIGHTNING: Lightning Controller	D52_AP_MASTER_3.50.0	
66	94	LIGHTNING: USB-PD	D52_AP_MASTER_3.50.0	
67	95	LIGHTNING: Accessory Buck	D52_AP_MASTER_3.50.0	
68	96	LIGHTNING: eUSB	D52_AP_MASTER_3.50.0	
69	97	LIGHTNING: Aliases	D52_AP_MASTER_3.50.0	
70	99	LVL SHIFT: Misc Nets	D52_AP_MASTER_3.50.0	
71	100	B2B: Battery		
72	101	B2B: Cyclone		
73	104	B2B: RCAM: Single-flex		
74	105	B2B: RCAM: Super-flex		
75	106	B2B: Jasper		
76	107	B2B: FCAM		
77	108	B2B: Pearl: Juliet		
78	109	B2B: Pearl: Romeo		
79	110	B2B: Sensor		
80	111	B2B: Strobe		
81	112	B2B: Dock		
82	115	B2B: Display		
83	116	B2B: Touch		09/20/2019
84	120	B2B: UAT1		
85	121	B2B: UAT2		
86	125	MECHANICAL: Standoffs, Fiducials, Etc.		10/17/2019
87	126	TESTING: Test Points		
88	127	TESTING: Test Points (FF-Specific)		
89	128	TESTING: Probe Points		
90	129	TESTING: Probe Points (FF-Specific)		

LAST_MODIFICATION=Fri Apr 3 17:41:42 2020

PAGE	CSA	CONTENTS	SYNC	DATE
91	130	INTERPOSER: Symbol (1/2)		
92	131	INTERPOSER: Symbol (2/2)		
93	132	INTERPOSER: Aliases (1/4)		
94	133	INTERPOSER: Aliases (2/4)		
95	134	INTERPOSER: Aliases (3/4)		
96	135	INTERPOSER: Aliases (4/4)		
97	139	INTERPOSER: Misc.		
98	140	HIER: Arrow		
99	142	HIER: NFC		
100	150	HIER: WiFi		
101	160	HIER: Radio		
102	1	FRONT PAGE		
103	2	MODULE		
104	3	FILTERS MATCHING		
105	1	NFC: TABLE OF CONTENTS		
106	74	NFC_P		
107	75	NFC_P_FE		
108	76	NFC_F		
109	1	FRONT PAGE		
110	20	LB PAD		07/30/2019
111	22	UHB LAT PAD		07/30/2019
112	23	LMB_2G_PAD		07/30/2019
113	36	LOWER ANTENNA FEEDS_ANT7		07/30/2019
114	39	UPPER ANTENNA FEEDS_ANT4		07/30/2019
115	1	Table of Contents		
116	4	5G rFEM (UAT)	D52_WIFI_MASTER_0.19.0	
117	7	2G4 rFEM (UAT)	D52_WIFI_MASTER_0.19.0	
118	8	2G4 rFEM (LAT)	D52_WIFI_MASTER_0.19.0	

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-08619	MRNT	CRITICAL	EEEE:08619
825-7691	1	EEEE FOR 639-10097	NY3J	CRITICAL	EEEE:10097
825-7691	1	EEEE FOR 639-10099	NY47	CRITICAL	EEEE:10099
825-7691	1	EEEE FOR 639-10096	NY35	CRITICAL	EEEE:10096
825-7691	1	EEEE FOR 639-10098	NY3W	CRITICAL	EEEE:10098
825-7691	1	EEEE FOR 639-10100	NY4L	CRITICAL	EEEE:10100
825-7691	1	EEEE FOR 639-10101	NY4Y	CRITICAL	EEEE:10101
825-7691	1	EEEE FOR 639-10103	NY5X	CRITICAL	EEEE:10103
825-7691	1	EEEE FOR 639-10107	NY73	CRITICAL	EEEE:10107
825-7691	1	EEEE FOR 639-10102	NY59	CRITICAL	EEEE:10102
825-7691	1	EEEE FOR 639-10105	NY6M	CRITICAL	EEEE:10105
825-7691	1	EEEE FOR 639-10108	NY7G	CRITICAL	EEEE:10108

APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05215	1	SCH,MLB_TOP,D53	SCH	CRITICAL	?
820-01955	1	PCB,MLB_TOP,D53	PCB	CRITICAL	?

Sub-designs

Hierarchies

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/ SOFT	SYNC_DATE/TIME	FORCE SUBDESIGN
D52	HIER_ARROW	0.42.0	S	2020_03_30_21:49:04	Y
D53	HIER_NFC_TOP	0.29.0	S	2020_03_30_22:03:02	Y
D53	HIER_RADIO_MAV_TOP	1.26.0	S	2020_04_02_13:14:28	Y
D53	HIER_WIFI_TOP	0.25.0	S	2020_03_30_21:47:34	Y

Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	AP_MASTER	2,7,10-21,23-26,29,31,33-47,49,52-59,64,66,70-71,78-81,83-84,89,91,93-97,99	3.50.0	S	2020_04_02_13:16:58

Packaging Options

PACK_OPTIONS TO INCLUDE IN NETLIST
D53

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DRAWING TITLE: SCH,MLB,TOP,D53

DRAWING NUMBER: 051-05215 SIZE: D

REVISION: 4.6.0

BRANCH:

PAGE: 65 OF 191

SHEET:

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Multi-Vendor Criticals

Capacitors

In descending order of value, then package size

CRITICAL PART#	COMMENT
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
132S0663	CAP,CER,X5R,1UF,10%,25V,0402
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
132S00008	CAP,CER,0.1UF,10%,50V,X7R,0402
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S0664	CAP,CER,0.047UF,10%,25V,X5R,0201
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S00093	CAP,X5R,0.022UF,20%,6.3V,01005
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S0396	CAP,CER,X5R,1000PF,10%,10V,01005
132S0296	CAP,CER,X5R,1000PF,10%,6.3V,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
131S0883	CAP,CER,NP0/C0G,220PF,2%,50V,0201
131S00170	CAP,CER,C0G,220PF,5%,25V,01005
131S00053	CAP,CER,C0G,220PF,5%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
131S0307	CAP,CER,NP0/C0G,100PF,5%,16V,01005

Capacitors (cont'd)

CRITICAL PART#	COMMENT
131S00303	CAP,CER,NPO/C0G,100PF,5%,16V,01005
131S00323	CAP,CER,NPO/C0G,56PF,5%,25V,01005
131S0643	CAP,CER,NP0/C0G,56PF,5%,25V,01005
131S0216	CAP,CER,NP0/C0G,47PF,5%,16V,01005
131S0804	CAP,CER,27PF,5%,C0G,25V,0201
131S0223	CAP,CER,NP0/C0G,27PF,5%,16V,01005
131S0215	CAP,CER,NPO/C0G,22PF,5%,16V,01005
131S0225	CAP,CER,NP0/C0G,15PF,5%,16V,01005
131S0220	CAP,CER,NP0/C0G,12PF,5%,16V,01005
131S00353	CAP,CER,NPO/C0G,10PF,5%,16V,01005

Ferrites

CRITICAL PART#	COMMENT
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605

Resistors

CRITICAL PART#	COMMENT
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
117S0055	RES,MF,1/20W,2M OHM,5,0201,SMD

Misc.

CRITICAL PART#	COMMENT
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005

2020 MLCCs

16uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00316	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402	Primary: Murata
138S00314	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402	Taiyo
138S00315	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402	Kyocera
					Samsung

11uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00318	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T	Primary: Murata
138S00319	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T	Kyocera
138S00320	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T	Samsung
					Taiyo

2.7uF, 0201, 6.3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00326	138S00325	?	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201	Primary: Murata
138S00327	138S00325	?	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201	Kyocera
					Samsung

2.7uF, 0201, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00324	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201	Primary: Murata
138S00322	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201	Taiyo
138S00323	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201	Kyocera
					Samsung

MAV20 PDN Single-source

0.22uF, 01005

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Kyocera

(C700,E-C750,E-C751,E-C752,E-C753,E-C757,E-C758,E-C761,E-C762,E-C764,E-C765,E-C766,E-C767,E-C770,E-C771,E-C774,E-C776,E-C778,E-C780,E)
(C700,E-C750,E-C751,E-C752,E-C753,E-C757,E-C758,E-C761,E-C762,E-C764,E-C765,E-C766,E-C767,E-C770,E-C771,E-C774,E-C776,E-C778,E-C780,E)

2.2uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	[SEE BELOW]	CAP,CER,X5R,2.2UF,20%,6.3V,0201

(C700,E-C702,E-C704,E-C721,E-C722,E-C726,E-C729,E-C732,E-C733,E-C734,E-C741,E-C744,E-C747,E-C748,E-C751,E-C752,E-C754,E-C756,E-C757,E-C759,E-C760,E-C772,E-C777,E-C780,E)

4uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C511,E-C518,E-C522,E-C524,E-C526,E-C702,E-C704,E-C708,E-C709,E-C777,E-C787,E-C788,E-C1138,E-C1142,E-C1226,E-C1227,E-C5001,E-C5003,E-C5023,E-C5027,E-C5028,E)
(C511,E-C518,E-C522,E-C524,E-C526,E-C702,E-C704,E-C708,E-C709,E-C777,E-C787,E-C788,E-C1138,E-C1142,E-C1226,E-C1227,E-C5001,E-C5003,E-C5023,E-C5027,E-C5028,E)

Capacitor Alternates

0.1uF, 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	?	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005

CRITICAL PART#	COMMENT
132S0316	01005,0.1uF, 6.3V

0.22uF, 01005

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?		01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?		01005,0.22uF,6.3V,Kyocera

CRITICAL PART#	COMMENT
132S00014	01005,0.22uF, 6.3V

0.47uF, 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00133	138S00128	?	ALL	01005,0.47uF,6.3V,Murata
138S00269	138S00128	?	ALL	01005,0.47uF,6.3V,Taiyo

CRITICAL PART#	COMMENT
138S00128	01005,0.47uF, 6.3V

1uF, 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA

CRITICAL PART#	COMMENT
138S0706	CAP,X5R,1UF,20%,10V,0201

2.2uF, 0201

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?		CAP,CER,X5R,2.2UF,20%,6.3V,0201

CRITICAL PART#	COMMENT
138S0831	CAP,CER,X5R,2.2UF,20%,6.3V,0201

3uF @ 1V, 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	?	ALL	0201,3uF@1V,KYOCERA
138S00164	138S00139	?	ALL	0201,3uF@1V,TAIYO
138S00280	138S00139	?	ALL	0201,3uF@1V,SAMSUNG

CRITICAL PART#	COMMENT
138S00139	0201,3uF@1V

4uF, 0201

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?		CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?		CAP,X5R,4UF,0201,0.55MM,KYOCERA

CRITICAL PART#	COMMENT
138S00071	0201,X5R,4UF,0201,0.55MM,MURATA

4.7uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1103	138S0719	?	ALL	CAP,CER,X5R,4.7UF,20%,10V,0402

CRITICAL PART#	COMMENT
138S0719	0402,4.7uF,10V

15uF, 0402

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?		0402,15uF,6.3V, Kyocera

(C1805,C3321,C1872,C3371,C3382)

CRITICAL PART#	COMMENT
138S00003	0402,15uF,6.3V

18uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00221	138S00146	?	ALL	CAP,CER,X5R,18UF,20%,6.3V,MUR,0402

CRITICAL PART#	COMMENT
138S00146	CAP,CER,X5R,18UF,20%,6.3V,MUR,0402

20uF, 0402

All parts are single-sourced except for approved parts (listed below)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00339	138S0884	?		Taiyo
138S00338	138S0884	?		Kyocera

C3302,C3312,C3333,C3350,C3364,C1893,C3412,C3423,C3525,C3535,C3403,C1807,C1866,C1874,C2030
C3302,C3312,C3333,C3350,C3364,C1893,C3412,C3423,C3525,C3535,C3403,C1807,C1866,C1874,C2030

CRITICAL PART#	COMMENT
138S0884	CAP,CER,X5R,20UF,20%,6.3V,0402,H=0.7MM

22uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	?	ALL	CAP,X5R,26UF,20%,4V,MURATA,0402
138S00143	138S00279	?	ALL	CAP,X5R,22UF,20%,4V,KYOCERA,0402

CRITICAL PART#	COMMENT
138S00279	CAP,X5R,26UF,20%,4V,MURATA,0402

10uF @ 1V, 4-Term

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00148	138S00149	?	ALL	0402-3T,10.5uF@1V, Kyocera
138S00150	138S00149	?	ALL	0402-3T,10.5uF@1V, SEMCO
138S00151	138S00149	?	ALL	0402-3T,10.5UF@1V, TY

CRITICAL PART#	COMMENT
138S00149	0402-3T,10.5uF@1V

22uF, 0402 3T (WiFi)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00024	138S0986	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
138S0986	CAP,CER,3-TERM,7.5UF,20%,4V,0402

Display Choke Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00415	155S00524	?	ALL	FLTR,NOISE,35 OHMZ,3 OHM,7GHZ,50MA,0403

CRITICAL PART#	COMMENT
155S00524	FLTR,NOISE,35 OHMZ,3 OHM,7GHZ,50MA,0403

Level Shifter Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S00231	311S00232	?	ALL	IC,74AVC2T45,XCVR,2 BIT,2 SPLY,X2SON8
311S00230	311S00212	?	ALL	IC,74AVC1T45,XCVR,1 BIT,2 SPLY,X2SON6
311S00261	311S00233	?	ALL	IC,LSF0101,XCVR,2 BIT CFG,2 SPLY,X2SON6

CRITICAL PART#	COMMENT
311S00232	IC,74AVC2T45,XCVR,2 BIT,2 SPLY,X2SON8
311S00212	IC,74AVC1T45,XCVR,1 BIT,2 SPLY,X2SON6
311S00233	IC,LSF0101,XCVR,2 BIT CFG,2 SPLY,X2SON6
311S00235	IC,NVT0202,XCVR,2 BIT, 2 SPLY,BIDI,DFN8

Power Inductor Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00721	152S00876	?	ALL	Taiyo,IND,MLD,1UH,3.6A,60MΩ,2016
152S00930	152S00897	?	ALL	Cyntec,IND,CPL/D,0.33M,6.1A,27MΩ,2016
152S00826	152S00821	?	ALL	Taiyo,IND,MLD,1UH,2.3A,68MΩ,2012
152S00831	152S00818	?	ALL	Taiyo,IND,MLD,0.22UH,5.3A,40MΩ,1608
152S00991	152S00984	?	ALL	Taiyo,IND,MLD,0.47UH,3.5A,34MΩ,1614
152S00992	152S00985	?	ALL	Taiyo,IND,MLD,0.47UH,4.0A,45MΩ,2012
152S00989	152S00982	?	ALL	Taiyo,IND,MULT,0.47UH,2.8A,79MΩ,1608
152S00824	152S00819	?	ALL	Taiyo,IND,MLD,1UH,20%,3A,69MΩ,H=0.65,2012
152S00872	152S00918	?	ALL	TDK,IND,MLD,0.47UH,5.6A,30MΩ,H=0.8,2016
152S00847	152S00918	?	ALL	CYNTEC,IND,MLD,0.47UH,5.6A,30MΩ,H=0.8,3010
152S01282	152S01255	?	ALL	TAIYO,IND,MLD,0.47UH,5A,38MΩ,H=0.65,2117

CRITICAL PART#	COMMENT
152S00876	Cyntec,IND
152S00897	Taiyo,IND
152S00821	Cyntec,IND
152S00818	Cyntec,IND
152S00984	Cyntec.IND
152S00985	Cyntec,IND
152S00982	Cyntec,IND
152S00819	Cyntec,IND

Boost/Yeti (2117/0.8mm)

Boost/Yeti (2117/0.65mm)

Misc. Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00437	155S00402	?	ALL	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00194	155S00400	?	ALL	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
155S00414	155S0876	?	ALL	FERR BD,190HM,50%,1.1A,0.05OHM DCR,01005
155S00131	155S0755	?	ALL	FERR BD,2400HM,25%,200MA,1.0OHM DCR,01005
155S00583	155S00140	?	ALL	FERR BD,330HM,25%,400MA,0.20DCR,01005
377S00070	377S00001	?	ALL	TVS,BIDIR,5.8V,6PF,01005
377S00140	377S00001	?	ALL	TVS,BIDIR,5V,6PF,01005
377S00168	377S00129	?	ALL	SUPPRESS,TRANS,6.8V,100PF,AMOTECH,01005
107S0245	107S0244	?	ALL	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

CRITICAL PART#	COMMENT
155S00402	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00400	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
155S0876	FERR BD,190HM,50%,1.1A,0.05OHM DCR,01005
155S0755	FERR BD,240 OHM,25%,200MA,1.0 DCR,01005
155S00140	FERR BD,330HM,25%,400MA,0.20DCR,01005
377S00001	TVS,BIDIR,5.8V,6PF,01005
377S00129	SUPRESS,TRANS,6.8V,100PF,01005
107S0244	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

ZRB Cap ALTs

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00240	138S00187	?	ALL	CAP,X5R,4.7UF,20%,25V,0402
138S00246	138S00185	?	ALL	CAP,X5R,2.2UF,20%,25V,0402

CRITICAL PART#	COMMENT
138S00175	CAP,X5R,4.7UF,20%,25V,0402
138S00185	CAP,X5R,2.2UF,20%,25V,0402

0-ohm, 0201, 4.5A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
117S00040	117S00012	?	ALL	RES,MF,0 OHM,1/10W,4.5A,0201

CRITICAL PART#	COMMENT
117S00012	RES,MF,0 OHM,1/10W,4.5A,0201

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PAGE TITLE: SYSTEM: BOM Tables

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Spacing CSet Definitions

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculate dielectric distance from min/max planned distance is used unless 1.X is defined	EXAMPLE: 1.5/1.7/1.9=.5/.7/.9 1.5,2,2.5,3,4
A_DIELECTRIC_(N)XO XV,XVL,X Calculate dielectric distance from min/max planned distance is used unless 1 defined	EXAMPLE: 2.2/4.2/7.2=.2/.4/.7 PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculate dielectric distance from min/max planned distance is used unless 1.X defined	EXAMPLE: 2.4,3L,3L ?

90-ohm Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	E_LPDP_WIDE	DIFF_PAIR	DP:DP_90_LPDP*_WIDE*	Y
	E_LPDP_SUPERFLEX-CAM2	DIFF_PAIR	DP:DP_90_LPDP*_SUPERFLEX_CAM2*	Y
	E_LPDP_SINGLEFLEX_CAM	DIFF_PAIR	DP:DP_90_LPDP*_SINGLEFLEX_CAM*	Y
	E_LPDP_FCAM	DIFF_PAIR	DP:DP_90_LPDP*_FCAM*	Y
	E_LPDP_JASPER	DIFF_PAIR	DP:DP_90_LPDP*_JASPER*	Y
MIPI	E_MIPI_DISPLAY	DIFF_PAIR_MIPI-D	DP:DP_90_MIPI*DISPLAY*	N
	E_MIPI_IRCAM	DIFF_PAIR_MIPI-C	DP:DP_90_MIPI*_IRCAM*	N
PCIE	E_PCIE_NAND	DIFF_PAIR	DP:DP_90_PCIE*_NAND*	Y
	E_PCIE_WLAN	DIFF_PAIR	DP:DP_90_PCIE*_WLAN*	Y
	E_PCIE_BB	DIFF_PAIR	DP:DP_90_PCIE*_BB*	Y
USB	E_KRAKEN_DP	DIFF_PAIR	DP:DP_90_KRAKEN*	Y
	E_MIKEYBUS_DP	DIFF_PAIR	DP:DP_90_MIKEYBUS*	Y
	E_USB_DP	DIFF_PAIR	DP:DP_90_USB*	Y
	E_EUSB_DP	DIFF_PAIR	DP:DP_90_EUSB*	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	90_LPDP_WIDE	A_90_OHM_DIFF	DP:DP_90_LPDP*_WIDE*	Y
	90_LPDP_SUPERFLEX_CAM2	A_90_OHM_DIFF	DP:DP_90_LPDP*_SUPERFLEX_CAM2*	Y
	90_LPDP_SINGLEFLEX_CAM	A_90_OHM_DIFF	DP:DP_90_LPDP*_SINGLEFLEX_CAM*	Y
	90_LPDP_FCAM	A_90_OHM_DIFF	DP:DP_90_LPDP*_FCAM*	Y
	90_LPDP_JASPER	A_90_OHM_DIFF	DP:DP_90_LPDP*_JASPER*	Y
MIPI-D	90_MIPI_DISPLAY	A_90_OHM_DIFF	DP:DP_90_MIPI*DISPLAY*	Y
MIPI-C	90_MIPI_IRCAM	A_90_OHM_DIFF	DP:DP_90_MIPI*_IRCAM*	Y
PCIE (Gen4)	90_PCIE_NAND	A_90_OHM_DIFF	DP:DP_90_PCIE*_NAND*	Y
	90_PCIE_BB	A_90_OHM_DIFF	DP:DP_90_PCIE*_BB*	Y
PCIE (Gen2)	90_PCIE_WLAN	A_90_OHM_DIFF	DP:DP_90_PCIE*_WLAN*	Y
USB	90_KRAKEN_DP	A_90_OHM_DIFF	DP:DP_90_KRAKEN*	Y
	90_USB_DP	A_90_OHM_DIFF	DP:DP_90_USB*	Y
	90_EUSB_DP	A_90_OHM_DIFF	DP:DP_90_EUSB*	Y
MIKEYBUS	90_MIKEYBUS_DP	A_90_OHM_DIFF	DP:DP_90_MIKEYBUS*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	90_LPDP_WIDE	A_DIELECTRIC_3X	=	Y
	90_LPDP_SUPERFLEX_CAM2	A_DIELECTRIC_3X	=	Y
	90_LPDP_SINGLEFLEX_CAM	A_DIELECTRIC_3X	=	Y
	90_LPDP_FCAM	A_DIELECTRIC_3X	=	Y
	90_LPDP_JASPER	A_DIELECTRIC_3X	=	Y
MIPI-D	90_MIPI_DISPLAY	A_DIELECTRIC_3X	=	Y
MIPI-C	90_MIPI_IRCAM	A_DIELECTRIC_2X	=	Y
PCIE (Gen4)	90_PCIE_NAND	A_DIELECTRIC_3X	=	Y
	90_PCIE_BB	A_DIELECTRIC_3X	=	Y
PCIE (Gen2)	90_PCIE_WLAN	A_DIELECTRIC_3X	=	Y
USB	90_KRAKEN_DP	A_DIELECTRIC_3X	=	Y
	90_USB_DP	A_DIELECTRIC_3X	=	Y
	90_EUSB_DP	A_DIELECTRIC_3X	=	Y
MIKEYBUS	90_MIKEYBUS_DP	A_DIELECTRIC_2X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
	CLASS NAME	CLASS NAME	CONSTRAINT SET
LPDP <-> LPDP	90_LPDP_WIDE	90_LPDP_WIDE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_SUPERFLEX_CAM2	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_SINGLEFLEX_CAM	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_SUPERFLEX_CAM2	90_LPDP_SUPERFLEX_CAM2	A_DIELECTRIC_2X
	90_LPDP_SUPERFLEX_CAM2	90_LPDP_SINGLEFLEX_CAM	A_DIELECTRIC_2X
	90_LPDP_SUPERFLEX_CAM2	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_SUPERFLEX_CAM2	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_SINGLEFLEX_CAM	90_LPDP_SINGLEFLEX_CAM	A_DIELECTRIC_2X
	90_LPDP_SINGLEFLEX_CAM	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_SINGLEFLEX_CAM	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_FCAM	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_FCAM	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_JASPER	90_LPDP_JASPER	A_DIELECTRIC_2X
MIPI-D	90_MIPI_DISPLAY	90_MIPI_DISPLAY	A_DIELECTRIC_2X
PCIE (Gen2)	90_PCIE_WLAN	90_PCIE_WLAN	A_DIELECTRIC_2X
USB	90_KRAKEN_DP	90_KRAKEN_DP	A_DIELECTRIC_2X
	90_KRAKEN_DP	90_USB_DP	A_DIELECTRIC_2X
	90_KRAKEN_DP	90_EUSB_DP	A_DIELECTRIC_2X
	90_USB_DP	90_USB_DP	A_DIELECTRIC_2X
	90_USB_DP	90_EUSB_DP	A_DIELECTRIC_2X
	90_EUSB_DP	90_EUSB_DP	A_DIELECTRIC_2X

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Power Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	...	CONSTRAINT SET		
LX/CX Nodes	P	PWR_SHAPE	LX*, !LX_DPMIC*	Y
PWR_SHAPE_LX_GALENA	P	PWR_SHAPE	LX_DPMIC*	Y
PWR_SHAPE_LX	P	PWR_SHAPE	CX*	Y
System-Wide	P	PWR_SHAPE	PP_VDD_MAIN	Y
PWR_SHAPE	P	PWR_SHAPE	PP_VDD_BOOST*	Y
PWR_50UM	P	PWR_50UM	PP3V0_S2	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V8_IO	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V8_S2	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V8_S4	Y
PWR_200UM	P	PWR_200UM	PP1V2_IO	Y
PWR_200UM	P	PWR_200UM	PP1V2_S2	Y
PWR_100UM	P	PWR_100UM	PP1V2_S4	Y
SoC:CPU/GPU	P	PWR_SHAPE	PP_CPU_PCORE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_CPU_ECORE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_GPU	Y
SoC:SRAM/SOC	P	PWR_SHAPE	PP_CPU_SRAM	Y
PWR_SHAPE	P	PWR_SHAPE	PP_SRAM_S1	Y
PWR_SHAPE	P	PWR_SHAPE	PP_SOC_S1	Y
SoC:Fixed	P	PWR_SHAPE	PP0V78_SOC_FIXED_S1	Y
PWR_80UM	P	PWR_80UM	PP0V78_VDD_FIXED_XTAL	Y
PWR_80UM	P	PWR_80UM	PP0V78_SOC_FIXED_PCIE_REFBUF	Y
SoC:VDD12	P	PWR_80UM	PP1V2_S1	Y
PWR_80UM	P	PWR_80UM	PP1V2_S1_XTAL	Y
PWR_200UM	P	PWR_200UM	PP1V2_SOC	Y
PWR_80UM	P	PWR_80UM	PP1V2_SOC_FILT	Y
PWR_80UM	P	PWR_80UM	PP1V2_VDD12_FMON	Y
PWR_80UM	P	PWR_80UM	PP1V2_VDD12_ULPPLL_S2	Y
PWR_80UM	P	PWR_80UM	PP1V2_IO_GRP*	Y
SoC:DDR	P	PWR_SHAPE	PP_DCS_S1	Y
PWR_200UM	P	PWR_200UM	PP0V6_VDDQL_S1	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V06_S2	Y
SoC:Misc.	P	PWR_SHAPE	PP0V7_VDD_LOW_S2	Y
PWR_80UM	P	PWR_80UM	PP0V7_VDD_LOW_*LPPLL	Y
PWR_SHAPE	P	PWR_SHAPE	PP_AVE_S1	Y
PWR_SHAPE	P	PWR_SHAPE	PP_DISP_S1	Y
PWR_200UM	P	PWR_200UM	PP0V6_VDDIO06_GRP1_*	Y
NAND	P	PWR_100UM	PP_NAND_VDDIO1_R	Y
PWR_300UM	P	PWR_300UM	PP_NAND_VDDIO1_F	Y
PWR_SHAPE	P	PWR_SHAPE	PP0V83_NAND	Y
PWR_100UM	P	PWR_100UM	PP0V83_NAND_PLL	Y
PWR_SHAPE	P	PWR_SHAPE	PP2V625_NAND	Y
PMU	P	PWR_SHAPE	PP1V5_VLDOINT	Y
PWR_SHAPE	P	PWR_SHAPE	PP0V9_S1	Y
Yangtze	P	PWR_SHAPE	PP_VBUS1_E75	Y
PWR_SHAPE	P	PWR_SHAPE	PP_VBUS2_DOTARA	Y
PWR_SHAPE	P	PWR_SHAPE	PP_CHARGER_PMID	Y
PWR_SHAPE	P	PWR_SHAPE	PP_BATT_VCC_YANGTZE	Y
PWR_100UM	P	PWR_100UM	CHARGER_BOOT*	Y
PWR_SHAPE	P	PWR_SHAPE	PP6V0_CHARGER_LDO_INTERNAL	Y
PWR_80UM	P	PWR_80UM	PP1V8_ALWAYS	Y
Dotara	P	PWR_SHAPE	PAC_DOTARA_COIL1	Y
PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_AC2	Y
PWR_SHAPE	P	PWR_SHAPE	DOTARA_TX_BANK_2	Y
PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_COIL2	Y
PWR_100UM	P	PWR_100UM	DOTARA_COMM*	Y
PWR_200UM	P	PWR_200UM	DOTARA_CLAMP*	Y
PWR_200UM	P	PWR_200UM	DOTARA_BOOT*	Y
PWR_SHAPE	P	PWR_SHAPE	PP_DOTARA_VMID	Y
PWR_SHAPE	P	PWR_SHAPE	PP_DOTARA_VRECT	Y
PWR_200UM	P	PWR_200UM	PP1V8_DOTARA_LDO	Y
PWR_100UM	P	PWR_100UM	PP5V0_VDD_DOTARA	Y
PWR_100UM	P	PWR_100UM	PP5V0_DOTARA_VMID	Y
PWR_DEFAULT	P	PWR_DEFAULT	PP1V2_DOTARA_S2	Y
Camera PMUs	P	PWR_SHAPE	PP1V3_CAM_PMU*_BUCK0	Y
PWR_100UM	P	PWR_100UM	PP_VDD_MAX_CAM_PMU*	Y
PWR_100UM	P	PWR_100UM	PP_VDD_RTC_CAM_PMU*	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V8_CAM_PMU1_IO_SW	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V8_CAM_PMU2_IO_SW	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V2_INT_CAM_PMU*	Y
Will/Jasper	P	PWR_100UM	PP3V0_WILL_VDD	Y
PWR_100UM	P	PWR_100UM	PP1V8_CAM_PMU2_IO_SW	Y
PWR_100UM_HV	P	PWR_100UM	PN_JASPER_VDDHV*	Y
PWR_100UM	P	PWR_100UM	PP_JASPER_VDDLAS*	Y
Rigel/Pearl	P	PWR_SHAPE	PP_VANA	Y
PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_VINCORE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_BUCK_BOOST_A	Y
PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_BUCK_BOOST_B	Y
PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_CATHODE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_DENSE_ANODE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_SPARSE_ANODE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_A_ANODE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_B_ANODE	Y
PWR_SHAPE	P	PWR_SHAPE	PP_BANE_ANODE	Y
PWR_100UM	P	PWR_100UM	PP3V3_MAMABEAR_VDD	Y
Audio	P	PWR_50UM	PP1V8_AUDIO_VA_S2	Y
Mic Bias	P	PWR_DEFAULT	PP_CODEC_TO_MIC*_BIAS*	Y
PWR_MIC	P	PWR_DEFAULT	RET_CODEC_FROM_MIC*	Y
Codec	P	PWR_200UM	AGND_CODEC	Y
BotSpk	P	PWR_50UM	PP_VA_BOT_SPK_INTERNAL	Y
PWR_SHAPE	P	PWR_SHAPE	PP_SPKRAMP_BOT_VBOOST	Y
PWR_SHAPE	P	PWR_SHAPE	SPKRAMP_BOT_TO_COIL_OUT_*	Y
PWR_80UM	P	PWR_80UM	AGND_BOT_SPK	Y
TopSpk	P	PWR_50UM	PP_VA_TOP_SPK_INTERNAL	Y
PWR_SHAPE	P	PWR_SHAPE	PP_SPKRAMP_TOP_VBOOST	Y
PWR_SHAPE	P	PWR_SHAPE	SPKRAMP_TOP_TO_COIL_OUT_*	Y
PWR_80UM	P	PWR_80UM	AGND_TOP_SPK	Y

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Physical (continued)

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	...	CONSTRAINT SET		
Arc	P	PWR_50UM	PP1V2_ARCAMP_VD_FILT_INTERNAL	Y
PWR_50UM	P	PWR_50UM	PP1V8_ARCAMP_VA_VL_INTERNAL	Y
PWR_SHAPE	P	PWR_SHAPE	PP_ARCAMP_VBOOST	Y
PWR_SHAPE	P	PWR_SHAPE	ARCAMP_TO_SOLENOID_OUT*	Y
PWR_80UM	P	PWR_80UM	AGND_ARCAMP	Y
Touch (DITO)	P	PWR_100UM	PP5V5_TOUCH_BOOST	Y
PWR_100UM	P	PWR_100UM	PP5V1_TOUCH_VDDH*	Y
PWR_80UM	P	PWR_80UM	PP1V8_IO_TOUCH_EEPROM_CONN	Y
Touch (Both)	P	PWR_200UM	PP1V8_TOUCH_S2*	Y
Display PMIC	P	PWR_SHAPE	PP7V3_DISPLAY_AVDDH*	Y
PWR_SHAPE	P	PWR_SHAPE	PP4V6_DISPLAY_VDDEL*	Y
PWR_SHAPE	P	PWR_SHAPE	PNVAR_DISPLAY_VSSEL*	Y
Kraken	P	PWR_SHAPE	PP_ACC_VAR	Y
PWR_80UM	P	PWR_80UM	PP_VAR_USB_RVP	Y
PWR_200UM	P	PWR_200UM	PP_KRAKEN_ACC1*	Y
PWR_SHAPE	P	PWR_SHAPE	PP_KRAKEN_ACC2*	Y
PWR_80UM	P	PWR_80UM	ANALOG_VDD_MAIN_OV_R	Y
Parrot	P	PWR_80UM	PP3V3_USB_S2	Y
AF/OIS (Shared)	P	PWR_SHAPE	PPVAR_RCAM_PVDD	Y
Wide RCAM	P	PWR_100UM	PPVAR_WIDE_PVDD_CONN	Y
PWR_80UM	P	PWR_80UM	PP1V8_WIDE_SINGLEFLEX_CAM_VDDIO*	Y
PWR_100UM	P	PWR_100UM	PP2V85_WIDE_AVDD1*	Y
PWR_200UM	P	PWR_200UM	PPVAR_WIDE_AVDD2	Y
PWR_100UM	P	PWR_100UM	PP1V1_WIDE_DVDD	Y
Superflex-Cam2	P	PWR_100UM	PP2V85_SUPERFLEX_CAM2_AVDD1*	Y
PWR_200UM	P	PWR_200UM	PPVAR_SUPERFLEX_CAM2_AVDD2	Y
PWR_100UM	P	PWR_100UM	PP1V2_SUPERFLEX_CAM2_DVDD	Y
PWR_80UM	P	PWR_80UM	PP1V8_SUPERFLEX_CAM2_VDDIO_CONN	Y
Singleflex-Cam	P	PWR_100UM	PPVAR_SINGLEFLEX_CAM_PVDD_CONN	Y
PWR_80UM	P	PWR_80UM	PP1V8_SINGLEFLEX_CAM_VDDIO_CONN,PP1V8_WIDE_VDDIO_CONN	Y
PWR_100UM	P	PWR_100UM	PP2V85_SINGLEFLEX_CAM_AVDD1	Y
PWR_200UM	P	PWR_200UM	PPVAR_SINGLEFLEX_CAM_AVDD2	Y
PWR_100UM	P	PWR_100UM	PP1V2_SINGLEFLEX_CAM_DVDD	Y
FCAM	P	PWR_80UM	PP1V8_FCAM_IO_CONN	Y
PWR_200UM	P	PWR_200UM	PP2V85_FCAM_AVDD*	Y
PWR_200UM	P	PWR_200UM	PP1V1_FCAM_DVDD	Y
Juliet IRCAM	P	PWR_80UM	PP1V8_IRCAM_VDDIO_CONN	Y
PWR_80UM	P	PWR_80UM	PP2V85_IRCAM_AVDD*	Y
PWR_80UM	P	PWR_80UM	PP1V2_IRCAM_DVDD	Y
Jasper	P	PWR_80UM	PP1V8_JASPER_VDDIO_CONN	Y
PWR_80UM	P	PWR_80UM	PP3V0_JASPER_RX_AVDD*	Y
PWR_80UM	P	PWR_80UM	PP3V3_JASPER_TX_AVDD*	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V1_JASPER_DVDD*	Y
ALS	P	PWR_80UM	PP1V8_ALS_S2	Y
Compass	P	PWR_80UM	PP1V8_COMPASS_S2_CONN	Y
Penrose	P	PWR_80UM	PP3V0_PENROSE_SINGLEFLEX_CAM_SVDD, PP3V0_PENROSE_SVDD_CONN	Y
Dock	P	PWR_80UM	PP1V8_DOCK_S2_CONN	Y
PWR_200UM	P	PWR_200UM	PPVAR_EIGER_S2*	Y
PWR_80UM	P	PWR_80UM	PP1V2_EIGER_S2_CONN	Y
Display	P	PWR_80UM	PP1V2_DISPLAY_S2_CONN	Y
PWR_80UM	P	PWR_80UM	PP1V8_DISPLAY_DVDD_CONN	Y
PWR_SHAPE	P	PWR_SHAPE	PP1VX_DISPLAY_S2*	Y
PWR_80UM	P	PWR_80UM	PP3V0_DISPLAY_S2*	Y
NFC/Ironman NFC	P	PWR_80UM	PP1V2_NFC_S2	Y
PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*_VDDBOOST	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDC	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX, PP_NFC_*_VCASCHI, PP_NFC_*_VCASLO	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDNV	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_TVDD	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDPLL	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_VHV	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_VREF	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_AVDD	Y
PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*_VUP	Y
PWR_100UM	P	PWR_100UM	PP_NFC_*_TXVCASC*	Y
PWR_NFC_ANT	P	PWR_NFC_ANT	NFC_*_ANT_POS, NFC_*_ANT_NEG, NFC_*_ANT_MATCH_*	Y
PWR_NFC_ANT	P	PWR_NFC_ANT	NFC_*_TXP, NFC_*_TXN, NFC_*_BAL*, NFC_*_PROBE_*	Y
PWR_80UM	P	PWR_80UM	PP_SIMVCC1	Y
Arrow	P	PWR_SHAPE	PP1V0_S4	Y
PWR_SHAPE	P	PWR_SHAPE	PP1V0_R1_ANA_S4	Y
QETs/APTs	P	PWR_300UM	PP_QET*	Y
PWR_SHAPE	P	PWR_SHAPE	PP_APT*	Y
Misc. Radio	P	PWR_100UM	PP_VDD_RF_1V2	Y
PWR_100UM	P	PWR_100UM	PP_LDO6_VIO_1V8*	Y
PWR_100UM	P	PWR_100UM	PP_RFFE1_VIO_XCVR_1V8_R	Y
PWR_100UM	P	PWR_100UM	UAT_SUBUS_*, UAT_SAWTOOTH_*	Y
GND	P	DEFAULT	GND	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	...	CONSTRAINT SET		
GND	S	MSAP_YIELD	GND	Y
PWR_DEFAULT	S	DEFAULT	=	Y
PWR_50UM	S	DEFAULT	=	Y
PWR_80UM	S	DEFAULT	=	Y
PWR_100UM	S	DEFAULT	=	Y
PWR_200UM	S	DEFAULT	=	Y
PWR_300UM	S	DEFAULT	=	Y
PWR_SHAPE	S	DEFAULT	=	Y
PWR_100UM_HV	S	HV_SPACING	=	Y
PWR_MIC	S	DEFAULT	=	Y
PWR_NFC_ANT	S	DEFAULT	=	Y
PWR_SHAPE_LX	S	LX_SPACING	=	Y
PWR_SHAPE_LX_GALENA	S	LX_SPACING	=	Y

Class-Class on next page

PAGE TITLE: CONSTRAINTS: Power

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Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
E_DP_GENERIC	E	GENERIC_DP	DP:DP_CODEC_AOUT*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_MIC*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_PENROSE*	Y
E_DP_NTC	E	DIFF_PAIR_NTC	DP:DP_NTC_*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_*MTR*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_ANALOG*SENSE*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_ANALOG_VIN_SAKONNET_FROM_HALL	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_PMU_VDD_MAIN_SENSE*	Y
E_DP_NC	E	GENERIC_DP	DP:DP_NC*	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
DP_PWR	P	PWR_DP	DP:DP_CODEC_AOUT*	Y
DP_MIC	P	GENERIC_DP	DP:DP_*MIC*	Y
DP_PENROSE	P	GENERIC_DP	DP:DP_PENROSE*	Y
DP_NTC	P	GENERIC_DP	DP:DP_NTC_*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_*MTR*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_ANALOG*SENSE*	Y
DP_SAKONNET	P	GENERIC_DP	DP:DP_ANALOG_VIN_SAKONNET_FROM_HALL	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_PMU_VDD_MAIN_SENSE*	Y
DP_NC	P	GENERIC_DP	DP:DP_NC*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
DP_PWR	S	DEFAULT	=	Y
DP_MIC	S	A_DIELECTRIC_1.5X	=	Y
DP_PENROSE	S	A_DIELECTRIC_1.5X	=	Y
DP_NTC	S	A_DIELECTRIC_1.5X	=	Y
DP_GENERIC	S	DEFAULT	=	Y
DP_SAKONNET	S	DEFAULT	=	Y
DP_NC	S	DEFAULT	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
DP_MIC	GND	DEFAULT
DP_MIC	PWR_MIC	DEFAULT
DP_MIC	DP_SAKONNET	DEFAULT

Sensitive Analog

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
ANALOG_SAKONNET_BIAS	P	DEFAULT	ANALOG_BIAS_SAKONNET*, ANALOG_RET_SAKONNET*	Y
ANALOG	P	DEFAULT	ANALOG*DOTARA*	Y
ANALOG	P	DEFAULT	ANALOG*DOMBRA*	Y
ANALOG	P	DEFAULT	ANALOG*SENSE,ANALOG*SENSE_SE,ANALOG*SENSE_FILT	Y
ANALOG	P	DEFAULT	ANALOG_DDR*ZQ*	Y
ANALOG_NAND_ZQ	P	PWR_100UM	ANALOG_NAND*ZQ*	Y
ANALOG	P	DEFAULT	ANALOG*REXT*	Y
ANALOG	P	DEFAULT	ANALOG*CAL*	Y
ANALOG	P	DEFAULT	ANALOG_*REF*	Y
ANALOG	P	DEFAULT	ANALOG_FB*	Y
ANALOG	P	DEFAULT	ANALOG_KRAKEN_BYPASS,ANALOG_KRAKEN_BI_CCG2B_CC	Y
ANALOG	P	DEFAULT	ANALOG_RIGEL_LSCP	Y
ANALOG_AMP_FILT	P	PWR_80UM	ANALOG_*_SPK_FILT,ANALOG_ARCAMP_FILT	Y
ANALOG_VSS_PMU_XTAL	P	DEFAULT	VSS_PMU_XTAL	Y
ANALOG_AMUX	P	DEFAULT	AMUX*	Y
ANALOG_NTC	P	DEFAULT	NTC_NFC_UAT*_POS	Y
ANALOG_NTC	P	DEFAULT	NTC_PEARL_VCSEL_TO_RIGEL	Y
ANALOG_NTC	P	DEFAULT	NTC_STROBE_MODULE*	Y
ANALOG_SPKR_SENSE	P	DEFAULT	COIL_TO_SPKRAMP_*_VSENSE_*, SOLENOID_TO_ARC_VSENSE_*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
ANALOG	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_SAKONNET_BIAS	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_AMP_FILT	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_VSS_PMU_XTAL	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_AMUX	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_NTC	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_SPKR_SENSE	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_NAND_ZQ	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
ANALOG	GND	DEFAULT
ANALOG_SAKONNET_BIAS	GND	DEFAULT
ANALOG_AMP_FILT	GND	DEFAULT
ANALOG_VSS_PMU_XTAL	GND	DEFAULT
ANALOG_AMUX	GND	DEFAULT
ANALOG_NTC	GND	DEFAULT
ANALOG_SPKR_SENSE	GND	DEFAULT
ANALOG_SAKONNET_BIAS	ANALOG_SAKONNET_BIAS	DEFAULT
ANALOG_SAKONNET_BIAS	DP_SAKONNET	DEFAULT
ANALOG_NAND_ZQ	GND	DEFAULT

Clocks

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
CLK	P	DEFAULT	CLK_*	Y
CLK_SPMI	P	DEFAULT	SPMI*CLK*	Y
CLK_I2S	P	DEFAULT	I2S*MCLK*, I2S*BCLK*	Y
CLK_SPI	P	DEFAULT	SPI*SCLK*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
CLK	S	A_DIELECTRIC_1.5X	=	Y
CLK_SPMI	S	A_DIELECTRIC_1.5X	=	Y
CLK_I2S	S	A_DIELECTRIC_1.5X	=	Y
CLK_SPI	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CLK	GND	DEFAULT
CLK_SPMI	GND	DEFAULT
CLK_I2S	GND	DEFAULT
CLK_SPI	GND	DEFAULT

Grouping Constraints

Physical

Used to clean up CM

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
GRP_GPIO	P	DEFAULT	GPIO*, IO_*	Y
GRP_NC	P	DEFAULT	NC_*	Y
GRP_I2C	P	DEFAULT	I2C*	Y
GRP_I2S	P	DEFAULT	I2S*LRCLK*, I2S*DOUT*, I2S*DIN*	Y
GRP_SPI	P	DEFAULT	SPI*MOSI*, SPI*MISO*, SPI*CS*	Y
GRP_UART	P	DEFAULT	UART*	Y
GRP_SWD	P	DEFAULT	SWD*	Y
GRP_SPMI_DATA	P	DEFAULT	SPMI*DATA*	Y
GRP_PCIE_SIDE	P	DEFAULT	PCIE*CLKREQ*, PCIE*PERST*	Y
GRP_LPDP_AUX	P	DEFAULT	LPDP*AUX*	Y
GRP_CODEC_FILT	P	PWR_200UM	CODEC_*FILTP, CODEC_*FILTN	Y
RFFE	P	DEFAULT	SHIELD_RFFE*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***_***	CONSTRAINT SET		
GRP_GPIO	S	DEFAULT	=	Y
GRP_NC	S	DEFAULT	=	Y
GRP_I2C	S	DEFAULT	=	Y
GRP_I2S	S	DEFAULT	=	Y
GRP_SPI	S	DEFAULT	=	Y
GRP_UART	S	DEFAULT	=	Y
GRP_SWD	S	DEFAULT	=	Y
GRP_SPMI_DATA	S	DEFAULT	=	Y
GRP_PCIE_SIDE	S	DEFAULT	=	Y
GRP_LPDP_AUX	S	DEFAULT	=	Y
GRP_CODEC_FILT	S	DEFAULT	=	Y
RFFE	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
RFFE	50_TX0_THIN	A_DIELECTRIC_3X
RFFE	50_TX1_THIN	A_DIELECTRIC_3X
RFFE	50_TX2_THIN	A_DIELECTRIC_3X
RFFE	50_RX_THIN	A_DIELECTRIC_3X
RFFE	RFFE	DEFAULT
RFFE	GND	DEFAULT

Power (cont'd from prev. page)

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_100UM	GND	MSAP_YIELD_PWR
PWR_100UM	PWR_100UM	100UM-249UM_SPACING
PWR_100UM	PWR_200UM	100UM-249UM_SPACING
PWR_100UM	PWR_300UM	100UM-249UM_SPACING
PWR_100UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_200UM	GND	MSAP_YIELD_PWR
PWR_200UM	PWR_200UM	100UM-249UM_SPACING
PWR_200UM	PWR_300UM	100UM-249UM_SPACING
PWR_200UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_300UM	GND	MSAP_YIELD_PWR
PWR_300UM	PWR_300UM	250UM+_SPACING
PWR_300UM	PWR_SHAPE	250UM+_SPACING
PWR_SHAPE	GND	MSAP_YIELD_PWR
PWR_SHAPE	PWR_SHAPE	250UM+_SPACING
PWR_SHAPE_LX	GND	DEFAULT
PWR_SHAPE_LX	PWR_SHAPE_LX	DEFAULT
PWR_SHAPE_LX	ANALOG	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_SAKONNET_BIAS	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_AMP_FILT	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_VSS_PMU_XTAL	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_NTC	A_DIELECTRIC_3X

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_SHAPE_LX	ANALOG_AMUX	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_SPKR_SENSE	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK_SPMI	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK_I2S	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK_SPI	A_DIELECTRIC_3X
PWR_SHAPE_LX_GALENA	GND	A_DIELECTRIC_3X
PWR_100UM_HV	GND	DEFAULT

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Hybrid RF CSets

50-Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= 2			
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
ISL3	ISL2,ISL4	50	
ISL6	ISL7,ISL5	50	
ISL8	ISL9,ISL7	50	
ISL9	BOTTOM,ISL8	50	
BOTTOM	ISL9	50	

50-Wide

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= 2			
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
ISL3	TOP,ISL5	50	
ISL6	ISL8,ISL4	50	
ISL7	ISL9,ISL5	50	
BOTTOM	ISL8	50	

50-Wide w/ Thin on L1/L10

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= 2			
RULE NAME= 50_WIDE_SURFACE_THIN		ZONE NAME= PRIMARY	
ISL3	TOP,ISL5	50	
ISL6	ISL8,ISL4	50	
ISL7	ISL9,ISL5	50	
BOTTOM	ISL9	50	

50-ohm (Thin) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	50_TX0_THIN	P	A_50_THIN_SE	50_TX_IN_*TX0_*	Y
	50_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_*TX1_*	Y
	50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_*TX2_*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT_M	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_UHB_L_CPLR_OUT	Y
WiFi	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_WLAN_A_C0*	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_UAT*	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_WLAN_G_C0*	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_G_UAT_TXRX_FEM	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_WLAN_G_C1*	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_G_LAT_TXRX_FEM	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_LB_PORTB_RX1, 50_TRX_LB_PORTB_TX_ANT2	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_PAUHBL_N79_ANT1_TO_ANT7	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_ANT4_MB_HB_WLAN24	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_UWB_ANT2_6G_FL_OUT	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_UWB_ANT2_6G_T_MATCHING	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Everything	50_TX_IN_THIN	S	NA_DIELECTRIC_2XDS_50_THIN_SE	=	Y
	50_TX0_THIN	S	NA_DIELECTRIC_2XDS_50_THIN_SE	=	Y
	50_TX1_THIN	S	NA_DIELECTRIC_2XDS_50_THIN_SE	=	Y
	50_TX2_THIN	S	NA_DIELECTRIC_2XDS_50_THIN_SE	=	Y
	50_RX_THIN	S	NA_DIELECTRIC_2XDS_50_THIN_SE	=	Y
	50_TRX_THIN	S	NA_DIELECTRIC_2XDS_50_THIN_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
CLASS NAME	CLASS NAME	CONSTRAINT SET	
Same Class	50_TX0_THIN	50_TX0_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	50_TX1_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	50_TX2_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	50_RX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TRX_THIN	50_TRX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
GND	50_TX0_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TRX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
Thin-Thin	50_TX0_THIN	50_TX1_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX0_THIN	50_TX2_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX0_THIN	50_RX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX0_THIN	50_TRX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX1_THIN	50_TX2_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX1_THIN	50_RX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX1_THIN	50_TRX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX2_THIN	50_RX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX2_THIN	50_TRX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_RX_THIN	50_TRX_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
Thin-Wide	50_TX0_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX1_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX2_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_THIN_SE
	50_RX_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TRX_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX0_THIN	50_TRX_WIDE_SURFACE_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX1_THIN	50_TRX_WIDE_SURFACE_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TX2_THIN	50_TRX_WIDE_SURFACE_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_RX_THIN	50_TRX_WIDE_SURFACE_THIN	NA_DIELECTRIC_4XD_50_THIN_SE
	50_TRX_THIN	50_TRX_WIDE_SURFACE_THIN	NA_DIELECTRIC_4XD_50_THIN_SE

50-ohm (Wide) Constraints

Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT2_LB_LMB_MB_HB_L1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4_MB_HB_WLAN24_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT7_UHB_N79	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT7_UHB_N79_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT8*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_CPLR_U_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PAD_*	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_LB_PORTB_TX_M	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_LB_PORTB_RX1_M	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBL_UHB_ANT1_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_UHB_ANT2_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT2_TO_ANT9	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBU_N79_*	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBU_UHB_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_UHB_PAD_PORTB_*	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_UHB_PAD_N79_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_LMB_ANT	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_IN_LMB_PAD_LMB_ANT_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_MB_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	Y
WiFi	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_WLAN_G_BT_ANT3_NPLXR	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_G_BT_LAT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_WLAN_G_BT_ANT4*	Y
Arrow	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_R1_AOA2, 50_TRX_R1_AOA3	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_R1_ANT2_CH5	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_R1_AOA1, 50_TRX_R1_ANT2_CH9	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_R1_ANT*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT0	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT2_6G	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT2_6G_FL_IN	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT2_8G	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT2_8G_FL_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT3	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_R1_WLAN_A_LAA_ANT6	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_R1_WLAN_A_LAA_DPLXR*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_R1_WLAN_A_LAA_M	Y
	50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBL_N79_ANT1_TO_ANT7_M	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE	S	NA_DIELECTRIC_2XDS_50_WIDE_SE	=	Y
50_TRX_WIDE_SURFACE_THIN	S	NA_DIELECTRIC_2XDS_50_WIDE_SURFACE_THIN_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
	CLASS NAME	CLASS NAME	CONSTRAINT SET
GND	50_TRX_WIDE	GND	NA_DIELECTRIC_2X_50_WIDE_SE
	50_TRX_WIDE_SURFACE_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_THIN_SE
Wide-Wide	50_TRX_WIDE	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_WIDE_SE
	50_TRX_WIDE_SURFACE_THIN	50_TRX_WIDE	NA_DIELECTRIC_4XD_50_WIDE_SURFACE_THIN_SE
	50_TRX_WIDE_SURFACE_THIN	50_TRX_WIDE_SURFACE_THIN	NA_DIELECTRIC_4XD_50_WIDE_SURFACE_THIN_SE

Pin Delay Check

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
U1000	SicilyPinDelay.csv
J10800	D53-JulietPinDelay.csv

*Location: /physical/rule/pindelays

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PAGE TITLE: CONSTRAINTS: Stackup/Misc. (FF-Specific)

DRAWING NUMBER: 051-05215 | SIZE: D

REVISION: 4.6.0

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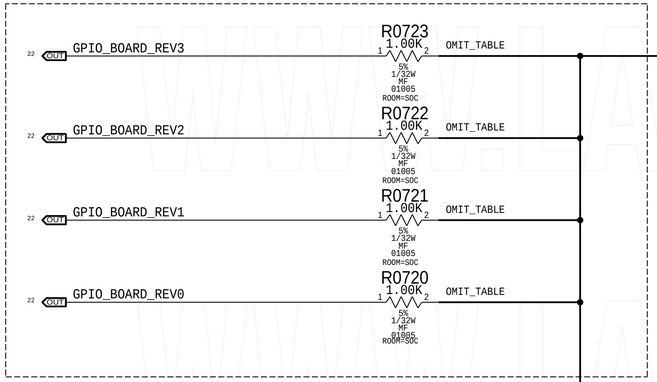
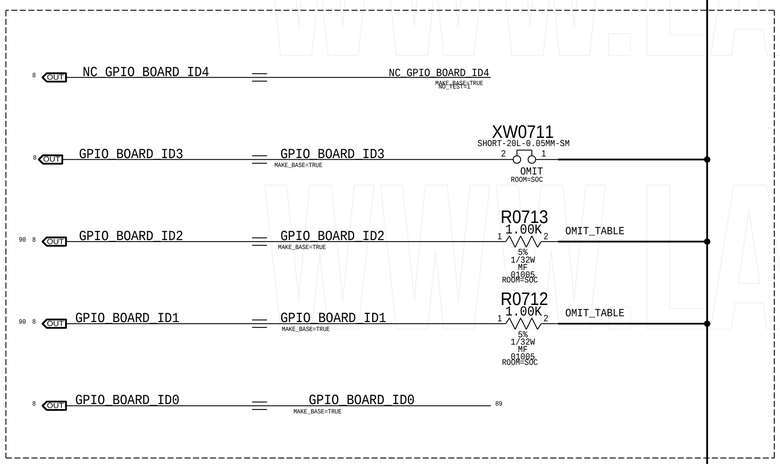
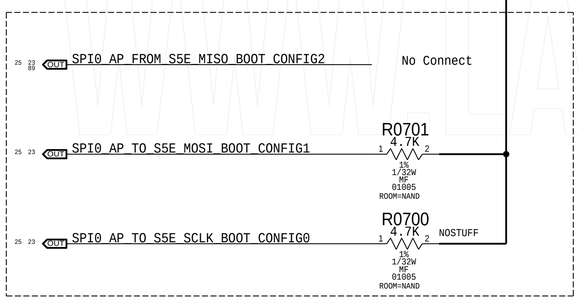
BOOTSTRAPPING

BOARD REV + BOARD ID + BOOT CONFIG







Board Rev [3:0]

* Float = 0 | PU = 1

Note: iBoot uses the inverse of BOARD_REV[3:0], so that it counts up (Pre-Proto = 0x0, PVT = 0xF)

	BOARD_REV[3:0]	[3]	[2]	[1]	[0]
Pre-Proto	4'b1111	1	1	1	1
Proto 1	4'b1110	1	1	1	0
Proto 1.5	4'b1101	1	1	0	1
Proto 2	4'b1100	1	1	0	0
Proto 2.5	4'b1011	1	0	1	1
Pre-EVT	4'b1010	1	0	1	0
EVT	4'b1001	1	0	0	1
Carrier	4'b1000	1	0	0	0

(Allocate more as necessary in descending order)

DVT	4'b0001	0	0	0	1
PVT	4'b0000	0	0	0	0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0721,R0720	BOARD_REV:PROTO0	PROTO0
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0721	BOARD_REV:PROTO1	PROTO1
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0720	BOARD_REV:PROTO1.5	PROTO1.5
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722	BOARD_REV:PROTO2	PROTO2
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0721,R0720	BOARD_REV:PROTO2.5	PROTO2.5
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0721	BOARD_REV:PRE-EVT	PRE-EVT
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0720	BOARD_REV:EVT	EVT
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723	BOARD_REV:CRB	CRB
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0720	BOARD_REV:DVT	DVT

(PVT NOSTUFF ALL)

Board ID [4:0]

* Float = 0 | PU = 1

	BOARD_ID[4:0]	[4] Unused	[3] 1=MAV20	[2]	[1]	[0] 0=MLB, 1=DEV
MLB D52G	5'b01010	0	1	0	1	0
DEV D52G	5'b01011	0	1	0	1	1
MLB D53G	5'b01100	0	1	1	0	0
DEV D53G	5'b01101	0	1	1	0	1
MLB D53P	5'b01110	0	1	1	1	0
DEV D53P	5'b01111	0	1	1	1	1
MLB D54P	5'b01000	0	1	0	0	0
DEV D54P	5'b01001	0	1	0	0	1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0712	BOARD_ID:D52	D52 = 01
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0713	BOARD_ID:D53G	D53G = 10
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0713,R0712	BOARD_ID:D53P	D53P = 11
(D54 both NOSTUFF)					D54 = 00

Boot Config [2:0]

* Float = 0 | PU = 1

	USAGE	SPEED	TEST	[2]	[1]	[0]	
SPI1 NOR	--	12MHz	--	0	0	0	
SPI1 NOR	--	12MHz	Test	0	0	1	
SPI0 NAND	POR	12MHz	--	0	1	0	<-- POR
SPI0 NAND	Proto	12MHz	Test	0	1	1	<-- Proto Builds
SPI1 NOR	--	24MHz	--	1	0	0	
SPI1 NOR	--	24MHz	Test	1	0	1	
SPI1 NOR	--	6MHz	--	1	1	0	
SPI1 NOR	--	6MHz	Test	1	1	1	

<--- Remove at EVT

PAGE TITLE

SYSTEM: Bootstrapping

DRAWING NUMBER 051-05215 | SIZE D

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SOC

4GB DRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-19672	1	Sicily,A0,4GB,M	U1000	CRITICAL	BOARD_ID:0528B0ARD_ID:0536

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-19673	998-19672	BOARD_ID:0528B0ARD_ID:0536	U1000	Sicily,A0,4GB,H
998-19674	998-19672	BOARD_ID:0528B0ARD_ID:0536	U1000	Sicily,A0,4GB,S

6GB DRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-19675	1	Sicily,A0,6GB,M	U1000	CRITICAL	BOARD_ID:053FB0ARD_ID:054

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-19676	998-19675	BOARD_ID:053FB0ARD_ID:054	U1000	Sicily,A0,6GB,H
998-19677	998-19675	BOARD_ID:053FB0ARD_ID:054	U1000	Sicily,A0,6GB,S

24M XTAL Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0612	197S00118	?	Y1000	XTAL, 24M, 1612
197S00120	197S00118	?	Y1000	XTAL, 24M, 1612

SOC: Misc

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 1 OF 21
OMIT_TABLE

BOARD ID
- BOARD_ID0
- BOARD_ID1
- BOARD_ID2
- BOARD_ID3
- BOARD_ID4

DFU
- REQUEST_DFU1
- REQUEST_DFU2
- FORCE_DFU
- DFU_STATUS

FPWM
- FPWM0
- FPWM1
- FPWM2

MTR
- PAD_MTR_ANALOG_TEST_P
- PAD_MTR_ANALOG_TEST_N
- PAD_MTR_VREF_P
- PAD_MTR_VREF_N

THROTTLERS
- THROTTLE_TRIGGER0 — BJ61 — NC_DEV_SOC_THROTTLE_TRIGGER0
- THROTTLE_TRIGGER1 — BJ60 — IO_AP_FROM_PMU_SW_SHDN_L
- THROTTLE_TRIGGER2 — BG62 — IO_AP_FROM_PMU_PRE_UVLO_L
- THROTTLE_TRIGGER3 — BG61 — NC_DEV_SOC_THROTTLE_TRIGGER3
- THROTTLE_TRIGGER4 — BE62 — NC_DEV_SOC_THROTTLE_TRIGGER4

THROTTLE_TRIGGER[0:4]:
These need an internal pull-up enabled on SoC

MISC
- SOCHOT1 — BE61 — IO_SOC_TO_PMU_SOCHOT_RESET_L
- SWD_TCK_OUT1 — CP15 — SWD_AP_TO_MANY_SWCLK
- SWD_TMS2 — CN15 — SWD_AP_BI_NAND_SWDIO
- SWD_TMS3 — CP13 — SWD_AP_BI_BB_SWDIO
- SWD_TMS4 — CK62 — SWD_AP_BI_R1_SWDIO
- TST_CLKOUT — BE60 — CLK_AP_TO_PMU_TST_CLKOUT
- ANALOGMUX_OUT — CN3 — AMUX_SOC_TO_PMU_AMUX_OUT
- CFSB — CL7 — IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY
- CFSB_XTAL — F5 — IO_AON_TO_AP_XTAL_CFSB
- HOLD_RESET — AG60 — GND
- TESTMODE — AF62 — GND

Clocked by SWD_TCK_OUT1

PP0V6_VDDQL_S1

R1010 / R1011 / R1012 / R1013 / R1014 / R1015: 240 1% 1/32W MF 01005 ROOM=SOC

DDR
- DDR0_RREF — CJ3 — ANALOG_DDR0_RREF
- DDR0_ZQ — BM2 — ANALOG_DDR0_ZQ
- DDR1_RREF — BV60 — ANALOG_DDR1_RREF
- DDR2_RREF — K3 — ANALOG_DDR2_RREF
- DDR3_RREF — Y61 — ANALOG_DDR3_RREF
- DDR3_ZQ — AB62 — ANALOG_DDR3_ZQ
- LP4_IN_RESET* — V60 — IO_PMU_TO_SYSTEM_RESET_L

XTAL
- XI0 — E9 — CLK_AP_XTAL_24M_IN
- XO0 — D9 — CLK_AP_XTAL_24M_OUT

R1021 499 1% 1/32W MF 01005 ROOM=SOC_XTAL

CLK_AP_XTAL_24M_OUT_R

197S00118 CRITICAL ROOM=SOC_XTAL
Y1000 1.60X1.20MM-SM 24MHZ-30PPM-9.5PF-60OHM

C1020 12PF 5% 16V NP0-C0G 01005-1 ROOM=SOC_XTAL
C1021 12PF 5% 16V NP0-C0G 01005-1 ROOM=SOC_XTAL

SOC_XTAL_GND

XW1000 SHORT-20L-0.05MM-SM OMIT NO_XNET_CONNECTION ROOM=SOC_XTAL

REQUEST_DFUx: Legacy button detection
MLB: Hard tie to PP1V2_IO
DEV: Wire to PMU BUTTONO

PP (dev board only)
- GPIO_BOARD_ID0 — CN11
- GPIO_BOARD_ID1 — CM15
- GPIO_BOARD_ID2 — CP9
- GPIO_BOARD_ID3 — CJ62
- NC_GPIO_BOARD_ID4 — CP11

PP1V2_IO — BK61
PP1V2_IO — BJ62

- IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU — AN60
- IO_SOC_DFU_STATUS — BK62

PP (dev board only)
- NC_DEV_AP_TMR32_PWM0 — AG3
- NC_DEV_AP_TMR32_PWM1 — AG2
- NC_DEV_AP_TMR32_PWM2 — AJ3

- TEST_PAD_MTR_ANALOG_P — CB60
- TEST_PAD_MTR_ANALOG_N — CB61

PP (dev board only)
- NC_DEV_PAD_MTR_VREF_P — CD60
- NC_DEV_PAD_MTR_VREF_N — CD61

SOC: NAND + USB

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 2 OF 21
OMIT_TABLE

NAND - IOS
- NAND_SYS_CLK — AR2
- SSD_RESET* — AJ62
- SSD_BFH — AL60

USB
- USB_EDP — A28 — 90_EUSB_PARROT_BI_AP_P
- USB_EDM — B28 — 90_EUSB_PARROT_BI_AP_N
- USB_RESREF — D28 — ANALOG_SOC_USB_RESREF
- EUSB_VBUS_DETECT — AG61 — PP1V2_IO

R1001 33.2 1% 1/32W MF 01005 ROOM=SOC

CLK_AP_TO_NAND_24M → CLK_AP_TO_NAND_24M_R
- IO_AP_TO_NAND_RESET_L
- IO_AP_TO_NAND_FW_STRAP

R1002 200 1% 1/32W MF 01005 ROOM=SOC

SYNCING: D52, D53, D54

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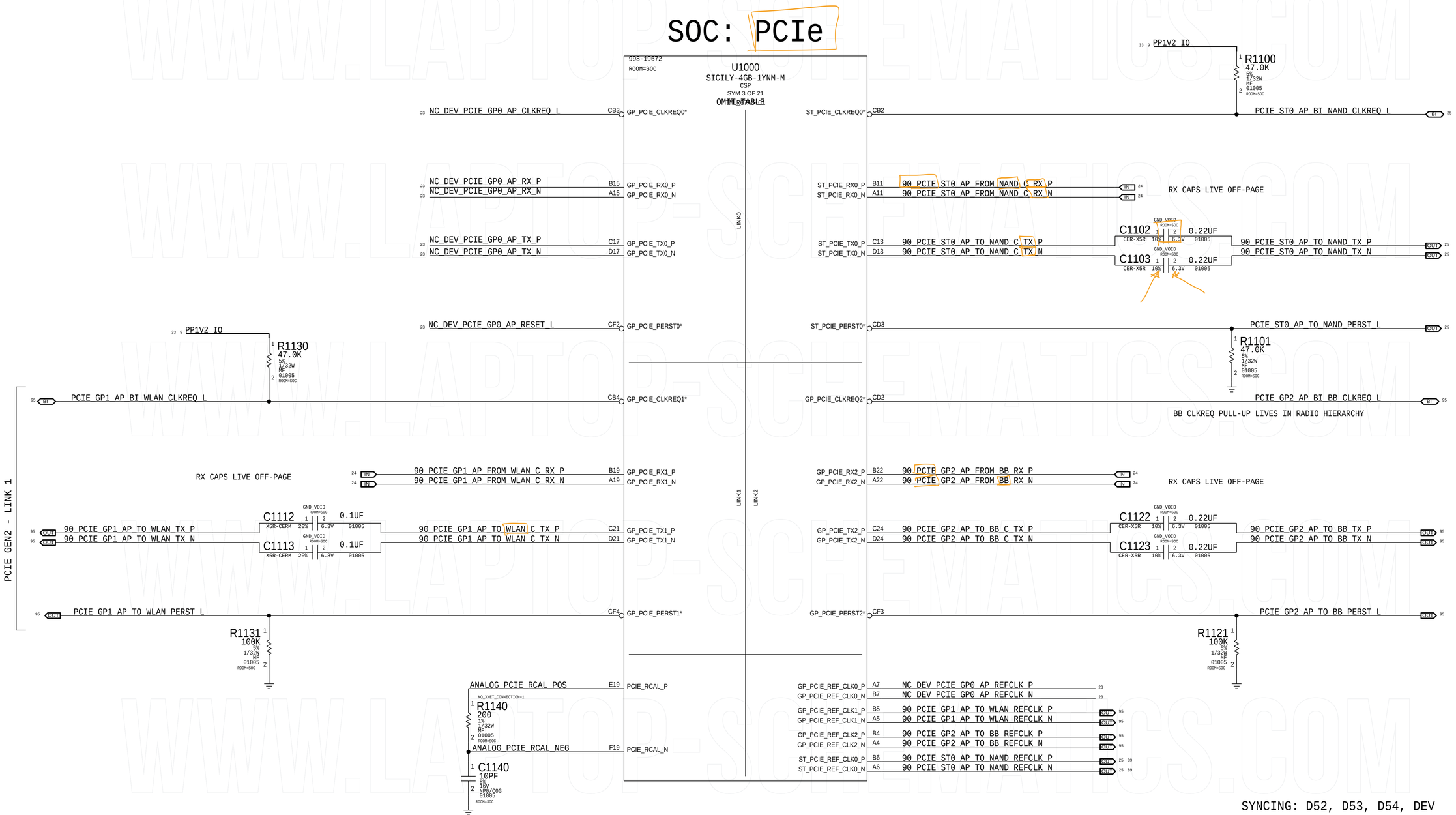
SOC: PCIe



SYNCING: D52, D53, D54, DEV

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DO NOT SWIZZLE LPDP LANES UNLESS ROUTING NECESSITATES IT
LPDP Swizzle Options:
-P/N can be switched
-Non-sequential lanes can be grouped
(e.g. FCAM 0 -> SOC 5, FCAM 1 -> SOC 2)
-AUX pin (one per device) doesn't have to match lane numbers

SOC: ISP

Note: LPDP RX and AUX lanes need a series 0.1uF cap

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 4 OF 21
OMIT_TABLE TMLR67A0-C1

90_LPDP_ISP_FROM_FCAM_RX_D1_N	CP19	LPDPRX_RX_D0_P	MIPI-C
90_LPDP_ISP_FROM_FCAM_RX_D1_P	CN19	LPDPRX_RX_D0_N	
90_LPDP_ISP_FROM_FCAM_RX_D0_N	CN21	LPDPRX_RX_D1_P	
90_LPDP_ISP_FROM_FCAM_RX_D0_P	CM21	LPDPRX_RX_D1_N	
90_LPDP_ISP_FROM_WIDE_RX_D2_P	CP22	LPDPRX_RX_D2_P	
90_LPDP_ISP_FROM_WIDE_RX_D2_N	CN22	LPDPRX_RX_D2_N	
90_LPDP_ISP_FROM_WIDE_RX_D1_N	CP26	LPDPRX_RX_D3_P	
90_LPDP_ISP_FROM_WIDE_RX_D1_P	CN26	LPDPRX_RX_D3_N	
90_LPDP_ISP_FROM_WIDE_RX_D0_N	CN28	LPDPRX_RX_D4_P	
90_LPDP_ISP_FROM_WIDE_RX_D0_P	CM28	LPDPRX_RX_D4_N	
90_LPDP_ISP_FROM_SUPERFLEX_CAM2_RX_D2_N	CP30	LPDPRX_RX_D5_P	
90_LPDP_ISP_FROM_SUPERFLEX_CAM2_RX_D2_P	CN30	LPDPRX_RX_D5_N	
90_LPDP_ISP_FROM_SUPERFLEX_CAM2_RX_D0_P	CN32	LPDPRX_RX_D6_P	
90_LPDP_ISP_FROM_SUPERFLEX_CAM2_RX_D0_N	CM32	LPDPRX_RX_D6_N	
90_LPDP_ISP_FROM_SUPERFLEX_CAM2_RX_D1_N	CP34	LPDPRX_RX_D7_P	
90_LPDP_ISP_FROM_SUPERFLEX_CAM2_RX_D1_P	CN34	LPDPRX_RX_D7_N	
90_LPDP_ISP_FROM_JASPER_RX_D0_P	CN36	LPDPRX_RX_D8_P	
90_LPDP_ISP_FROM_JASPER_RX_D0_N	CM36	LPDPRX_RX_D8_N	
90_LPDP_ISP_FROM_SINGLEFLEX_CAM_RX_D0_P	CN40	LPDPRX_RX_D9_P	
90_LPDP_ISP_FROM_SINGLEFLEX_CAM_RX_D0_N	CM40	LPDPRX_RX_D9_N	
90_LPDP_ISP_FROM_SINGLEFLEX_CAM_RX_D1_P	CP42	LPDPRX_RX_D10_P	
90_LPDP_ISP_FROM_SINGLEFLEX_CAM_RX_D1_N	CN42	LPDPRX_RX_D10_N	
90_LPDP_ISP_FROM_SINGLEFLEX_CAM_RX_D2_P	CN43	LPDPRX_RX_D11_P	
90_LPDP_ISP_FROM_SINGLEFLEX_CAM_RX_D2_N	CM43	LPDPRX_RX_D11_N	
ANALOG_LPDP_ISP_RX0_RCAL_POS	CM24	LPDPRX0_RCAL_P	
	CN24	LPDPRX0_RCAL_N	
	CN38	LPDPRX1_RCAL_P	
ANALOG_LPDP_ISP_RX0_RCAL_NEG	CP38	LPDPRX1_RCAL_N	

R1200 200 1% 1/32W MF 01005 ROOM=SOC
C1200 10PF 5% 16V NP0/C0G 01005 ROOM=SOC

ANALOG_LPDP_ISP_RX1_RCAL_POS
ANALOG_LPDP_ISP_RX1_RCAL_NEG

R1210 200 1% 1/32W MF 01005 ROOM=SOC
C1210 10PF 5% 16V NP0/C0G 01005 ROOM=SOC

NC_LPDP_ISP_AUX_RX_D0P	CL22	LPDPRX_AUX_D0_P	LPDP-RX
NC_LPDP_ISP_AUX_RX_D1P	CK24	LPDPRX_AUX_D1_P	
LPDP_ISP_BI_SUPERFLEX_CAM2_AUX_RX_D2P	CL26	LPDPRX_AUX_D2_P	
NC_LPDP_ISP_AUX_RX_D3P	CK28	LPDPRX_AUX_D3_P	
NC_LPDP_ISP_AUX_RX_D4P	CL30	LPDPRX_AUX_D4_P	
LPDP_ISP_BI_SINGLEFLEX_CAM_AUX_RX_D5P	CK32	LPDPRX_AUX_D5_P	
NC_LPDP_ISP_AUX_RX_D6P	CL34	LPDPRX_AUX_D6_P	
NC_LPDP_ISP_AUX_RX_D7P	CK36	LPDPRX_AUX_D7_P	
NC_LPDP_ISP_AUX_RX_D8P	CL38	LPDPRX_AUX_D8_P	
NC_LPDP_ISP_AUX_RX_D9P	CK40	LPDPRX_AUX_D9_P	
NC_LPDP_ISP_AUX_RX_D10P	CL42	LPDPRX_AUX_D10_P	
NC_LPDP_ISP_AUX_RX_D11P	CK43	LPDPRX_AUX_D11_P	

MIPI0C_DPCLK	CP60	90_MIPI_ISP_FROM_IRCAM_CLK_P	MIPI-C
MIPI0C_DNCLK	CN60	90_MIPI_ISP_FROM_IRCAM_CLK_N	
MIPI0C_DPDATA0	CN58	90_MIPI_ISP_FROM_IRCAM_D0_P	
MIPI0C_DNDATA0	CP58	90_MIPI_ISP_FROM_IRCAM_D0_N	
MIPI0C_DPDATA1	CN59	90_MIPI_ISP_FROM_IRCAM_D1_P	
MIPI0C_DNDATA1	CP59	90_MIPI_ISP_FROM_IRCAM_D1_N	
MIPI0C_REXT	CL55	ANALOG_MIPI_ISP_REXT	
ISP_I2C0_SCL	CL58	NC_I2C0_ISP_SCL	I2C
ISP_I2C0_SDA	CL57	NC_I2C0_ISP_SDA	
ISP_I2C1_SCL	CM6	NC_I2C1_ISP_SCL	
ISP_I2C1_SDA	CM4	NC_I2C1_ISP_SDA	

PP (dev board only)
R1250 200 1% 1/32W MF 01005 ROOM=SOC

ISP_GPIO_0	CK59	GPIO_ISP_TO_CAM_PMU1_CAM_PMU2_RESET_L	GPIO
ISP_GPIO_1	CM7	NC_ISP_GPIO_1	
ISP_GPIO_2	CL59	NC_ISP_GPIO_2	
ISP_GPIO_3	CN5	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	

External flash trigger:
Kraken sends signal to Lightning accessory

SENSOR0_CLK	AL2	CLK_ISP_TO_CAM_PMU1_24M_R	SENSOR CLK
SENSOR1_CLK	AN4	CLK_ISP_TO_CAM_PMU2_24M_R	
SENSOR2_CLK	AN3	NC_SENSOR2_CLK_AP	
SENSOR3_CLK	AR3	NC_SENSOR3_CLK_AP	

R1240 33.2 1% 1/32W MF 01005 ROOM=SOC
CLK_ISP_TO_CAM_PMU1_24M

R1260 33.2 1% 1/32W MF 01005 ROOM=SOC
CLK_ISP_TO_CAM_PMU2_24M

PACK_OPTION=D53,D54,DEV
BOMOPTION=PRO

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: ISP
DRAWING NUMBER	051-05215
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SOC: DISPLAY / ISP

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 5 OF 21
OMIT_TABLE

24	OUT	90_MIPI_AP_TO_DISPLAY_CLK_P	CN51	MIPID_DPCLK			
24	OUT	90_MIPI_AP_TO_DISPLAY_CLK_N	CP51	MIPID_DNCLK			
24	OUT	90_MIPI_AP_TO_DISPLAY_D0_P	CN55	MIPID_DPDATA0			
24	OUT	90_MIPI_AP_TO_DISPLAY_D0_N	CP55	MIPID_DNDATA0			
24	OUT	90_MIPI_AP_TO_DISPLAY_D1_P	CP53	MIPID_DPDATA1			
24	OUT	90_MIPI_AP_TO_DISPLAY_D1_N	CN53	MIPID_DNDATA1			
24	OUT	NC_MIPI_AP_TO_DISPLAY_D2_P	CP47	MIPID_DPDATA2			
24	OUT	NC_MIPI_AP_TO_DISPLAY_D2_N	CN47	MIPID_DNDATA2			
24	OUT	90_MIPI_AP_TO_DISPLAY_D2_P	CN49	MIPID_DPDATA3			
24	OUT	90_MIPI_AP_TO_DISPLAY_D2_N	CP49	MIPID_DNDATA3			
		ANALOG_MIPI_AP_REXT	CL53	MIPID_REXT			

R1300 200 1% 1/32W MF 01005 800M=SUC

Dev breaks out to baseboard LPDP header

LPDP_RCAL_P/N are for LPDP TX, NC if unused

23		NC_DEV_LPDP_AP_TX0P	A40	LPDP_TX0P			
23		NC_DEV_LPDP_AP_TX0N	B40	LPDP_TX0N			
23		NC_DEV_LPDP_AP_TX1P	A42	LPDP_TX1P			
23		NC_DEV_LPDP_AP_TX1N	B42	LPDP_TX1N			
23		NC_DEV_LPDP_AP_TX2P	A43	LPDP_TX2P			
23		NC_DEV_LPDP_AP_TX2N	B43	LPDP_TX2N			
23		NC_DEV_LPDP_AP_TX3P	A45	LPDP_TX3P			
23		NC_DEV_LPDP_AP_TX3N	B45	LPDP_TX3N			
23		NC_DEV_LPDP_AP_AUXP	A47	LPDP_AUX_P			
23		NC_DEV_LPDP_AP_AUXN	B47	LPDP_AUX_N			
23		NC_DEV_LPDP_AP_RCALP	A49	LPDP_RCAL_P			
23		NC_DEV_LPDP_AP_RCALN	B49	LPDP_RCAL_N			

External LPDP not used

23		NC_LPDP_EXT_AP_TX0_P	A53	LPDP_EXT_TX0P			
23		NC_LPDP_EXT_AP_TX0_N	B53	LPDP_EXT_TX0N			
23		NC_LPDP_EXT_AP_TX1_P	A55	LPDP_EXT_TX1P			
23		NC_LPDP_EXT_AP_TX1_N	B55	LPDP_EXT_TX1N			
23		NC_LPDP_EXT_AP_TX2_P	A57	LPDP_EXT_TX2P			
23		NC_LPDP_EXT_AP_TX2_N	B57	LPDP_EXT_TX2N			
23		NC_LPDP_EXT_AP_TX3_P	A58	LPDP_EXT_TX3P			
23		NC_LPDP_EXT_AP_TX3_N	B58	LPDP_EXT_TX3N			
23		NC_LPDP_EXT_AP_AUX_P	A59	LPDP_EXT_AUX_P			
23		NC_LPDP_EXT_AP_AUX_N	B59	LPDP_EXT_AUX_N			
23		NC_LPDP_EXT_AP_RCAL_P	A60	LPDP_EXT_RCAL_P			
23		NC_LPDP_EXT_AP_RCAL_N	B60	LPDP_EXT_RCAL_N			

ISP_SPMI

		ISP_SPMI0_SCLK	BJ4	SPMI_ISP_TO_CAM_PMU1_CLK	OUT	47	90
		ISP_SPMI0_SDATA	BJ2	SPMI_ISP_BI_CAM_PMU1_DATA	BI	47	90
		ISP_SPMI1_SCLK	BK2	SPMI_ISP_TO_CAM_PMU2_CLK	OUT	50	90
		ISP_SPMI1_SDATA	BJ3	SPMI_ISP_BI_CAM_PMU2_DATA	BI	50	90

DWI

	1.8V	DWI_CLK	CM3	NC_SOC_DWI_CLK		23
		DWI_DO	CK5	NC_SOC_DWI_DATA		23

MIPI-D

		DISP_TOUCH_BSYNC0	CM11	GPIO_AP_CANARY4		24
		DISP_TOUCH_BSYNC1	CN6	NC_TOUCH_BSYNC1_DISP		23
		DISP_TOUCH_EB	CM9	NC_SOC_DISP_TOUCH_EB		23

GPIOS

	DISP_TE	F34	IO_AOP_FROM_DISPLAY_TE	IN	82	
	DISP_MIPI_PWR_DWN	D47	IO_AOP_TO_DISPLAY_MIPI_PWR_DWN	OUT	82	
	DISP_HPD	CK61	NC_EDP_HPD_DISP			23
	DISP_I2C_SCL	CL13	NC_SOC_DISP_I2C_SCL			23
	DISP_I2C_SDA	CL60	NC_SOC_DISP_I2C_SDA			23
	DISP_POL	CL62	NC_SOC_DISP_POL			23
	DISP_AGPIO	D45	NC_SOC_DISP_AGPIO			23
	DISP_EXT_HPD	BG3	NC_SOC_DISP_EXT_HPD			23
	DP_WAKEUP	CK17	GPIO_AP_CANARY3			24

DISPLAY_TE also provides WDG functionality

PP (dev board only)

SPMI Address Map

BUS	DEVICE	ADDR	LOCATION
SPMI0 ISP	Adams1	0x09	Top MLB
SPMI1 ISP	Adams2	0x09	Top MLB

NOTE: SPMI1 ISP is for D53P/D54 only

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Display
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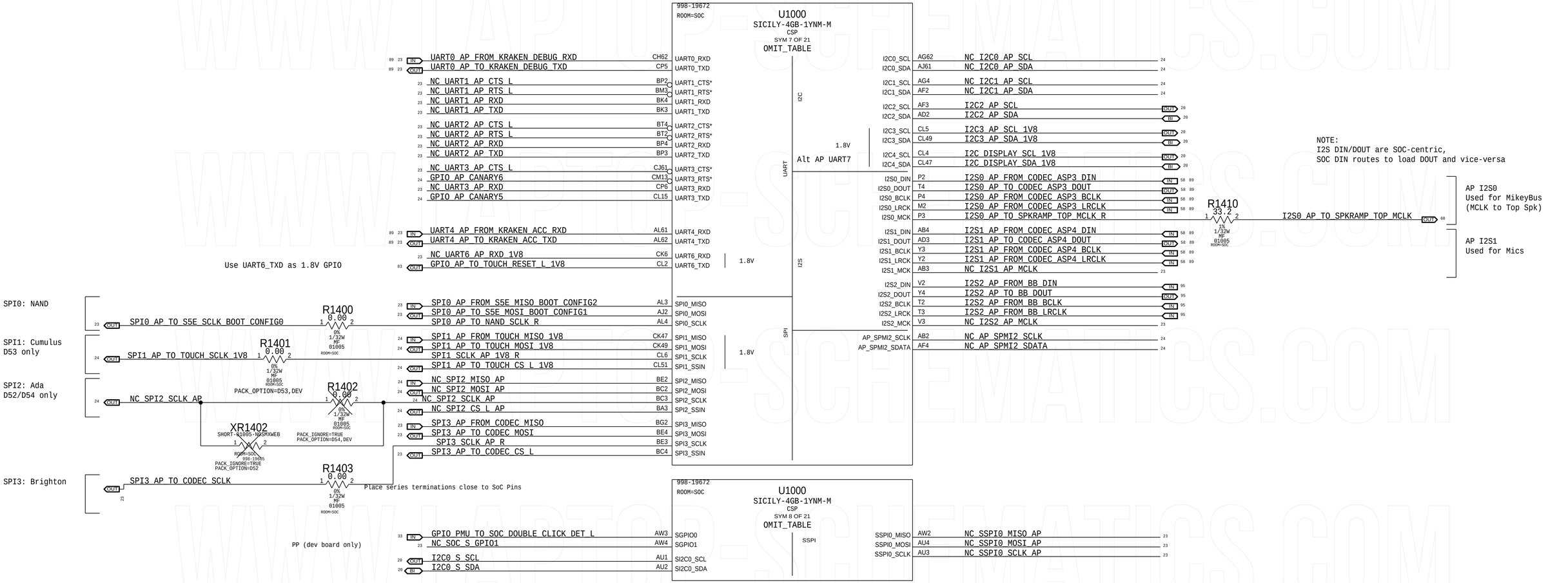
SOC: AP Serial



SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Serial
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SOC: AP GPIO

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 6 OF 21
OMIT_TABLE
GPIO

GPIO_BOARD_REV3	BT3	GPIO0	
GPIO_BOARD_REV2	BV2	GPIO1	
GPIO_BOARD_REV1	BY2	GPIO2	
GPIO_BOARD_REV0	BV3	GPIO3	
GPIO_AP_CANARY1	BY3	GPIO4	
GPIO_AP_CANARY2	BY4	GPIO5	
GPIO_AP_BI_CCG2B_SWDIO	CK58	GPIO6	
GPIO_AP_TO_CCG2B_SWCLK	CL11	GPIO7	
GPIO_AP_FROM_DISPLAY_PANEL_ID	CM5	GPIO8	
GPIO_AP_FROM_WLAN_TIME_SYNC	CK15	GPIO9	
GPIO_AP_TO_BB_PEAK_PWR_IND	CN9	GPIO10	
GPIO_AP_TO_BB_COREDUMP	CP7	GPIO11	
GPIO_AP_FROM_BB_RESET_DETECT_L	CK19	GPIO12	
GPIO_AP_FROM_CODEC_INT_L	CL17	GPIO13	
NC_AP_GPIO14	CJ60	GPIO14	
GPIO_AP_TO_SPKRAMP_TOP_RESET_L	BC62	GPIO15	
		GPIO16	BC61 GPIO_AP_FROM_BT_AUDIO_SYNC
		GPIO17	BC60 GPIO_AP_TO_AMUX_PMU_SYNC
		GPIO18	AW62 NC_DEV_AP_GPIO18
		GPIO19	AW61 NC_DEV_AP_GPIO19
		GPIO20	AW60 NC_DEV_AP_GPIO20
		GPIO21	AU62 NC_DEV_AP_GPIO21
		GPIO22	AU61 NC_DEV_AP_GPIO22
		GPIO23	AU60 NC_DEV_AP_GPIO23
		GPIO24	AR62 NC_DEV_AP_GPIO24
		GPIO25	AR61 GPIO_AP_TO_BB_TIME_MARK
		GPIO26	AN61 NC_DEV_AP_GPIO26

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: GPIO
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SOC: AOP

NOTE:
I2S DIN/DOUT are SOC-centric,
SOC DIN routes to load DOUT and vice-versa

SPI0_AOP_TO_IMU_R1_SCLK → R1601 33.2 1% 1/32W MF 01005 ROOM=SOC

AOP I2S0
Penrose, LDCM,
Borealis
(MCLK to Codec)

I2S0_AOP_TO_CODEC_MCLK1 → R1603 33.2 1% 1/32W MF 01005 ROOM=SOC
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN → R1606 0.00 0% 1/32W MF 01005 ROOM=SOC

AOP I2S1
Out to BotSpk,
TopSpk, Arc,
in from Sak.
(MCLK to Arc
and BotSpk)

I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT → R1607 0.00 0% 1/32W MF 01005 ROOM=SOC
I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK → R1608 0.00 0% 1/32W MF 01005 ROOM=SOC

SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK → R1622 33.2 1% 1/32W MF 01005 ROOM=SOC

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
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OMIT_TABLE

I2C0_AOP_SCL	F61	AOP_I2CM0_SCL	I2C	
I2C0_AOP_SDA	F62	AOP_I2CM0_SDA		
I2C1_AOP_SCL	F45	AOP_I2CM1_SCL		
I2C1_AOP_SDA	D42	AOP_I2CM1_SDA		
SPI0_AOP_FROM_IMU_R1_MISO	H60	AOP_SPI0_MISO	SPI	GPIO
SPI0_AOP_TO_IMU_R1_MOSI	H62	AOP_SPI0_MOSI		
SPI0_AOP_TO_IMU_R1_SCLK_R	G62	AOP_SPI0_SCLK		
I2C2_AOP_SCL	D55	AOP_SPI1_MISO	AOP I2C2 SCL	
I2C2_AOP_SDA	D57	AOP_SPI1_MOSI	AOP I2C2 SDA	
GPIO_AOP_TO_WLAN_CONTEXT_B	D58	AOP_SPI1_SCLK		
GPIO_AOP_TO_WLAN_CONTEXT_A	E34	AOP_SPI1_SSIN		
I2S0_AOP_FROM_CODEC_ASP1_DIN	D59	AOP_I2S0_DIN	I2S	
I2S0_AOP_TO_CODEC_ASP1_DOUT	E49	AOP_I2S0_DOUT		
I2S0_AOP_FROM_CODEC_ASP1_BCLK	D36	AOP_I2S0_BCLK		
I2S0_AOP_FROM_CODEC_ASP1_LRCLK	E36	AOP_I2S0_LRCK		
I2S0_AOP_TO_CODEC_MCLK1_R	F36	AOP_I2S0_MCK		
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_R	C36	AOP_I2S1_DIN		
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT_R_SOC	B36	AOP_I2S1_DOUT		
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK	E53	AOP_I2S1_BCLK		
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK	E51	AOP_I2S1_LRCK		
I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK_R	E47	AOP_I2S1_MCK		
UART1_AOP_FROM_BB_RXD	K62	AOP_SPMI1_SDATA	SUPPORTS UART	UART
UART1_AOP_TO_BB_TXD	G61	AOP_SPMI1_SCLK	ALT FUNC1	
SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	D43	AOP_SPMI0_SDATA	SUPPORTS UART	
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK_R	F47	AOP_SPMI0_SCLK	ALT FUNC1	
UART2_AOP_FROM_TOUCH_RXD	G60	AOP_UART2_RXD		
UART2_AOP_TO_TOUCH_TXD	E45	AOP_UART2_TXD		

AOP_FUNC0	E62	GPIO_SCM_AOP_FROM_IMU_DATARDY
AOP_FUNC1	F60	GPIO_SCM_AOP_TO_IMU_SPI_CS_L
AOP_FUNC2	E43	GPIO_AOP_FROM_PEARL_B2B_DETECT
AOP_FUNC3	E60	NC_DEV_AOP_FUNC3
AOP_FUNC4	K61	GPIO_SCM_AOP_FROM_R1_INT
AOP_FUNC5	D60	GPIO_AOP_TO_R1_COREDUMP_TRIGGER
AOP_FUNC6	D62	GPIO_AOP_TO_R1_TIME_SYNC_L
AOP_FUNC7	A36	GPIO_AOP_TO_CODEC_RESET_L
AOP_FUNC8	E42	GPIO_AOP_TO_BB_FORCE_PWM
AOP_FUNC9	E59	GPIO_AOP_FROM_IRCAM_B2B_DETECT
AOP_FUNC10	F57	GPIO_SCM_AOP_TO_R1_SPI_CS_L
AOP_FUNC11	F42	NC_AOP_FUNC11
AOP_FUNC12	D40	GPIO_AOP_TO_ALS_COEX
AOP_FUNC13	F58	GPIO_AOP_TO_NFC_IRONMAN_EN
AOP_FUNC14	F53	GPIO_AOP_FROM_TOUCH_CTS
AOP_FUNC15	E58	GPIO_SCM_AOP_BI_PROX_INT_L
AOP_FUNC16	E40	GPIO_SCM_AOP_FROM_ALS_INT_L
AOP_FUNC17	F51	GPIO_SCM_AOP_FROM_EIGER_INT_L
AOP_FUNC18	E57	GPIO_SCM_AOP_FROM_COMPASS_INT
AOP_FUNC19	F40	GPIO_SCM_AOP_FROM_JARVIS_INT
AOP_FUNC20	D38	GPIO_AOP_FROM_TOUCH_INT_L
AOP_FUNC21	E55	NC_AOP_FUNC21
AOP_FUNC22	E38	NC_DEV_AOP_FUNC22

SPMI Address Map

BUS	DEVICE	ADDR	LOCATION
SPMI0 AOP	WLAN	0x0E	Bottom MLB
SPMI0 AOP	Ceres (P)	0x0C	D52/D53: Top MLB D54: Bottom MLB
SPMI0 AOP	Ceres (F)	0x0B	D53/D54: Top MLB D52: Bottom MLB

NOTE: Ceres (F) default address is 0x0C, programmed to 0x0B on SMT line

BUS	DEVICE	ADDR	LOCATION
SPMI0 NUB	Cota	0x0F	Top MLB
SPMI0 NUB	DotaraLV	0x0E	Top MLB

Touch UART
D52/D54: WIRED TO ADA
D53: WIRED TO TOUCH B2B

R1621 1.00M 5% 1/32W MF 01005
R1620 1.00M 5% 1/32W MF 01005

SOC: SMC

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
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OMIT_TABLE

I2C0_SMC_SCL	G4	SMC_I2CM0_SCL	I2C
I2C0_SMC_SDA	F26	SMC_I2CM0_SDA	
I2C1_SMC_SCL	G2	SMC_I2CM1_SCL	
I2C1_SMC_SDA	H2	SMC_I2CM1_SDA	
I2C2_SMC_SCL	G3	SMC_I2CM2_SCL	
I2C2_SMC_SDA	F2	SMC_I2CM2_SDA	

SOC: NUB

998-19672
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
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OMIT_TABLE

SPMI0_NUB_TO_PMU_DOTARA_CLK_R	D32	NUB_SPMI0_SCLK	SPMI
SPMI0_NUB_BI_PMU_DOTARA_DATA	D4	NUB_SPMI0_SDATA	
SWD_NUB_TO_PMU_TOUCH_SWCLK	F6	NUB_SWD_TCK_OUT0	SWD
SWD_NUB_BI_PMU_SWDIO	F13	NUB_SWD_TMS0	
NC_SWD_NUB_BI_TOUCH_SWDIO	F11	NUB_SWD_TMS1	
IO_NUB_FROM_KRAKEN_DOCK_CONNECT	F30	NUB_DOCK_CONNECT	DOCK
IO_NUB_FROM_KRAKEN_INT	E30	NUB_DOCK_ATTENTION	
GPIO_NUB_FROM_CCG2B_INT_L	D2	NUB_GPIO_0	GPIO
GPIO_NUB_FROM_GECKO_IRQ_L	E4	NUB_GPIO_1	
GPIO_NUB_FROM_PARROT_INT_L	E3	NUB_GPIO_2	
GPIO_NUB_TO_GECKO_RESET_L	F28	NUB_GPIO_3	
GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	E2	NUB_GPIO_4	
NC_NUB_GPIO5	F3	NUB_GPIO_5	
GPIO_AOP_CANARY7	E28	NUB_GPIO_6	
SWD_DOCK_TO_AP_SWCLK	E5	JTAG_TCK	JTAG
SWD_DOCK_BI_AP_SWDIO	C34	JTAG_TMS	
GND	D6	JTAG_SEL	
NC_DEV_JTAG_TDI	B34	JTAG_TDI	
NC_DEV_JTAG_TDO	E6	JTAG_TDO	
NC_DEV_JTAG_TRST_L	D5	JTAG_TRST*	
90_EUSB_DBG_PARROT_BI_AP_N	B30	DBG_USB_EDM	DEBUG USB
90_EUSB_DBG_PARROT_BI_AP_P	A30	DBG_USB_EDP	
ANALOG_DBG_USB_RESREF	D30	DBG_USB_RESREF	
PP1V2_S2	E32	DBG_PROBE_VALID	
IO_PMU_TO_SYSTEM_RESET_L	D51	COLD_RESET*	MISC
IO_PMU_TO_SYSTEM_RESET_L	D53	CFSB_AON	
CLK_PMU_TO_AOP_32K	D49	RT_CLK32768	
IO_SOC_TO_PMU_WDOG_RESET	D34	WDOG	
IO_AON_TO_AP_XTAL_CFSB	A34	AON_SLEEP1_RESET*	
NC_CLK_NUB_TO_TOUCH_24M	F15	NUB_CLK_OUT0	
GND	CP4	KIS_DFU_SELECT	

Touch SWDIO: Wired to Touch B2B (D52/D54)
Touch SWDIO: No connect (D53)

Gecko IRQ needs SOC weak internal PU
Parrot INT needs external or SOC pull-up

Can use Dotara GPIO for BBPMU Clock EN

SPMI0_NUB_TO_PMU_DOTARA_CLK → R1610 33.2 1% 1/32W MF 01005 ROOM=SOC

R1650 200 1% 1/32W MF 01005 ROOM=SOC

XR1660 SHORT-01005-NOSMXWEB ROOM=SOC 998-19035 PACK_IGNORE=TRUE PACK_OPTION=D52
R1660 0.00 0% 1/32W MF 01005 ROOM=SOC PACK_OPTION=D54_DEV PACK_IGNORE=TRUE

NC_CLK_NUB_TO_TOUCH_24M

KIS_DFU_SELECT:
POR = 0 (GND): USB0 for DFU (legacy)
Debug = 1 (1V2): USB1 for DFU (Kanzi-in-System)

SYNCING: D52, D53, D54, DEV

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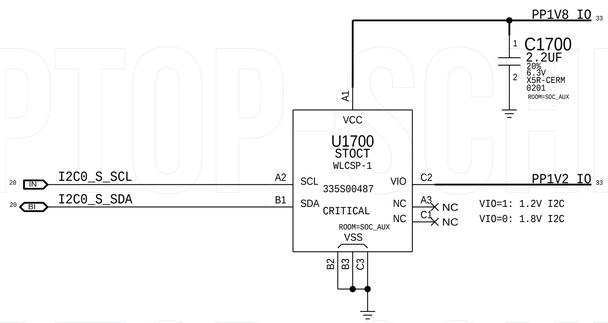
OCELOT



SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Ocelot
DRAWING NUMBER	051-05215
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SOC: CPU/GPU

PP_CPU_PCORE 33

C1802 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1803 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1801 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1807 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV
C1805 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV
2020-MLCC
138S00317 ROOM=SOC_FILT C1804 11UF 20% 4V X5R 0402 ROOM=SOC_FILT C1806 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1805 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT C1807 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
PACK_IGNORE=TRUE PACK_OPTION=D54 PACK_IGNORE=TRUE PACK_OPTION=D54

PP_CPU_ECORE 33

C1895 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1894 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1893 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV
C1891 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1892 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1893 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
PACK_IGNORE=TRUE PACK_OPTION=D54

ANALOG_PCPU_SENSE_P 89 27 OUT
ANALOG_ECPU_SENSE_SE 89 OUT

998-19672 ROOM=SOC U1000 SICILY-4GB-1YNM-M CSP SYM 12 OF 21 OMIT_TABLE CPU/GPU

AP56	VDD_PCPU	VDD_GPU	AA27
AP48	VDD_PCPU	VDD_GPU	AA31
AP52	VDD_PCPU	VDD_GPU	AA44
AT41	VDD_PCPU	VDD_GPU	AA48
AT50	VDD_PCPU	VDD_GPU	AA52
AT54	VDD_PCPU	VDD_GPU	AC25
AV39	VDD_PCPU	VDD_GPU	AC33
AV54	VDD_PCPU	VDD_GPU	AC41
BF39	VDD_PCPU	VDD_GPU	AC50
BH54	VDD_PCPU	VDD_GPU	AE27
BL39	VDD_PCPU	VDD_GPU	AE35
BL48	VDD_PCPU	VDD_GPU	AE44
BL52	VDD_PCPU	VDD_GPU	AE48
BN37	VDD_PCPU	VDD_GPU	AE52
BN41	VDD_PCPU	VDD_GPU	N31
BN46	VDD_PCPU	VDD_GPU	N35
BN50	VDD_PCPU	VDD_GPU	N39
BN54	VDD_PCPU	VDD_GPU	N44
BR44	VDD_PCPU	VDD_GPU	R25
BR52	VDD_PCPU	VDD_GPU	R33
BU37	VDD_PCPU	VDD_GPU	R41
BU50	VDD_PCPU	VDD_GPU	R50
BW39	VDD_PCPU	VDD_GPU	U27
BW52	VDD_PCPU	VDD_GPU	U31
CA37	VDD_PCPU	VDD_GPU	U44
CA50	VDD_PCPU	VDD_GPU	U48
CC37	VDD_PCPU	VDD_GPU	U52
CC44	VDD_PCPU	VDD_GPU	W29
CC52	VDD_PCPU	VDD_GPU	W46
		VDD_GPU	AE31
BL37	VDD_PCPU_SENSE	VDD_GPU_SENSE	AH29
AT29	VDD_ECPU		
AT33	VDD_ECPU		
AT37	VDD_ECPU		
AV31	VDD_ECPU		
BB27	VDD_ECPU		
BD37	VDD_ECPU		
BF31	VDD_ECPU		
BF35	VDD_ECPU		
BH37	VDD_ECPU		
BL33	VDD_ECPU_SENSE		

ANALOG_GPU_SENSE_P 89 OUT

PP_GPU 33

C1831 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1832 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1833 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1834 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT

PP_SOC_S1 33

C1860 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1861 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D54
C1830 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1862 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1863 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D54
138S00313 C1863 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV 2020-MLCC
C1864 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1866 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT

SOC: SOC

998-19672 ROOM=SOC U1000 SICILY-4GB-1YNM-M CSP SYM 13 OF 21 OMIT_TABLE SOC

AY25	VDD_SOC_S1	VDD_SOC_S1	BF56
AA14	VDD_SOC_S1	VDD_SOC_S1	BL18
AA18	VDD_SOC_S1	VDD_SOC_S1	BL23
AH20	VDD_SOC_S1	VDD_SOC_S1	BL31
AM54	VDD_SOC_S1	VDD_SOC_S1	BN20
AH37	VDD_SOC_S1	VDD_SOC_S1	BN29
AH46	VDD_SOC_S1	VDD_SOC_S1	AE14
AH54	VDD_SOC_S1	VDD_SOC_S1	BR18
AK10	VDD_SOC_S1	VDD_SOC_S1	BR23
AK14	VDD_SOC_S1	VDD_SOC_S1	BR27
AK18	VDD_SOC_S1	VDD_SOC_S1	BR31
AK23	VDD_SOC_S1	VDD_SOC_S1	BR35
AK27	VDD_SOC_S1	VDD_SOC_S1	BU25
AA23	VDD_SOC_S1	VDD_SOC_S1	BU33
AK31	VDD_SOC_S1	VDD_SOC_S1	BW35
AK35	VDD_SOC_S1	VDD_SOC_S1	CE44
AK39	VDD_SOC_S1	VDD_SOC_S1	CE52
AK44	VDD_SOC_S1	VDD_SOC_S1	AE18
AK48	VDD_SOC_S1	VDD_SOC_S1	CG18
AK52	VDD_SOC_S1	VDD_SOC_S1	CG29
AK56	VDD_SOC_S1	VDD_SOC_S1	N14
AM16	VDD_SOC_S1	VDD_SOC_S1	N18
AM25	VDD_SOC_S1	VDD_SOC_S1	N23
AM33	VDD_SOC_S1	VDD_SOC_S1	N27
AC16	VDD_SOC_S1	VDD_SOC_S1	N37
AM50	VDD_SOC_S1	VDD_SOC_S1	N56
AP10	VDD_SOC_S1	VDD_SOC_S1	R16
AP14	VDD_SOC_S1	VDD_SOC_S1	U14
BH25	VDD_SOC_S1	VDD_SOC_S1	AE23
AP23	VDD_SOC_S1	VDD_SOC_S1	U18
AP27	VDD_SOC_S1	VDD_SOC_S1	U23
AP31	VDD_SOC_S1	VDD_SOC_S1	W12
N46	VDD_SOC_S1	VDD_SOC_S1	W20
BL27	VDD_SOC_S1	VDD_SOC_S1	AH12
AT12	VDD_SOC_S1	VDD_SOC_S1	AP39
CA12	VDD_SOC_S1		
AT20	VDD_SOC_S1		
AV10	VDD_SOC_S1		
AV14	VDD_SOC_S1		
AV18	VDD_SOC_S1		
AV23	VDD_SOC_S1		
AY16	VDD_SOC_S1		
BB10	VDD_SOC_S1		
BB14	VDD_SOC_S1		
BB18	VDD_SOC_S1		
BB23	VDD_SOC_S1		
AE10	VDD_SOC_S1		
BD12	VDD_SOC_S1		
BD20	VDD_SOC_S1		
BF18	VDD_SOC_S1		
BF23	VDD_SOC_S1		
	VDD_SOC_SENSE	AP16	ANALOG_SOC_SENSE_P 89 OUT

SOC: SRAM

PP_CPU_SRAM 33

C1812 10UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV
C1812 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D54
138S00313 C1811 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT 2020-MLCC
C1808 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV
2020-MLCC
ROOM=SOC_FILT C1809 14UF 20% 4V X5R 0402-D2X-1
138S00317 ROOM=SOC_FILT C1810 11UF 20% 4V X5R 0402
ROOM=SOC_FILT C1808 14UF 20% 4V X5R 0402-D2X-1
PACK_IGNORE=TRUE PACK_OPTION=D54

PP_SRAM_S1 33

138S00313 C1872 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D54 2020-MLCC
C1872 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D52,D53,DEV
C1873 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1874 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1865 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT PACK_OPTION=D52,D53

998-19672 ROOM=SOC U1000 SICILY-4GB-1YNM-M CSP SYM 14 OF 21 OMIT_TABLE SRAM

AT46	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AH50
AV27	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM12
CC48	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM20
AV35	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM29
BB39	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM37
BD54	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM46
BH33	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AT16
BL44	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AT25
BR39	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AY12
BR48	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AY20
CC39	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	BD16
		VDD_SRAM_SOC_S1	BD25
R29	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BH12
R37	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BH20
AC29	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN16
AC37	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN25
AC46	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN33
R46	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN8
W25	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BU12
W33	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BU20
W50	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BU29
		VDD_SRAM_SOC_S1	BU52
		VDD_SRAM_SOC_S1	CA16
		VDD_SRAM_SOC_S1	CA25
		VDD_SRAM_SOC_S1	CA33
		VDD_SRAM_SOC_S1	CE29
		VDD_SRAM_SOC_S1	CE50
		VDD_SRAM_SOC_S1	AC12
		VDD_SRAM_SOC_S1	AC20
		VDD_SRAM_SOC_S1	AH16
		VDD_SRAM_SOC_S1	AH25
		VDD_SRAM_SOC_S1	AH33
		VDD_SRAM_SOC_S1	AH41
		VDD_SRAM_SOC_S1	AM56
		VDD_SRAM_SOC_S1	L25
		VDD_SRAM_SOC_S1	N52
		VDD_SRAM_SOC_S1	R20
		VDD_SRAM_SOC_S1	U12
		VDD_SRAM_SOC_S1	W16

PP_SRAM_S1 33

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: Power (CPU/GPU & SRAM & SOC)
DRAWING NUMBER: 051-05215
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SUBSYSTEM SPECIFIC BOM TABLES

2.2uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	(C1970)	CAP,CER,X5R,2.2UF,20%,6.3V,0201

SOC: FIXED

U1000 SICILY-4GB-1YNM-M CSP SYM 17 OF 21 OMIT_TABLE — 998-19672, ROOM=SOC

AP8	VDD_FIXED_S1	J12	VDD_FIXED_PCIE_REFBUF_S1
AV56	VDD_FIXED_S1	AP46	VDD_FIXED_PCPU_S1
CA52	VDD_FIXED_S1	AY39	VDD_FIXED_ECPU_S1
CE16	VDD_FIXED_S1	CF60	VDD_FIXED_MTR_S1
CG31	VDD_FIXED_S1	AE41	VDD_FIXED_PLL_GPU_S1
CG52	VDD_FIXED_MIPID_S1	CE12	VDD_FIXED_PLL_DDR0_S1
CG56	VDD_FIXED_MIPIC_S1	BP60	VDD_FIXED_PLL_DDR1_S1
CK55	VDD_FIXED_MIPID_PLL_S1	AC10	VDD_FIXED_PLL_DDR2_S1
J20	VDD_FIXED_USB_S1	P60	VDD_FIXED_PLL_DDR3_S1
J52	VDD_FIXED_LPDP_TX_S1	BH27	VDD_FIXED_PLL_SOC_S1
J56	VDD_FIXED_LPDP_TX_S1	CA35	VDD_FIXED_PLL_ANE_S1
CE33	VDD_FIXED_LPDP_RX_S1	F9	VDD_FIXED_XTAL_S1
CE37	VDD_FIXED_LPDP_RX_S1		
CE41	VDD_FIXED_LPDP_RX_S1		
CE46	VDD_FIXED_LPDP_RX_S1		
L16	VDD_FIXED_PCIE_S1		
L20	VDD_FIXED_PCIE_S1		
N16	VDD_FIXED_PCIE_S1		

FIXED

PP0V78_SOC_FIXED_S1 (33) → C1901 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1907 220PF 5% 25V C0G 01005 ROOM=SOC_FILT; C1908 220PF 5% 25V C0G 01005 ROOM=SOC_FILT; C1909 220PF 5% 25V C0G 01005 ROOM=SOC_FILT

PP0V78_SOC_FIXED_S1 (33) → C1906 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1905 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP0V78_SOC_FIXED_S1 (33) → C1910 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

GND (33) (Not used for MLBs)

PP0V78_SOC_FIXED_S1 (33) → C1916 4UF 20% 4V X5R 0201 ROOM=SOC_FILT; C1918 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1917 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP0V78_SOC_FIXED_S1 (33) → C1922 4UF 20% 4V X5R 0201 ROOM=SOC_FILT; C1921 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1920 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

OMIT XW1940 SHORT-20L-0.05MM-SM (ROOM=SOC_FILT) — PP0V78_SOC_FIXED_S1 (33) ↔ PP0V78_SOC_FIXED_S1 (33)

C1940 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

C1941 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1942 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1902 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP0V78_SOC_FIXED_S1 (33)

PP0V78_VDD_FIXED_XTAL — VOLTAGE=0.8 → R1970 20.0 5% 1/32W MF 01005 ROOM=SOC_FILT → PP0V78_SOC_FIXED_S1 (33)

C1970 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT [SS] MURATA

SOC: VDD12

U1000 SICILY-4GB-1YNM-M CSP SYM 18 OF 21 OMIT_TABLE — 998-19672, ROOM=SOC

F22	VDD12_USB	CG12	VDDIO12_GRP1_S2
F24	VDD12_USB_DEBUG_S2	AY56	VDDIO12_GRP3
AP44	VDD12_PLL_PCPU	BD56	VDDIO12_GRP3
AY37	VDD12_PLL_ECPU	BL56	VDDIO12_GRP3
AE39	VDD12_PLL_GPU	CG16	VDDIO12_GRP4
F7	VDD12_XTAL_S1	CG20	VDDIO12_GRP4
CL9	VDD12_AMUX_S2	CG23	VDDIO12_GRP4
CG54	VDD12_MIPIC	AH8	VDDIO12_GRP5
CK53	VDD12_MIPID_S1	AM8	VDDIO12_GRP5
AM41	VDD12_TSADC_CPU0	AT8	VDDIO12_GRP5
AT39	VDD12_TSADC_CPU1	AY8	VDDIO12_GRP5
AP35	VDD12_TSADC_SOC0	BD8	VDDIO12_GRP5
AC52	VDD12_TSADC_SOC1	J14	VDD12_PCIE
R12	VDD12_TSADC_SOC2	J18	VDD12_PCIE
J27	VDDIO12_AOP_S2	CH60	VDD12_MTR
J31	VDDIO12_AOP_S2	L50	VDD12_LPDP_TX
J35	VDDIO12_AOP_S2	L54	VDD12_LPDP_TX
J39	VDDIO12_AOP_S2	CG35	VDD12_LPDP_RX
J44	VDDIO12_AOP_S2	CG39	VDD12_LPDP_RX
J48	VDDIO12_AOP_S2	CG44	VDD12_LPDP_RX
BF27	VDD12_PLL_SOC_S1	CG48	VDD12_LPDP_RX
BH29	VDD12_PLL_SOC_S1	CG37	VDD12_LPDP_RX
CE14	VDDIO12_PLL_DDR0_S1	N50	VDD12_EFUSE1
BM60	VDDIO12_PLL_DDR1_S1	W18	VDD12_EFUSE2
AC8	VDDIO12_PLL_DDR2_S1	AM39	VDD12_EFUSE3
M60	VDDIO12_PLL_DDR3_S1	N48	VDD12_EFUSE4
CC35	VDD12_PLL_ANE	AP37	VDD12_EFUSE5
		R14	VDD12_FMON
		L12	VDD12_PCIE_REFBUF
		L33	VDD12_ULPPLL_S2
		K60	VDD12_ADC_SOC_S1

PP1V2_IO (33) — Place cap near pin → C1935 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S2 (33) — Place cap near pin → C1900 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

RADAR #: 54364908 PLACE NEAR SOC

OMIT XW1930 SHORT-20L-0.05MM-SM (ROOM=SOC_FILT)

PP1V2_SOC (33) ↔ PP1V2_SOC_FILT — VOLTAGE=1.2 — To ANE (17)

Place 01005 caps near pins (incl. ANE)

C1926 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1927 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1928 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S1 (33) → FL1950 240-OHM-25%-0.20A-1.0DCR 0100S ROOM=SOC_FILT 155S0755 → PP1V2_S1_XTAL — VOLTAGE=1.2

C1946 4UF 20% 4V X5R 0201 ROOM=SOC_FILT; C1903 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S2 (33) → CL9

PP1V2_IO (33) → CG54

PP1V2_S1 (33) → CK53

C1998 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1999 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1997 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1996 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_IO (33) → R12

PP1V2_S2 (33) — Place cap near pins → C1923 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1924 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S1 (33) → C1963 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1964 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S1 (33) — Shares decap with other S1 rails

17 PP1V2_SOC_FILT — Share cap with VDD12_PLL_ECPU/_PCPU/_GPU

C1904 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

[LAYOUT] VDDIO12_GRPx: Isolation >= 2.5nH from other nets on the same domain

OMIT XW1901 SHORT-10L-0.1MM-SM (ROOM=SOC_FILT, NO_XNET_CONNECTION)

PP1V2_IO_GRP3 — VOLTAGE=1.2 → C1945 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

OMIT XW1902 SHORT-10L-0.1MM-SM (ROOM=SOC_FILT, NO_XNET_CONNECTION)

PP1V2_IO_GRP4 — VOLTAGE=1.2 → C1947 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

C1948 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

PP1V2_S2 (33); PP1V2_IO (33); PP1V2_SOC (33); PP1V2_SOC (33)

C1937 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT; C1955 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1950 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

GND (33)

PP1V2_IO (33)

C1931 0.01UF 10% 6.3V X5R 01005 ROOM=SOC_FILT; C1932 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1933 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

Used for SoC fusing GND on all systems

PP1V2_VDD12_FMON — VOLTAGE=1.2 → 49.9 R1960 1% MF 1/32W 01005 ROOM=SOC_FILT → PP1V2_IO (33)

PP1V2_VDD12_ULPPLL_S2 — VOLTAGE=1.2 → 49.9 R1961 1% MF 1/32W 01005 ROOM=SOC_FILT → PP1V2_S2 (33); PP1V2_S1 (33)

C1938 4UF 20% 4V X5R 0201 ROOM=SOC_FILT; C1995 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT; C1936 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

[LAYOUT] VDD12_PCIE_REFBUF: Inductance from C1995.1 to PP1V2_SOC plane >1.5nH @ 100MHz

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: Power (Fixed & 1V2)

DRAWING NUMBER: 051-05215 — SIZE: D

REVISION: 4.6.0

BRANCH:

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SOC: DDR

998-19672
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 16 OF 21
OMIT_TABLE
DDR

33 PP_DCS_S1

C2088 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2087 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2086 2.7UF 20% 4V X5R 0201 ROOM=SOC_FILT 2020-MLCC (138S00321)
C2085 2.7UF 20% 4V X5R 0201 ROOM=SOC_FILT 2020-MLCC (138S00321)
PLACE CAPS ON SOC CORNERS

BR10 VDD_DCS_DDR0_S1
CE10 VDD_DCS_DDR0_S1
BR54 VDD_DCS_DDR1_S1
CE54 VDD_DCS_DDR1_S1
AA10 VDD_DCS_DDR2_S1
L10 VDD_DCS_DDR2_S1
AC54 VDD_DCS_DDR3_S1
R54 VDD_DCS_DDR3_S1

89 OUT ANALOG_DCS_SENSE_SE
AD62 VDD_DCS_SENSE

33 PP0V6_VDDQL_S1

C2093 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2092 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2091 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2090 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
PLACE CAPS ON SOC CORNERS

BE1 VDDQL_DDR0_S1
BJ1 VDDQL_DDR0_S1
BM1 VDDQL_DDR0_S1
BU8 VDDQL_DDR0_S1
CE8 VDDQL_DDR0_S1
CF1 VDDQL_DDR0_S1
CJ1 VDDQL_DDR0_S1
CL1 VDDQL_DDR0_S1
BC63 VDDQL_DDR1_S1
BG63 VDDQL_DDR1_S1
BK63 VDDQL_DDR1_S1
BR56 VDDQL_DDR1_S1
CC56 VDDQL_DDR1_S1
CD63 VDDQL_DDR1_S1
CH63 VDDQL_DDR1_S1
CK63 VDDQL_DDR1_S1
AD1 VDDQL_DDR2_S1
AG1 VDDQL_DDR2_S1
AL1 VDDQL_DDR2_S1
E1 VDDQL_DDR2_S1
G1 VDDQL_DDR2_S1
K1 VDDQL_DDR2_S1
L8 VDDQL_DDR2_S1
W8 VDDQL_DDR2_S1
AB63 VDDQL_DDR3_S1
AE56 VDDQL_DDR3_S1
AF63 VDDQL_DDR3_S1
AJ63 VDDQL_DDR3_S1
D63 VDDQL_DDR3_S1
F63 VDDQL_DDR3_S1
H63 VDDQL_DDR3_S1
R56 VDDQL_DDR3_S1

89 OUT ANALOG_VDDQL_SENSE_SE
AD60 VDDQL_SENSE

VDD2_DDR0_S2 BA2
VDD2_DDR0_S2 BP1
VDD2_DDR0_S2 BV1
VDD2_DDR0_S2 CB1
VDD2_DDR0_S2 CL3
VDD2_DDR1_S2 BA62
VDD2_DDR1_S2 BM63
VDD2_DDR1_S2 BT63
VDD2_DDR1_S2 BY63
VDD2_DDR1_S2 CL61
VDD2_DDR2_S2 AB1
VDD2_DDR2_S2 AN2
VDD2_DDR2_S2 D3
VDD2_DDR2_S2 P1
VDD2_DDR2_S2 V1
VDD2_DDR3_S2 AN62
VDD2_DDR3_S2 D61
VDD2_DDR3_S2 M63
VDD2_DDR3_S2 T63
VDD2_DDR3_S2 Y63
VDDIO11_RET_DDR0_S2 CJ4
VDDIO11_RET_DDR1_S2 BT60
VDDIO11_RET_DDR2_S2 K4
VDDIO11_RET_DDR3_S2 Y60

C2080 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2081 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2082 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2083 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
PLACE CAPS ON SOC CORNERS
PP1V06_S2 33

VDD1_DDR0_S2 BA1
VDD1_DDR0_S2 CM2
VDD1_DDR1_S2 BA63
VDD1_DDR1_S2 CM62
VDD1_DDR2_S2 AN1
VDD1_DDR2_S2 C2
VDD1_DDR3_S2 AN63
VDD1_DDR3_S2 C62

C2096 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
C2097 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
C2098 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
C2099 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
PLACE CAPS ON SOC CORNERS
PP1V8_S2 33

SOC: AOP/AVE/ISP/USB

998-19672
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 15 OF 21
OMIT_TABLE
LOW/AVE/DISP

33 PP0V7_VDD_LOW_S2

C2000 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2001 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
PLACE AT SOC BALLS

R2021 10 5% 1/32W MF 01005 ROOM=SOC_FILT
C2020 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C2050 0.47UF 20% 6.3V X5R 01005 ROOM=SOC_FILT
R2022 49.9 1% 1/32W MF 01005 ROOM=SOC_FILT
C2052 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

PP0V7_VDD_LOW_FLPPLL VOLTAGE=0.7
PP0V7_VDD_LOW_ULPPLL VOLTAGE=0.7

J25 VDD_LOW_S2
L29 VDD_LOW_S2
L37 VDD_LOW_S2
L41 VDD_LOW_S2
L46 VDD_LOW_S2
J23 VDD_LOW_USB_DEBUG_S2
J33 VDD_LOW_FLPPLL_S2
L31 VDD_LOW_ULPPLL_S2

VDDIO18_GRP1 CG10
VDDIO06_GRP1_1 CK9
VDDIO06_GRP1_2 CK11
PP0V6_VDDIO06_GRP1_1 VOLTAGE=0.6
PP0V6_VDDIO06_GRP1_2 VOLTAGE=0.6

C2073 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2010 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2011 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
PP1V8_IO 33

VDDIO06_GRPx RADAR #: 48907718
Cmin = 4.7uF
Loop R < 0.2 ohm
Loop L < 1nH

33 PP_AVE_S1

C2026 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2025 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2024 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=DS4

BW23 VDD_AVE_S1
BW27 VDD_AVE_S1
BW31 VDD_AVE_S1
CA29 VDD_AVE_S1
CC23 VDD_AVE_S1
CC27 VDD_AVE_S1
CC31 VDD_AVE_S1
CE20 VDD_AVE_S1
CE25 VDD_AVE_S1
CG27 VDD_AVE_S1

33 PP_DISP_S1

C2033 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2030 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2032 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT

BF10 VDD_DISP_S1
BF14 VDD_DISP_S1
BH16 VDD_DISP_S1
BH8 VDD_DISP_S1
BL10 VDD_DISP_S1
BL14 VDD_DISP_S1
BN12 VDD_DISP_S1
BR14 VDD_DISP_S1
BU16 VDD_DISP_S1
BW14 VDD_DISP_S1
BW18 VDD_DISP_S1
CA20 VDD_DISP_S1
CC14 VDD_DISP_S1
CC18 VDD_DISP_S1

SYNCING: D52, D53, D54, DEV

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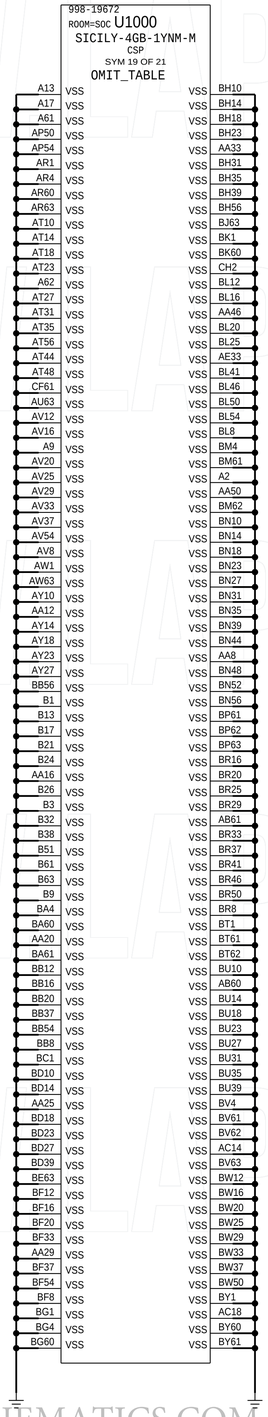
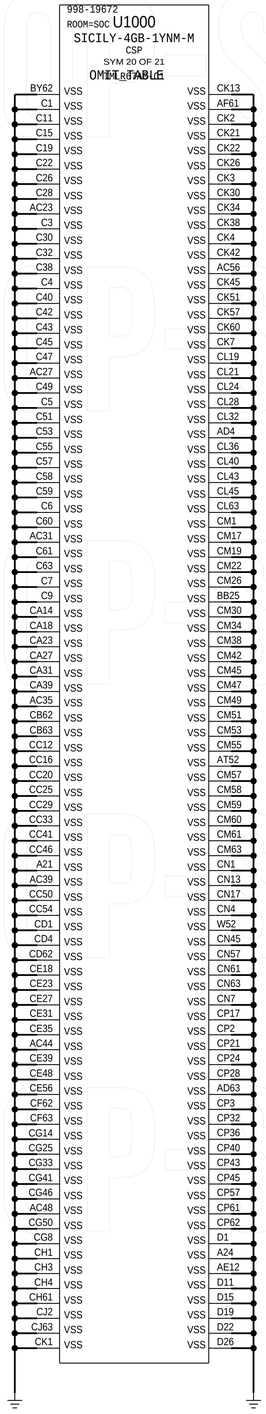
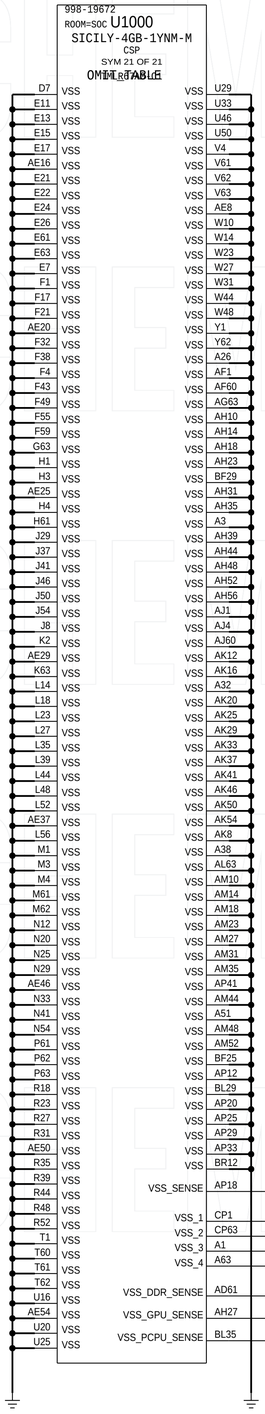
SOC: GND







SYNCING: D52, D53, D54, DEV

PAGE TITLE
SOC: Power (GND)

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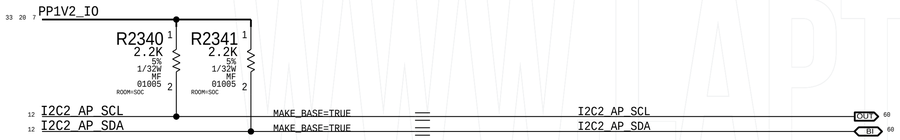
AP/ISP I2C

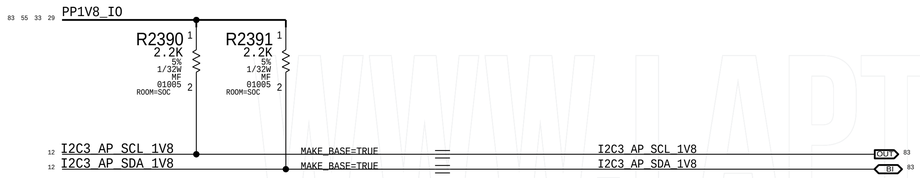
AP I2C0 (Unused)

AP I2C1 (Unused)

AP I2C2

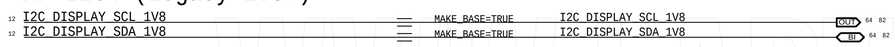


MASTER	AP	NUMBER	I2C2	DIAGS NUMBER	2	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Top Spk Amp	1.2V	0x40	0x80, 0x81	1MHz	MLB		



MASTER	AP	NUMBER	I2C3	DIAGS NUMBER	3	SPEED	400kHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Touch EEPROM	1.8V	0x51	0xA2, 0xA3	400kHz	Touch Flex		
Babbage (TFE)	1.8V	0x4B	0x96, 0x97	1MHz	Touch Flex	D52/D54 only	
NOTE: For D52/D54, bus can either be mastered by SoC or Ada							
Roswell	1.8V	0x10	0x20, 0x21	400kHz	Touch Flex	D53 only	
NOTE: Roswell is I2C for D53-only (AID for D52/D54)							

AP I2C4 (Legacy 1.8V)



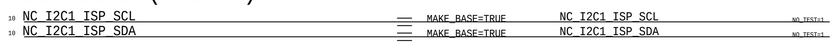
MAKE_BASE for Display PMIC intentional, test feature only

MASTER	AP	NUMBER	I2C4	DIAGS NUMBER	4	SPEED	400kHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Display PMIC	1.8V	0x50	0xA0, 0xA1	400kHz	MLB		
NOTE: SoC is master for FCT *ONLY*, DDIC is master for normal operation							

SI2C0

ISP I2C0

ISP I2C1 (Unused)



SYNCING: D52, D53, D54

PAGE TITLE	SOC: Aliases: I2C AP/ISP
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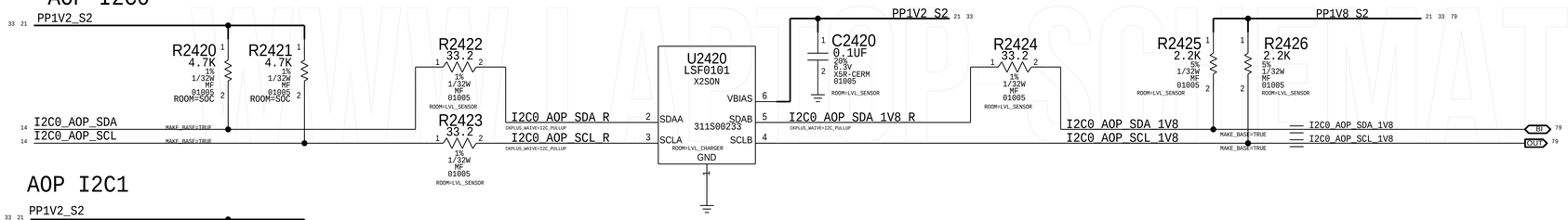
AOP/SMC I2C

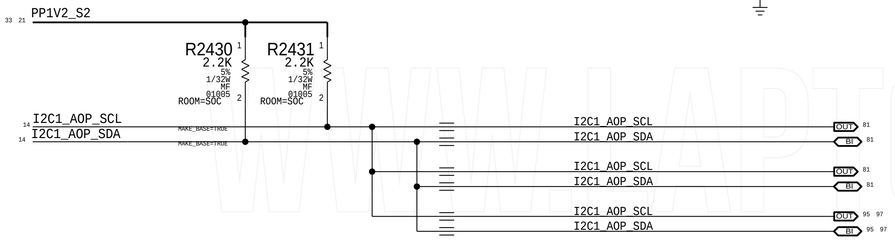
AOP I2C0



MASTER	AOP	NUMBER	I2C0	DIAGS NUMBER	5	SPEED	750kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Prox	1.8V	0x58	0xB0, 0xB1	1MHz	Sensor Flex
ALS	1.8V	0x29	0x52, 0x53	1MHz	Sensor Flex
Grievous	1.8V	0x33	0x66, 0x67	1MHz	Sensor Flex
Compass	1.8V	0x0E	0x1C, 0x1D	1MHz	Sensor Flex

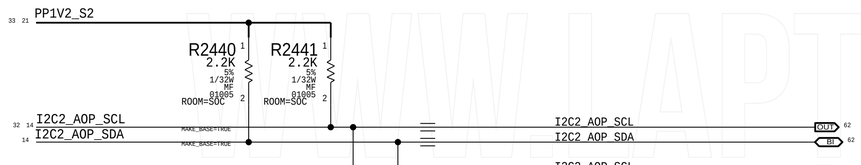
AOP I2C1



MASTER	AOP	NUMBER	I2C1	DIAGS NUMBER	6	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Eiger	1.2V	0x76	0xEC, 0xED	1MHz	Dock
Arc EEPROM	1.2V	0x50	0xA0, 0xA1	1MHz	Arc Flex
Jarvis	1.2V	0x0F	0x1E, 0x1F	1MHz	MLB

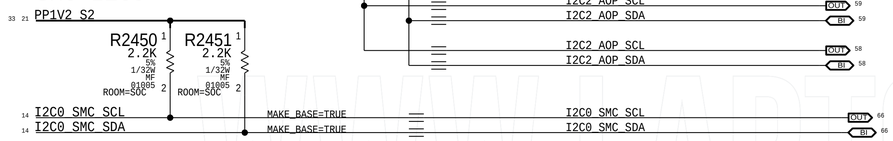
AOP I2C2



MASTER	AOP	NUMBER	I2C2	DIAGS NUMBER	7	SPEED	1MHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Sakonnet	1.2V	0x08	0x10, 0x11	1MHz	MLB
Codec	1.2V	0x4A	0x94, 0x95	1MHz	MLB
Arc Amp	1.2V	0x42	0x84, 0x85	1MHz	MLB
Bot Spk Amp	1.2V	0x40	0x80, 0x81	1MHz	MLB

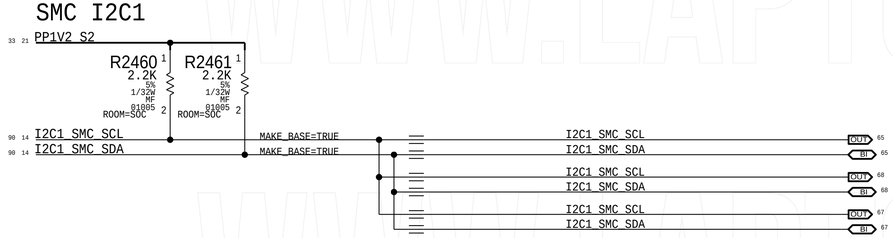
SMC I2C0



MASTER	SMC	NUMBER	I2C0	DIAGS NUMBER	8	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
CCG2B	1.2V	0x12	0x24, 0x25	1MHz	MLB

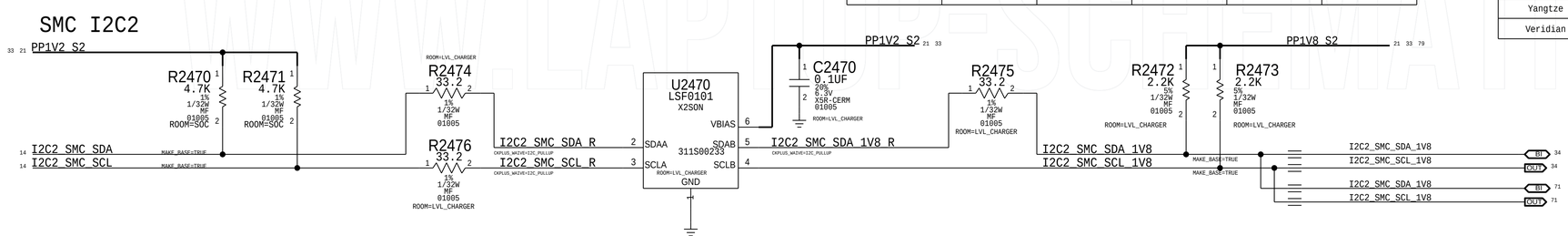
SMC I2C1



MASTER	SMC	NUMBER	I2C1	DIAGS NUMBER	9	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Kraken	1.2V	0x1A	0x34, 0x35	1MHz	MLB
Parrot	1.2V	0x21	0x42, 0x43	1MHz	MLB
Gecko2	1.2V	0x52	0xA4, 0xA5	1MHz	MLB

SMC I2C2



MASTER	SMC	NUMBER	I2C2	DIAGS NUMBER	10	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Yangtze	1.8V	0x71	0xE2, 0xE3	400kHz	MLB
Veridian	1.8V	0x0B	0x16, 0x17	400kHz	Battery Flex

SYNCING: D52, D53, D54

PAGE TITLE	SOC: Aliases: I2C AOP/SMC
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AOP GPIOs

* All AOP GPIOs tie into SCM block

SPMI0	SPI	AOP_FUNC0
SPMI0	SPI	AOP_FUNC1
SPMI0	SPI	AOP_FUNC2
SPMI0	SPI	AOP_FUNC3
SPMI1	SPI	AOP_FUNC4
SPMI1	SPI	AOP_FUNC5
SPMI1	SPI	AOP_FUNC6
SPMI1	SPI	AOP_FUNC7
	SPI	AOP_FUNC8
	SPI	AOP_FUNC9
	SPI	AOP_FUNC10
	SPI	AOP_FUNC11
I2C0	SPI	AOP_FUNC12
I2C0	SPI	AOP_FUNC13
I2C0	SPI	AOP_FUNC14
I2C1, I2C0	SPI	AOP_FUNC15
I2C1	I2C0	AOP_FUNC16
I2C1	I2C0	AOP_FUNC17
I2C1	I2C0	AOP_FUNC18
	I2C1	AOP_FUNC19
	I2C1	AOP_FUNC20
	I2C1	AOP_FUNC21
	I2C1	AOP_FUNC22

14	GPIO_SCM_AOP_FROM_IMU_DATARDY	=	GPIO_SCM_AOP_FROM_IMU_DATARDY	IN	96
14	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	=	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	OUT	96
14	GPIO_AOP_FROM_PEARL_B2B_DETECT	=	GPIO_AOP_FROM_PEARL_B2B_DETECT	IN	78
14	NC_DEV_AOP_FUNC3	=	NC_DEV_AOP_FUNC3		24
14	GPIO_SCM_AOP_FROM_R1_INT	=	GPIO_SCM_AOP_FROM_R1_INT	IN	98
14	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	=	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	OUT	98
14	GPIO_AOP_TO_R1_TIME_SYNC_L	=	GPIO_AOP_TO_R1_TIME_SYNC_L	OUT	98
14	GPIO_AOP_TO_CODEC_RESET_L	=	GPIO_AOP_TO_CODEC_RESET_L	OUT	58 89
14	GPIO_AOP_TO_BB_FORCE_PWM	=	GPIO_AOP_TO_BB_FORCE_PWM	OUT	93
14	GPIO_AOP_FROM_IRCAM_B2B_DETECT	=	GPIO_AOP_FROM_IRCAM_B2B_DETECT	IN	77
14	GPIO_SCM_AOP_TO_R1_SPI_CS_L	=	GPIO_SCM_AOP_TO_R1_SPI_CS_L	OUT	98
14	NC_AOP_FUNC11	=	NC_AOP_FUNC11		23
14	GPIO_AOP_TO_ALS_COEX	=	GPIO_AOP_TO_ALS_COEX	OUT	79
14	GPIO_AOP_TO_NFC_IRONMAN_EN	=	GPIO_AOP_TO_NFC_IRONMAN_EN	OUT	99
14	GPIO_AOP_FROM_TOUCH_CTS	=	GPIO_AOP_FROM_TOUCH_CTS	IN	24 83
14	GPIO_SCM_AOP_BI_PROX_INT_L	=	GPIO_SCM_AOP_BI_PROX_INT_L	IN	70
14	GPIO_SCM_AOP_FROM_ALS_INT_L	=	GPIO_SCM_AOP_FROM_ALS_INT_L	IN	79
14	GPIO_SCM_AOP_FROM_EIGER_INT_L	=	GPIO_SCM_AOP_FROM_EIGER_INT_L	IN	81
14	GPIO_SCM_AOP_FROM_COMPASS_INT	=	GPIO_SCM_AOP_FROM_COMPASS_INT	IN	70
14	GPIO_SCM_AOP_FROM_JARVIS_INT	=	GPIO_SCM_AOP_FROM_JARVIS_INT	IN	89 95
14	GPIO_AOP_FROM_TOUCH_INT_L	=	GPIO_AOP_FROM_TOUCH_INT_L	IN	83
14	NC_AOP_FUNC21	=	NC_AOP_FUNC21		23
14	NC_DEV_AOP_FUNC22	=	NC_DEV_AOP_FUNC22		24

AP GPIOs

AP_GPIO0	13 GPIO_BOARD_REV3	=	GPIO_BOARD_REV3	IN	7
AP_GPIO1	13 GPIO_BOARD_REV2	=	GPIO_BOARD_REV2	IN	7
AP_GPIO2	13 GPIO_BOARD_REV1	=	GPIO_BOARD_REV1	IN	7
AP_GPIO3	13 GPIO_BOARD_REV0	=	GPIO_BOARD_REV0	IN	7
AP_GPIO4	13 GPIO_AP_CANARY1	=	GPIO_AP_CANARY1	IN	97
AP_GPIO5	13 GPIO_AP_CANARY2	=	GPIO_AP_CANARY2	IN	95 97
AP_GPIO6	13 GPIO_AP_BI_CCG2B_SWDIO	=	GPIO_AP_BI_CCG2B_SWDIO	BI	66 89
AP_GPIO7	13 GPIO_AP_TO_CCG2B_SWCLK	=	GPIO_AP_TO_CCG2B_SWCLK	OUT	66 89
AP_GPIO8	13 GPIO_AP_FROM_DISPLAY_PANEL_ID	=	GPIO_AP_FROM_DISPLAY_PANEL_ID	IN	82
AP_GPIO9	13 GPIO_AP_FROM_WLAN_TIME_SYNC	=	GPIO_AP_FROM_WLAN_TIME_SYNC	IN	93
AP_GPIO10	13 GPIO_AP_TO_BB_PEAK_PWR_IND	=	GPIO_AP_TO_BB_PEAK_PWR_IND	OUT	93
AP_GPIO11	13 GPIO_AP_TO_BB_COREDUMP	=	GPIO_AP_TO_BB_COREDUMP	OUT	95
AP_GPIO12	13 GPIO_AP_FROM_BB_RESET_DETECT_L	=	GPIO_AP_FROM_BB_RESET_DETECT_L	IN	93
AP_GPIO13	13 GPIO_AP_FROM_CODEC_INT_L	=	GPIO_AP_FROM_CODEC_INT_L	IN	58 89
AP_GPIO14	13 NC_AP_GPIO14	=	NC_AP_GPIO14		23
AP_GPIO15	13 GPIO_AP_TO_SPKRAMP_TOP_RESET_L	=	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	OUT	60
AP_GPIO16	13 GPIO_AP_FROM_BT_AUDIO_SYNC	=	GPIO_AP_FROM_BT_AUDIO_SYNC	IN	93
AP_GPIO17	13 GPIO_AP_TO_AMUX_PMU_SYNC	=	GPIO_AP_TO_AMUX_PMU_SYNC	OUT	24
AP_GPIO18	13 NC_DEV_AP_GPIO18	=	NC_DEV_AP_GPIO18		24
AP_GPIO19	13 NC_DEV_AP_GPIO19	=	NC_DEV_AP_GPIO19		24
AP_GPIO20	13 NC_DEV_AP_GPIO20	=	NC_DEV_AP_GPIO20		24
AP_GPIO21	13 NC_DEV_AP_GPIO21	=	NC_DEV_AP_GPIO21		24
AP_GPIO22	13 NC_DEV_AP_GPIO22	=	NC_DEV_AP_GPIO22		24
AP_GPIO23	13 NC_DEV_AP_GPIO23	=	NC_DEV_AP_GPIO23		24
AP_GPIO24	13 NC_DEV_AP_GPIO24	=	NC_DEV_AP_GPIO24		24
AP_GPIO25	13 GPIO_AP_TO_BB_TIME_MARK	=	GPIO_AP_TO_BB_TIME_MARK	OUT	93
AP_GPIO26	13 NC_DEV_AP_GPIO26	=	NC_DEV_AP_GPIO26		24

Great Dane

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SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: Aliases: GPIOs

DRAWING NUMBER: 051-05215 | SIZE: D

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Misc. SoC Aliases

NAND + USB & MISC

8 PP1V2_IO
8 PP1V2_IO
→ PP1V2_IO (MAKE_BASE=TRUE) 23 29 33

87 8 IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU (MAKE_BASE=TRUE)
→ IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 30
→ IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 65

8 NC_DEV_AP_TMR32_PWM0 → NC_DEV_AP_TMR32_PWM0 (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_AP_TMR32_PWM1 → NC_DEV_AP_TMR32_PWM1 (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_AP_TMR32_PWM2 → NC_DEV_AP_TMR32_PWM2 (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_PAD_MTR_VREF_P → NC_DEV_PAD_MTR_VREF_P (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_PAD_MTR_VREF_N → NC_DEV_PAD_MTR_VREF_N (MAKE_BASE=TRUE, NO_TEST=1)

8 PP1V2_IO
→ PP1V2_IO (MAKE_BASE=TRUE) 23 29 33

87 30 IO_PMU_TO_SYSTEM_RESET_L (MAKE_BASE=TRUE)
→ IO_PMU_TO_SYSTEM_RESET_L 8
→ IO_PMU_TO_SYSTEM_RESET_L 14
→ IO_PMU_TO_SYSTEM_RESET_L 14

NC_DEV_SOC_THROTTLE_TRIGGER0 (MAKE_BASE=TRUE, NO_TEST=1) → NC_DEV_SOC_THROTTLE_TRIGGER0 8
NC_DEV_PMU_CPU_TRIGGER0 (MAKE_BASE=TRUE, NO_TEST=1) → NC_DEV_PMU_CPU_TRIGGER0 30

89 IO_AP_FROM_PMU_SW_SHDN_L (MAKE_BASE=TRUE)
→ IO_AP_FROM_PMU_SW_SHDN_L 8
→ IO_AP_FROM_PMU_SW_SHDN_L 30

89 IO_AP_FROM_PMU_PRE_UVLO_L (MAKE_BASE=TRUE)
→ IO_AP_FROM_PMU_PRE_UVLO_L 8
→ IO_AP_FROM_PMU_PRE_UVLO_L 30

NC_DEV_SOC_THROTTLE_TRIGGER3 (MAKE_BASE=TRUE, NO_TEST=1) → NC_DEV_SOC_THROTTLE_TRIGGER3 8
NC_DEV_PMU_GPU_TRIGGER0 (MAKE_BASE=TRUE, NO_TEST=1) → NC_DEV_PMU_GPU_TRIGGER0 30
NC_DEV_SOC_THROTTLE_TRIGGER4 (MAKE_BASE=TRUE, NO_TEST=1) → NC_DEV_SOC_THROTTLE_TRIGGER4 8
NC_DEV_PMU_GPU_TRIGGER1 (MAKE_BASE=TRUE, NO_TEST=1) → NC_DEV_PMU_GPU_TRIGGER1 30

89 8 IO_SOC_TO_PMU_SOCHOT_RESET_L (MAKE_BASE=TRUE) → IO_SOC_TO_PMU_SOCHOT_RESET_L 30
89 8 CLK_AP_TO_PMU_TST_CLKOUT (MAKE_BASE=TRUE) → CLK_AP_TO_PMU_TST_CLKOUT 30
8 AMUX_SOC_TO_PMU_AMUX_OUT (MAKE_BASE=TRUE) → AMUX_SOC_TO_PMU_AMUX_OUT 30

14 GND
8 GND
8 GND

89 14 IO_AON_TO_AP_XTAL_CFSB (MAKE_BASE=TRUE, CKPLUS_WAIVE=SINGLE_COMP_NET) → IO_AON_TO_AP_XTAL_CFSB 8

89 68 90_EUSB_DBG_PARROT_BI_AP_N (MAKE_BASE=TRUE) → 90_EUSB_DBG_PARROT_BI_AP_N 14
89 68 90_EUSB_DBG_PARROT_BI_AP_P (MAKE_BASE=TRUE) → 90_EUSB_DBG_PARROT_BI_AP_P 14

12 NC_SOC_S_GPIO1 → NC_SOC_S_GPIO1 (MAKE_BASE=TRUE, NO_TEST=1)

VSS CORNER BALLS

19 GND
19 GND
19 GND
19 GND

UART: KRAKEN

65 UART0_AP_TO_KRAKEN_DEBUG_TXD → UART0_AP_TO_KRAKEN_DEBUG_TXD (MAKE_BASE=TRUE) 12 89
65 UART0_AP_FROM_KRAKEN_DEBUG_RXD → UART0_AP_FROM_KRAKEN_DEBUG_RXD (MAKE_BASE=TRUE) 12 89
65 UART4_AP_TO_KRAKEN_ACC_TXD → UART4_AP_TO_KRAKEN_ACC_TXD (MAKE_BASE=TRUE) 12 89
65 UART4_AP_FROM_KRAKEN_ACC_RXD → UART4_AP_FROM_KRAKEN_ACC_RXD (MAKE_BASE=TRUE) 12 89

DISPLAY

11 NC_SOC_DWI_CLK → NC_SOC_DWI_CLK (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DWI_DATA → NC_SOC_DWI_DATA (MAKE_BASE=TRUE, NO_TEST=1)

11 NC_TOUCH_BSYNC1_DISP → NC_TOUCH_BSYNC1_DISP
11 NC_EDP_HPD_DISP → NC_EDP_HPD_DISP (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DISP_I2C_SCL → NC_SOC_DISP_I2C_SCL (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DISP_I2C_SDA → NC_SOC_DISP_I2C_SDA (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DISP_POL → NC_SOC_DISP_POL (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DISP_AGPIO → NC_SOC_DISP_AGPIO (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DISP_EXT_HPD → NC_SOC_DISP_EXT_HPD (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_SOC_DISP_TOUCH_EB → NC_SOC_DISP_TOUCH_EB (MAKE_BASE=TRUE, NO_TEST=1)

11 NC_DEV_LPDP_AP_TX0P → NC_DEV_LPDP_AP_TX0P
11 NC_DEV_LPDP_AP_TX0N → NC_DEV_LPDP_AP_TX0N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_TX1P → NC_DEV_LPDP_AP_TX1P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_TX1N → NC_DEV_LPDP_AP_TX1N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_TX2P → NC_DEV_LPDP_AP_TX2P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_TX2N → NC_DEV_LPDP_AP_TX2N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_TX3P → NC_DEV_LPDP_AP_TX3P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_TX3N → NC_DEV_LPDP_AP_TX3N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_AUXP → NC_DEV_LPDP_AP_AUXP (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_AUXN → NC_DEV_LPDP_AP_AUXN (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_RCALP → NC_DEV_LPDP_AP_RCALP (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_LPDP_AP_RCALN → NC_DEV_LPDP_AP_RCALN (MAKE_BASE=TRUE, NO_TEST=1)

11 NC_LPDP_EXT_AP_TX0_P → NC_LPDP_EXT_AP_TX0_P
11 NC_LPDP_EXT_AP_TX0_N → NC_LPDP_EXT_AP_TX0_N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_TX1_P → NC_LPDP_EXT_AP_TX1_P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_TX1_N → NC_LPDP_EXT_AP_TX1_N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_TX2_P → NC_LPDP_EXT_AP_TX2_P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_TX2_N → NC_LPDP_EXT_AP_TX2_N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_TX3_P → NC_LPDP_EXT_AP_TX3_P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_TX3_N → NC_LPDP_EXT_AP_TX3_N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_AUX_P → NC_LPDP_EXT_AP_AUX_P
11 NC_LPDP_EXT_AP_AUX_N → NC_LPDP_EXT_AP_AUX_N (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_EXT_AP_RCAL_P → NC_LPDP_EXT_AP_RCAL_P
11 NC_LPDP_EXT_AP_RCAL_N → NC_LPDP_EXT_AP_RCAL_N (MAKE_BASE=TRUE, NO_TEST=1)

ISP

10 NC_ISP_GPIO_1 → NC_ISP_GPIO_1 (MAKE_BASE=TRUE, NO_TEST=1)
10 NC_ISP_GPIO_2 → NC_ISP_GPIO_2 (MAKE_BASE=TRUE, NO_TEST=1)
10 NC_SENSOR2_CLK_AP → NC_SENSOR2_CLK_AP (MAKE_BASE=TRUE, NO_TEST=1)
10 NC_SENSOR3_CLK_AP → NC_SENSOR3_CLK_AP (MAKE_BASE=TRUE, NO_TEST=1)

SPI (AP)

12 SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2 → SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2 (MAKE_BASE=TRUE) 7 25 89
12 SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1 → SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1 (MAKE_BASE=TRUE) 7 25
12 SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 → SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 (MAKE_BASE=TRUE) 7 25

12 SPI3_AP_FROM_CODEC_MISO → SPI3_AP_FROM_CODEC_MISO (MAKE_BASE=TRUE) 58 89
12 SPI3_AP_TO_CODEC_MOSI → SPI3_AP_TO_CODEC_MOSI (MAKE_BASE=TRUE) 58 89
12 SPI3_AP_TO_CODEC_SCLK → SPI3_AP_TO_CODEC_SCLK (MAKE_BASE=TRUE) 58
12 SPI3_AP_TO_CODEC_CS_L → SPI3_AP_TO_CODEC_CS_L (MAKE_BASE=TRUE) 58 89

SOC: PCIe

9 NC_DEV_PCIE_GP0_AP_CLKREQ_L → NC_DEV_PCIE_GP0_AP_CLKREQ_L (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_REFCLK_P → NC_DEV_PCIE_GP0_AP_REFCLK_P (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_REFCLK_N → NC_DEV_PCIE_GP0_AP_REFCLK_N (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_RX_P → NC_DEV_PCIE_GP0_AP_RX_P (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_RX_N → NC_DEV_PCIE_GP0_AP_RX_N (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_TX_P → NC_DEV_PCIE_GP0_AP_TX_P (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_TX_N → NC_DEV_PCIE_GP0_AP_TX_N (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_DEV_PCIE_GP0_AP_RESET_L → NC_DEV_PCIE_GP0_AP_RESET_L (MAKE_BASE=TRUE, NO_TEST=1)

SOC: Serial

12 NC_UART1_AP_CTS_L → NC_UART1_AP_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART1_AP_RTS_L → NC_UART1_AP_RTS_L (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART1_AP_RXD → NC_UART1_AP_RXD (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART1_AP_TXD → NC_UART1_AP_TXD (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART2_AP_CTS_L → NC_UART2_AP_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART2_AP_RTS_L → NC_UART2_AP_RTS_L (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART2_AP_RXD → NC_UART2_AP_RXD (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART2_AP_TXD → NC_UART2_AP_TXD (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART3_AP_CTS_L → NC_UART3_AP_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART3_AP_RXD → NC_UART3_AP_RXD (MAKE_BASE=TRUE, NO_TEST=1)

12 NC_I2S1_AP_MCLK → NC_I2S1_AP_MCLK
22 NC_AP_GPIO14 → NC_AP_GPIO14 (MAKE_BASE=TRUE, NO_TEST=1)

12 NC_I2S2_AP_MCLK → NC_I2S2_AP_MCLK (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_SSPI0_MISO_AP → NC_SSPI0_MISO_AP (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_SSPI0_SCLK_AP → NC_SSPI0_SCLK_AP (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_SSPI0_MOSI_AP → NC_SSPI0_MOSI_AP (MAKE_BASE=TRUE, NO_TEST=1)
12 NC_UART6_AP_RXD_1V8 → NC_UART6_AP_RXD_1V8 (MAKE_BASE=TRUE, NO_TEST=1)

SOC: AOP

14 GPIO_AOP_TO_WLAN_CONTEXT_A → GPIO_AOP_TO_WLAN_CONTEXT_A (MAKE_BASE=TRUE) 93
14 GPIO_AOP_TO_WLAN_CONTEXT_B → GPIO_AOP_TO_WLAN_CONTEXT_B (MAKE_BASE=TRUE) 93
22 NC_AOP_FUNC11 → NC_AOP_FUNC11 (MAKE_BASE=TRUE, NO_TEST=1)
22 NC_AOP_FUNC21 → NC_AOP_FUNC21 (MAKE_BASE=TRUE, NO_TEST=1)

NUB

14 NC_NUB_GPIO5 → NC_NUB_GPIO5 (MAKE_BASE=TRUE)

14 GND
14 NC_DEV_JTAG_TDI → NC_DEV_JTAG_TDI (MAKE_BASE=TRUE, NO_TEST=1)
14 NC_DEV_JTAG_TDO → NC_DEV_JTAG_TDO (MAKE_BASE=TRUE, NO_TEST=1)
14 NC_DEV_JTAG_TRST_L → NC_DEV_JTAG_TRST_L (MAKE_BASE=TRUE, NO_TEST=1)
14 PP1V2_S2 → PP1V2_S2 (MAKE_BASE=TRUE) 29 33 67 77 78 82 83 96 97 99

89 14 SWD_NUB_TO_PMU_TOUCH_SWCLK (MAKE_BASE=TRUE) → SWD_NUB_TO_PMU_TOUCH_SWCLK 30

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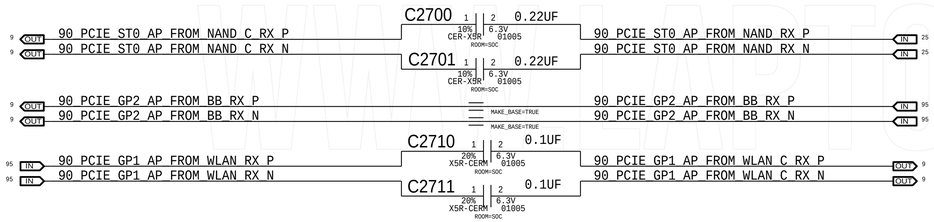

DISPLAY

11 90 MIPI AP TO DISPLAY CLK P — 90 MIPI AP TO DISPLAY CLK P 82
11 90 MIPI AP TO DISPLAY CLK N — 90 MIPI AP TO DISPLAY CLK N 82
MAKE_BASE=TRUE
MAKE_BASE=TRUE

11 90 MIPI AP TO DISPLAY D0 P — 90 MIPI AP TO DISPLAY D0 P 82
11 90 MIPI AP TO DISPLAY D0 N — 90 MIPI AP TO DISPLAY D0 N 82
MAKE_BASE=TRUE
MAKE_BASE=TRUE

11 90 MIPI AP TO DISPLAY D1 P — 90 MIPI AP TO DISPLAY D1 P 82
11 90 MIPI AP TO DISPLAY D1 N — 90 MIPI AP TO DISPLAY D1 N 82
MAKE_BASE=TRUE
MAKE_BASE=TRUE

11 NC MIPI AP TO DISPLAY D2 P — NC MIPI AP TO DISPLAY D2 P
11 NC MIPI AP TO DISPLAY D2 N — NC MIPI AP TO DISPLAY D2 N
NO_TEST=1
NO_TEST=1
MAKE_BASE=TRUE
MAKE_BASE=TRUE

11 90 MIPI AP TO DISPLAY D2 P — 90 MIPI AP TO DISPLAY D2 P 82
11 90 MIPI AP TO DISPLAY D2 N — 90 MIPI AP TO DISPLAY D2 N 82
MAKE_BASE=TRUE
MAKE_BASE=TRUE

LPDP

ISP: LPDP Lanes

10 90 LPDP ISP FROM FCAM RX D1 N — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM FCAM RX D1 N 76
10 90 LPDP ISP FROM FCAM RX D1 P — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM FCAM RX D1 P 76

10 90 LPDP ISP FROM FCAM RX D0 N — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM FCAM RX D0 N 76
10 90 LPDP ISP FROM FCAM RX D0 P — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM FCAM RX D0 P 76

10 90 LPDP ISP FROM WIDE RX D2 P — MAKE_BASE=TRUE — 90 LPDP ISP FROM WIDE RX D2 P 74
10 90 LPDP ISP FROM WIDE RX D2 N — MAKE_BASE=TRUE — 90 LPDP ISP FROM WIDE RX D2 N 74

10 90 LPDP ISP FROM WIDE RX D1 N — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM WIDE RX D1 N 74
10 90 LPDP ISP FROM WIDE RX D1 P — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM WIDE RX D1 P 74

10 90 LPDP ISP FROM WIDE RX D0 N — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM WIDE RX D0 N 74
10 90 LPDP ISP FROM WIDE RX D0 P — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM WIDE RX D0 P 74

10 90 LPDP ISP FROM SUPERFLEX CAM2 RX D2 N — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM SUPERFLEX CAM2 RX D2 N 74
10 90 LPDP ISP FROM SUPERFLEX CAM2 RX D2 P — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM SUPERFLEX CAM2 RX D2 P 74

10 90 LPDP ISP FROM SUPERFLEX CAM2 RX D0 P — MAKE_BASE=TRUE — 90 LPDP ISP FROM SUPERFLEX CAM2 RX D0 P 74
10 90 LPDP ISP FROM SUPERFLEX CAM2 RX D0 N — MAKE_BASE=TRUE — 90 LPDP ISP FROM SUPERFLEX CAM2 RX D0 N 74

10 90 LPDP ISP FROM SUPERFLEX CAM2 RX D1 N — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM SUPERFLEX CAM2 RX D1 N 74
10 90 LPDP ISP FROM SUPERFLEX CAM2 RX D1 P — CKPLUS_WAIVE=DIFFPAIR_RADTERM — MAKE_BASE=TRUE — 90 LPDP ISP FROM SUPERFLEX CAM2 RX D1 P 74

10 90 LPDP ISP FROM JASPER RX D0 P — MAKE_BASE=TRUE — 90 LPDP ISP FROM JASPER RX D0 P 75
10 90 LPDP ISP FROM JASPER RX D0 N — MAKE_BASE=TRUE — 90 LPDP ISP FROM JASPER RX D0 N 75

10 90 LPDP ISP FROM SINGLEFLEX CAM RX D0 P — MAKE_BASE=TRUE — 90 LPDP ISP FROM SINGLEFLEX CAM RX D0 P 73
10 90 LPDP ISP FROM SINGLEFLEX CAM RX D0 N — MAKE_BASE=TRUE — 90 LPDP ISP FROM SINGLEFLEX CAM RX D0 N 73

10 90 LPDP ISP FROM SINGLEFLEX CAM RX D1 P — MAKE_BASE=TRUE — 90 LPDP ISP FROM SINGLEFLEX CAM RX D1 P 73
10 90 LPDP ISP FROM SINGLEFLEX CAM RX D1 N — MAKE_BASE=TRUE — 90 LPDP ISP FROM SINGLEFLEX CAM RX D1 N 73

10 90 LPDP ISP FROM SINGLEFLEX CAM RX D2 P — MAKE_BASE=TRUE — 90 LPDP ISP FROM SINGLEFLEX CAM RX D2 P 73
10 90 LPDP ISP FROM SINGLEFLEX CAM RX D2 N — MAKE_BASE=TRUE — 90 LPDP ISP FROM SINGLEFLEX CAM RX D2 N 73

ISP: LPDP Aux

10 NC LPDP ISP AUX RX D0P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D0P
10 NC LPDP_ISP_AUX_RX_D1P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D1P
10 LPDP ISP BI SUPERFLEX CAM2 AUX RX D2P — MAKE_BASE=TRUE — LPDP ISP BI SUPERFLEX CAM2 AUX RX D2P 74
10 NC_LPDP_ISP_AUX_RX_D3P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D3P
10 NC_LPDP_ISP_AUX_RX_D4P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D4P
10 LPDP ISP BI SINGLEFLEX CAM AUX RX D5P — MAKE_BASE=TRUE — LPDP ISP BI SINGLEFLEX CAM AUX RX D5P 73
10 NC_LPDP_ISP_AUX_RX_D6P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D6P
10 NC_LPDP_ISP_AUX_RX_D7P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D7P
10 NC_LPDP_ISP_AUX_RX_D8P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D8P
10 NC LPDP ISP AUX RX D9P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D9P
10 NC_LPDP_ISP_AUX_RX_D10P — MAKE_BASE=TRUE NO_TEST=1 — NC LPDP ISP AUX RX D10P
10 NC_LPDP_ISP_AUX_RX_D11P — MAKE_BASE=TRUE — NC LPDP ISP AUX RX D11P

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12 NC AP SPMI2 SCLK — NC AP SPMI2 SCLK
12 NC AP SPMI2 SDATA — NC AP SPMI2 SDATA
MAKE_BASE=TRUE NO_TEST=1
MAKE_BASE=TRUE NO_TEST=1

12 NC I2C0 AP SCL — NC I2C0 AP SCL
12 NC I2C0 AP SDA — NC I2C0 AP SDA
MAKE_BASE=TRUE NO_TEST=1
MAKE_BASE=TRUE NO_TEST=1

12 NC I2C1 AP SCL — NC I2C1 AP SCL
12 NC I2C1 AP SDA — NC I2C1 AP SDA
MAKE_BASE=TRUE NO_TEST=1
MAKE_BASE=TRUE NO_TEST=1

22 NC DEV AOP FUNC22 — NC DEV AOP FUNC22
MAKE_BASE=TRUE

22 NC DEV AOP FUNC3 — NC DEV AOP FUNC3
MAKE_BASE=TRUE NO_TEST=1

83 24 22 GPIO AOP FROM TOUCH CTS — GPIO AOP FROM TOUCH CTS 22 24 83
MAKE_BASE=TRUE

22 GPIO AP TO AMUX PMU SYNC — GPIO_AP_TO_AMUX_PMU_SYNC 30 89
MAKE_BASE=TRUE

22 NC_DEV_AP_GPIO18 — NC_DEV_AP_GPIO18
22 NC_DEV_AP_GPIO19 — NC_DEV AP GPIO19
MAKE_BASE=TRUE

22 NC_DEV_AP_GPIO20 — NC_DEV AP GPIO20
MAKE_BASE=TRUE

22 NC_DEV_AP_GPIO21 — NC_DEV AP GPIO21
22 NC_DEV_AP_GPIO22 — NC_DEV AP GPIO22
MAKE_BASE=TRUE NO_TEST=1

22 NC_DEV_AP_GPIO23 — NC_DEV AP GPIO23
MAKE_BASE=TRUE NO_TEST=1

22 NC_DEV_AP_GPIO24 — NC_DEV AP GPIO24
MAKE_BASE=TRUE NO_TEST=1

22 NC_DEV_AP_GPIO26 — NC_DEV AP GPIO26
MAKE_BASE=TRUE NO_TEST=1

SPI (AP)

12 SPI1 AP FROM TOUCH MISO 1V8 — SPI1 AP FROM TOUCH MISO 1V8 83
12 SPI1 AP TO TOUCH MOSI 1V8 — SPI1 AP TO TOUCH MOSI 1V8 83
MAKE_BASE=TRUE
12 SPI1 AP TO TOUCH SCLK 1V8 — SPI1 AP TO TOUCH SCLK 1V8 83
MAKE_BASE=TRUE
12 SPI1 AP TO TOUCH CS L 1V8 — SPI1 AP TO TOUCH CS L 1V8 83
MAKE_BASE=TRUE
MAKE_BASE=TRUE

12 NC SPI2 MISO AP — NC SPI2 MISO AP
12 NC SPI2 MOSI AP — NC SPI2 MOSI AP
MAKE_BASE=TRUE NO_TEST=1
12 NC SPI2 SCLK AP — NC SPI2 SCLK AP
MAKE_BASE=TRUE NO_TEST=1
12 NC SPI2 SCLK AP
MAKE_BASE=TRUE
12 NC SPI2 CS L AP — NC SPI2 CS L AP
NO_TEST=1
MAKE_BASE=TRUE

Ada 24MHz clock (not used for DITO)

14 NC CLK NUB TO TOUCH 24M — NC CLK NUB TO TOUCH 24M
14 NC CLK NUB TO TOUCH 24M
NO_TEST=1
MAKE_BASE=TRUE

Hacky NO_TEST fix

51 NC_CAM_PMU2_BUCK0 — NC_CAM_PMU2_BUCK0 51
NO_TEST=1
MAKE_BASE=TRUE

Extra Canary

12 GPIO_AP_CANARY6 — GPIO_AP_CANARY6 93 97
MAKE_BASE=TRUE
12 GPIO_AP_CANARY5 — GPIO_AP_CANARY5 93 97
MAKE_BASE=TRUE
11 GPIO_AP_CANARY3 — GPIO_AP_CANARY3 93 97
MAKE_BASE=TRUE
14 GPIO_AOP_CANARY7 — GPIO_AOP_CANARY7 94 97
MAKE_BASE=TRUE
11 GPIO_AP_CANARY4 — GPIO_AP_CANARY4 95 97
MAKE_BASE=TRUE

SYNCING: D52, D53, D54

PAGE TITLE
SOC: Aliases: FF-Specific

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S5E NAND

I_VCC = 1150mA MAX (1us PEAK POWER)
PP2V625_NAND

C2913 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2916 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2919 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2921 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2949 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2950 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2951 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2952 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2953 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2954 330PF 10% 16V CER-X7R 01005 ROOM=NAND

C2936 220PF 5% 25V C0G 01005 ROOM=NAND
C2937 220PF 5% 25V C0G 01005 ROOM=NAND
C2934 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2938 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2935 22PF 5% 16V C0G 01005 ROOM=NAND
C2939 22PF 5% 16V C0G 01005 ROOM=NAND

D3 E12 G4 L12 R2 → VCC

I_VDDIO1 (@ 1.2V) = 72mA MAX
PP1V2_IO

C2941 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2924 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2926 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2910 0.1UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2911 220PF 5% 25V C0G 01005 ROOM=NAND
C2955 220PF 5% 25V C0G 01005 ROOM=NAND

J2 K9 T5 → VDDIO_1

FL2925 10-OHM-1.1A 01005 ROOM=NAND 155S0876

C2956 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2957 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2958 22PF 5% 16V C0G 01005 ROOM=NAND
C2925 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

PP_NAND_VDDIO1_F VOLTAGE=1.8 → J6 PCIE_AVDD_H
PP_NAND_VDDIO1_R VOLTAGE=1.8 → L2 AVDD1X_PLL

R2963 2.0 5% 1/32W MF 01005 ROOM=NAND

C2963 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

I_VDDIO2 (@ 1.2V) = 384mA MAX
PP1V2_IO

C2931 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2929 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2943 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2945 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2947 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2959 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2960 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2912 220PF 5% 25V C0G 01005 ROOM=NAND
C2915 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2917 22PF 5% 16V C0G 01005 ROOM=NAND

E10 E2 N2 P9 → VDDIO_2 (VCCQ_ANI)

G6 G8 L6 L8 R6 R8 → VDD (VDD)

C2961 220PF 5% 25V C0G 01005 ROOM=NAND PACK_OPTION=D52,D53
C2918 47PF 5% 16V NP0-C0G 01005 ROOM=NAND PACK_OPTION=D52,D53
C2914 22PF 5% 16V C0G 01005 ROOM=NAND PACK_OPTION=D52,D53
C2962 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=D52

J8 M9 N6 N8 → PCIE_VDD

I_VDD = 820mA MAX
PP0V83_NAND

C2948 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2902 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2905 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND

FL2923 10-OHM-1.1A 01005 ROOM=NAND 155S0876

PP0V83_NAND_PLL VOLTAGE=0.83 → R4 VDD_PLL

C2923 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2900 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2901 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2922 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2927 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2940 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2942 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2944 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2946 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2907 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2903 220PF 5% 25V C0G 01005 ROOM=NAND
C2908 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2904 22PF 5% 16V C0G 01005 ROOM=NAND
C2909 330PF 10% 16V CER-X7R 01005 ROOM=NAND PACK_OPTION=D52,D53
C2906 220PF 5% 25V C0G 01005 ROOM=NAND PACK_OPTION=D52,D53

U2900
H23BFG8127AEQ-BC
LGA
SYM 2 OF 2
335S00436
ROOM=NAND
OMIT_TABLE

VCC
VDDIO_1
(VCCQ_IO)
VSS
PCIE_AVDD_H
AVDD1X_PLL
VDDIO_2
(VCCQ_ANI)
VDD
(VDD)
PCIE_VDD
VDD_PLL
VSS_R
VPP
VQPS

NC_DEV_NAND_VPP 26
GND 26
VQPS used for fuse programming, GND in system

NOTES:
INT PU = internal pull up to VDDIO_1
INT PD = internal pull down to VSS
Internal pulls are 40kOhm (min), 80kOhm (typ), 165kOhm (max)

U2900
H23BFG8127AEQ-BC
LGA
SYM 1 OF 2
335S00436
ROOM=NAND
OMIT_TABLE

CLK_AP_TO_NAND_24M ~ 24M / 630mV → M3 CLK_IN
IO_AP_TO_NAND_RESET_L 1.239V → L4 RESET*
GND → G10 TRST* (INT PD)
90_PCIE_ST0_AP_TO_NAND_REFCLK_P 100mV → K11 PCIE_REFCLK_P
90_PCIE_ST0_AP_TO_NAND_REFCLK_N 100mV → J12 PCIE_REFCLK_N
PCIE_ST0_AP_BI_NAND_CLKREQ_L 1.24V → P5 PCIE_CLKREQ*
90_PCIE_ST0_AP_TO_NAND_TX_P encendido → M11 PCIE_RX0_P
90_PCIE_ST0_AP_TO_NAND_TX_N Apagado → N12 PCIE_RX0_N
90_PCIE_ST0_AP_FROM_NAND_RX_P → R12 PCIE_TX0_P
90_PCIE_ST0_AP_FROM_NAND_RX_N → T11 PCIE_TX0_N
PCIE_ST0_AP_TO_NAND_PERST_L Sin Actividad → E8 EXT_NCE/PERST*
ANALOG_NAND_PCIE_RESREF Sin Actividad → H7 PCIE_RESREF
(for dev) C2920 10PF 5% 16V NP0/C0G 01005 ROOM=NAND; R2904 200 0.5% 1/32W TK 01005 ROOM=NAND
Keep ZQ trace DCR < 200mOhm
ANALOG_NAND_ZQ_0 Sin Actividad → C10 ZQ_0
ANALOG_NAND_ZQ_1 Sin Actividad → K3 ZQ_1
(for dev) R2900 300 1% 1/32W MF 01005-1 ROOM=NAND; R2901 300 1% 1/32W MF 01005-1 ROOM=NAND; OMIT_TABLE

(INT PU) EXT_D0/BOOT0 → B3 GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L Sin Activ. 32 89
(INT PD) EXT_D1/BOOT1 → C4 IO_AP_TO_NAND_FW_STRAP Sin 8 89
EXT_D2/BOOT2/SPINAND_SCLK/SPI_SCLK → B5 SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 IN 8 23
EXT_D3/SPINAND_MISO/SPI_MISO/SWD_UID → C6 SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2 Sin Activ. OUT 7 23 89
EXT_D4/SPI_CS → B7 GND 26
EXT_D5/SPINAND_MOSI/SPI_MOSI/SWD_UID1 → C8 SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1 1.23V IN 7 23
EXT_D6/BOOT3 → B9 GND 26
EXT_D7/SPF_N → B11 IO_PMU_TO_NAND_SYSTEM_ALIVE 1.23V IN 30 89
(INT PU) EXT_DQS/BCM_N → D11 NC_DEV_NAND_BCM_L NC 26
(INT PU) EXT_NRE/JTAG_TMS → D7 SWD_AP_BI_NAND_SWDIO Sin BI 8 89
(INT PU) EXT_NWE/JTAG_TCK → E6 SWD_AP_TO_MANY_SWCLK Sin IN 8 95 98
EXT_RNB/JTAG_TDO → E4 GND 26
(INT PU) EXT_CLE/JTAG_TDI → D5 NC_DEV_NAND_JTAG_TDI NC 26
(INT PD) EXT_ALE/JTAG_SEL → D9 GND 26
DROOP* → T3
WP* → G2 PP1V2_IO 1.023V 26
ANI0_VREF → G12 ANALOG_NAND_ANI0_VREF Sin 89
ANI1_VREF → J4 ANALOG_NAND_ANI1_VREF Sin 89

NAND Capacities

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00436	1	HYNIX,3Dv5,64Gb,Ultimate	U2900	CRITICAL	NAND:ULTIMATE
335S00437	1	HYNIX,3Dv5,128Gb,Supreme	U2900	CRITICAL	NAND:SUPREME
335S00438	1	HYNIX,3Dv5,256Gb,Extreme	U2900	CRITICAL	NAND:EXTREME
335S00439	1	HYNIX,3Dv5,512Gb,Max	U2900	CRITICAL	NAND:MAX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00449	335S00436	NAND:ULTIMATE	U2900	TOSHIBA,BiCS4,64Gb,Ultimate
335S00446	335S00437	NAND:SUPREME	U2900	SAMSUNG,3Dv5,128Gb,Supreme
335S00447	335S00438	NAND:EXTREME	U2900	SAMSUNG,3Dv5,256Gb,Extreme
335S00450	335S00438	NAND:EXTREME	U2900	TOSHIBA,BiCS4,256Gb,Extreme
335S00448	335S00439	NAND:MAX	U2900	SAMSUNG,3Dv5,512Gb,Max

SYNCING: D52, D53, D54

SUBSYSTEM SPECIFIC BOM TABLES

ZQ Resistor

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0784	1	RES,3000HM,1%,1/32W,01005	R2901	CRITICAL	S5E

Note: Dev Board adds an S4E option

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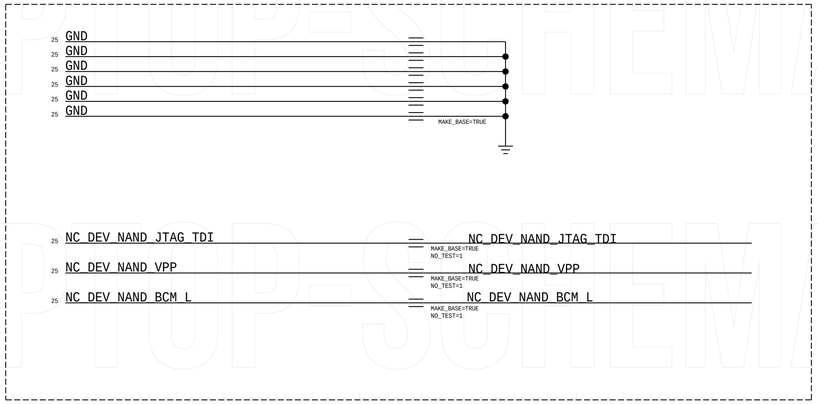
DEV BOARD COMPATIBILITY



VDDIO2

SYNCING: D52, D53, D54

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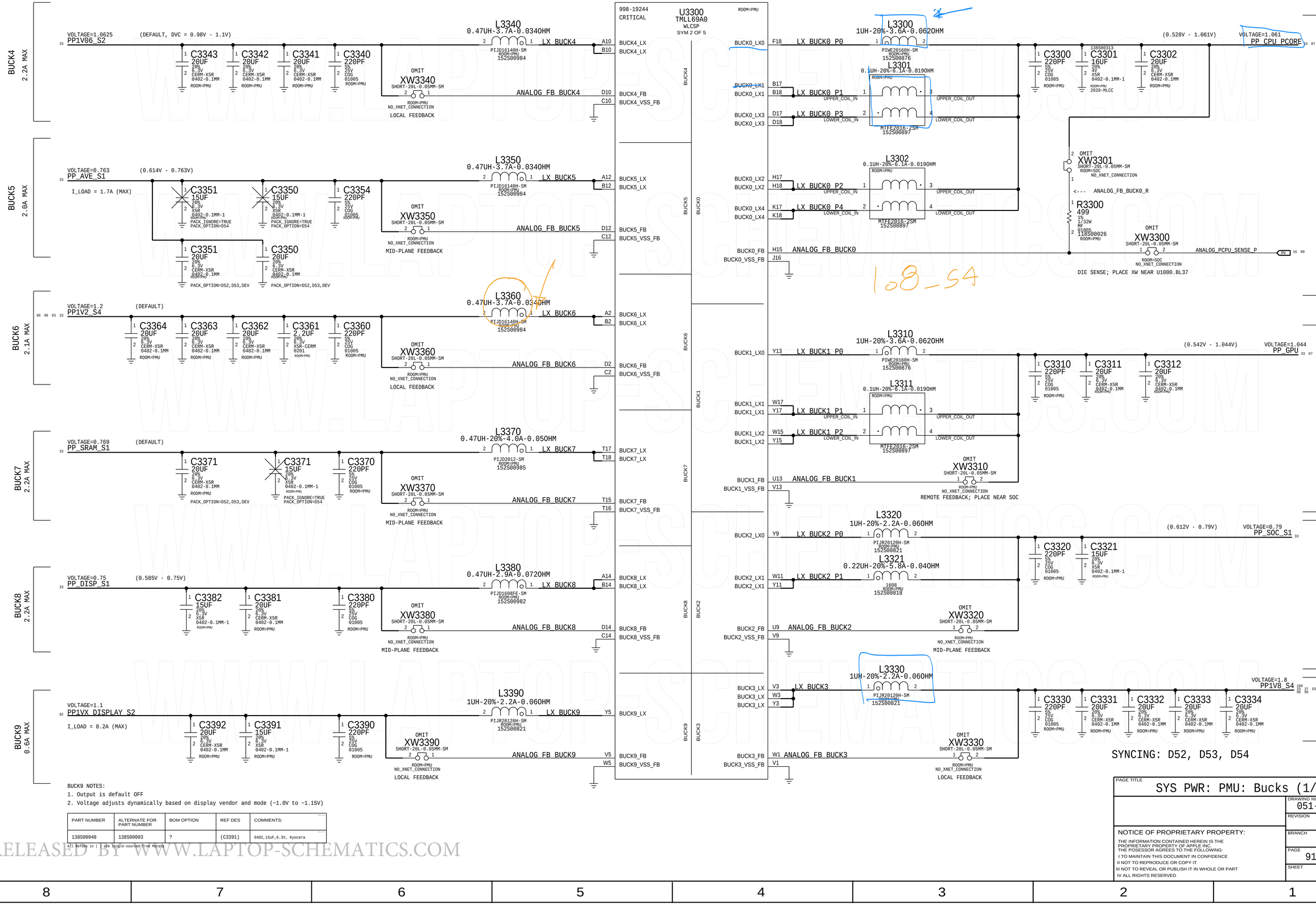

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C3391)	0402,15uF,6.3V, Kyocera

All Refdes in ( ) are Single-sourced from Murata

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PP_VDD_MAIN

PLACE IN VICINITY OF PMU FOR BULK CAP

C3404 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU (CRITICAL)
C3405 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU (CRITICAL)
C3406 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU (CRITICAL)
C3407 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU (CRITICAL)
C3408 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU (CRITICAL)

PLACE ON PMU CORNERS TO FILL 01005 RING AROUND PMU

C3480 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3481 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3482 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3483 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU

Buck0
C3490 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C3491 2.7UF 20% 6.3V X5R 0201 138S00325 ROOM=PMU 2020-MLCC

Buck1
C3492 2.7UF 20% 6.3V X5R 0201 138S00325 ROOM=PMU 2020-MLCC

Buck11
C3493 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

998-19244 CRITICAL
U3300 TML69A0 WLCSP SYM 3 OF 5 ROOM=PMU

C3450 0.22UF	A1	VDD_BUCK13_10_6_4
	B1	VDD_BUCK13_10_6_4
C3451 0.22UF	A3	VSS_BUCK13_6
	B3	VSS_BUCK13_6
C3452 0.22UF	A5	VDD_BUCK13_10_6_4
	B5	VDD_BUCK13_10_6_4
C3459 0.22UF	A7	VSS_BUCK10
	B7	VSS_BUCK10
C3453 0.22UF	A9	VDD_BUCK13_10_6_4
	B9	VDD_BUCK13_10_6_4
C3454 0.22UF	A11	VSS_BUCK5_4
	B11	VSS_BUCK5_4
C3455 0.22UF	A13	VDD_BUCK8_5
	B13	VDD_BUCK8_5
C3456 0.22UF	A15	VSS_BUCK8
	B15	VSS_BUCK8
	A16	VSS_BUCK0
	A17	VSS_BUCK0
	A18	VSS_BUCK0
C3457 0.22UF	C17	VDD_BUCK11_7_0
	C18	VDD_BUCK11_7_0
C3469 0.22UF	E17	VSS_BUCK0
	E18	VSS_BUCK0
C3458 0.22UF	G17	VDD_BUCK11_7_0
	G18	VDD_BUCK11_7_0
C3460 0.22UF	J17	VSS_BUCK0
	J18	VSS_BUCK0
C3470 0.22UF	L17	VDD_BUCK11_7_0
	L18	VDD_BUCK11_7_0
C3461 0.22UF	N17	VSS_BUCK11
	N18	VSS_BUCK11
C3462 0.22UF	R17	VDD_BUCK11_7_0
	R18	VDD_BUCK11_7_0
C3463 0.22UF	U17	VSS_BUCK7
	U18	VSS_BUCK7
	V18	VSS_BUCK1
	W18	VSS_BUCK1
	Y18	VSS_BUCK1
C3464 0.22UF	W16	VDD_BUCK12_2_1
	Y16	VDD_BUCK12_2_1
C3471 0.22UF	W14	VSS_BUCK1
	Y14	VSS_BUCK1
C3465 0.22UF	W12	VDD_BUCK12_2_1
	Y12	VDD_BUCK12_2_1
C3472 0.22UF	W10	VSS_BUCK2
	Y10	VSS_BUCK2
C3466 0.22UF	W8	VDD_BUCK12_2_1
	Y8	VDD_BUCK12_2_1
C3467 0.22UF	W6	VSS_BUCK12_9
	Y6	VSS_BUCK12_9
C3468 0.22UF	W4	VDD_BUCK9_3
	Y4	VDD_BUCK9_3
	V4	VDD_BUCK9_3
	V2	VSS_BUCK3
	W2	VSS_BUCK3
	Y1	VSS_BUCK3
	Y2	VSS_BUCK3

BUCK10 BUCK11 BUCK12 BUCK13

BUCK10_LX0 A8 LX_BUCK10_P0
BUCK10_LX1 A6 LX_BUCK10_P1 (B6)
BUCK10_FB D8 ANALOG_FB_BUCK10
BUCK10_VSS_FB C8

L3400 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU 152S00821
L3401 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
OMIT XW3400 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
MID-PLANE FEEDBACK

(0.765V - 1.099V) VOLTAGE=1.099 PP_CPU_SRAM 33
C3401 220PF 5% 25V C0G 01005 ROOM=PMU
C3402 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3403 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK10 4.2A MAX

BUCK11_LX0 M18 LX_BUCK11_P0
BUCK11_LX1 P17 (P18) LX_BUCK11_P1
BUCK11_FB M15 ANALOG_FB_BUCK11
BUCK11_VSS_FB M16

L3410 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU 152S00821
PACK_OPTION=D52,D53,DEV
L3411 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
OMIT XW3410 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
REMOTE FEEDBACK

(0.519V - 0.828V) VOLTAGE=0.828 PP_CPU_ECORE 28 33
C3410 220PF 5% 25V C0G 01005 ROOM=PMU
C3411 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3412 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D54
C3412 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D52,D53,DEV

L3410 1UH-20%-2A-0.069OHM 2012 ROOM=PMU 152S00819 PACK_IGNORE=TRUE PACK_OPTION=D54
28 LX_BUCK11_P0 — PP_CPU_ECORE 28 33

BUCK11 3.8A MAX

BUCK12_LX W7 (V7) LX_BUCK12
BUCK12_FB U7 ANALOG_FB_BUCK12
BUCK12_VSS_FB V7

L3420 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984
OMIT XW3420 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LOCAL FEEDBACK; PLACE NEAR U3300.N1

(DEFAULT) VOLTAGE=0.88 PP0V9_S1 33
C3420 220PF 5% 25V C0G 01005 ROOM=PMU
C3421 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3422 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3423 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK12 2.1A MAX

BUCK13_LX A4 LX_BUCK13
BUCK13_FB C4 ANALOG_FB_BUCK13
BUCK13_VSS_FB B4

L3430 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU 152S00982
OMIT XW3430 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
MID-PLANE FEEDBACK

(0.615V - 0.842V) VOLTAGE=0.842 PP_DCS_S1 33
C3432 220PF 5% 25V C0G 01005 ROOM=PMU
C3430 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3431 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK13 1.0A MAX

SYNCING: D52, D53, D54

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PMU:LDOs

SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	(C3515)	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	(C3515)	CAP,X5R,4UF,0201,0.55MM,KYOCERA

15uF 0402 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	[SEE BELOW]	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

(C3509,C3510,C3520,C3530,C3540,C3545,C3555,C3566,C3570)

NOTES:
1. PP1V2_SOC is low noise SOC rail, PP1V2_IO is its noisy cousin
2. PPVAR_EIGER_S2 typical output is 1.8V, max 3.275V during calibration
3. LDO3 and LDO8 are operating near-dropout by design (1.24Vin, 1.2Vout)
4. Max system load currents provided in power tree, radar # 43311246
5. OTP will disable LDO13 and LDO14 for all programs. Software must enable them for D52 and D54.
6. LDO6 is OTP programmed to be a load switch

998-19244
CRITICAL

U3300
TMLL69A0
WLCSP
SYM 1 OF 5
ROOM=PMU

VDD_BOOST_LDO	LDO GROUP 1	VLDO1	J6
VDD_BOOST_LDO		VLDO5	L1
VDD_BOOST_LDO		VLDO5	L2
VDD_BOOST_LDO		VLDO5	L3
VDD_BOOST_LDO		VLDO7	H3
VDD_BOOST_LDO		VLDO10	J1
VDD_BOOST_LDO		VLDO13	J3
VDD_MAIN_LDO	LDO GROUP 2 & INTERNAL POWER	VLDO9	K6
		VLDOINT	K4
		VMBX	L9
		VCP_OUT	N6
VDD_LDO2	LDO GROUP 3	VLDO2	H6
VDD_LDO15		VLDO15	G6
VDD_LDO14_3	LDO GROUP 4	VLDO3	L4
		VLDO14	L6
VDD_LDO4	LDO GROUP 5	VLDO4	H1
VDD_LDO6		VLDO6	F4
VDD_LDO8		VLDO8	F1
VDD_LDO11		VLDO11	G1
VDD_LDO12		VLDO12	G4
VIN_SW2_1_0	BUCK3 SWITCHES	VOUT_SW0	R4
VIN_SW2_1_0		VOUT_SW0	R5
VIN_SW2_1_0		VOUT_SW1	M4
VIN_SW2_1_0		VOUT_SW2	M5
VIN_SW5_4_3	BUCK6 SWITCHES	VOUT_SW3	R1
VIN_SW5_4_3		VOUT_SW4	R2
VIN_SW5_4_3		VOUT_SW4	R3
VIN_SW5_4_3		VOUT_SW5	M3
VIN_SW6	BUCK12 SWITCHES	VOUT_SW6	M1
VIN_SW6		VOUT_SW6	M2

PP_VDD_BOOST: C3504 2.2UF, C3505 2.2UF
PP_VDD_MAIN: C3521 0.1UF
PP_VDD_BOOST / PP_VDD_MAIN: C3522 2.2UF — PLACE AT LDO11/LDO12 INPUT
PP1V8_S4: C3523 2.2UF — PLACE AT SW2/1/0 INPUT
PP1V2_S4: GND, Dotara, UROSC
PP0V9_S1

PMU_VMBX / PMU_VPUMP: C3507 0.1UF, C3506 0.1UF

C3510 15UF	(1) PP3V3_USB_S2	VOLTAGE=3.3	PP3V3_USB_S2	LDO1 200 mA MAX
C3570 15UF	(7) PP3V0_S2	VOLTAGE=3.0	PP3V0_S2	LDO7 250 mA MAX
C3515 4UF	(10) PP3V0_DISPLAY_S2	VOLTAGE=3.0	PP3V0_DISPLAY_S2	LDO10 50 mA MAX
C3545 15UF (PACK_IGNORE=TRUE, PACK_OPTION=D52,D54,DEV) / C3546 10UF (PACK_IGNORE=TRUE, PACK_OPTION=D52,D54,DEV)	(13) PP3V1_TOUCH_S2	VOLTAGE=3.15	NC_PP3V1_TOUCH_S2	LDO13 150 mA MAX
C3590 10UF	(9) PP1V8_ALWAYS	VOLTAGE=1.8	PP1V8_ALWAYS	LDO9 10 mA MAX
C3509 15UF / C3508 220PF	PP1V5_VLDOINT	VOLTAGE=1.5	PP1V5_VLDOINT	
C3520 15UF	(2) PP1V8_AUDIO_VA_S2	VOLTAGE=1.8	PP1V8_AUDIO_VA_S2	LDO2 50 mA MAX
C3566 15UF	(15) PPVAR_EIGER_S2	VOLTAGE=3.0	PPVAR_EIGER_S2	LDO15 100 mA MAX
C3530 15UF	(3) PP1V2_SOC	VOLTAGE=1.2	PP1V2_SOC	LDO3 400 mA MAX
C3555 15UF (PACK_IGNORE=TRUE, PACK_OPTION=D52,D54,DEV)	(14) PP1V2_TOUCH_S2	VOLTAGE=1.22	NC_PP1V2_TOUCH_S2	LDO14 150 mA MAX
C3540 15UF	(4) PP0V7_VDD_LOW_S2	VOLTAGE=0.7	PP0V7_VDD_LOW_S2	LDO4 300 mA MAX
	(6) PP1V2_NFC_S2	VOLTAGE=1.2	PP1V2_NFC_S2	LDO6 250 mA MAX
C3580 20UF	(8) PP1V0_S4	VOLTAGE=1.0	PP1V0_S4	LDO8 600 mA MAX
C3525 20UF	(11) PP0V6_VDDQL_S1	VOLTAGE=0.6	PP0V6_VDDQL_S1	LDO11 700 mA MAX
C3535 20UF	(12) PP0V78_SOC_FIXED_S1	VOLTAGE=0.78	PP0V78_SOC_FIXED_S1	LDO12 580 mA MAX

RADAR #: 50896745

Assumes load cap <80mOhm DCR

Place XW3580 near U3300.F1 (star route from PMU to Arrow)

XW3580 (NO_XNET_CONNECTION, OMIT, SHORT-10L-0.1MM-SM, ROOM=PMU, PACK_OPTION=D52,D53,D54)
PP1V0_R1_ANA_S4, VOLTAGE=1.0

PP1V8_S2	VOLTAGE=1.8	33 37 64 72 79 83 93 94 99 100	BUCK_SW0: 700 mA MAX, 50mOhm MAX
PP1V8_IO	VOLTAGE=1.8	20 33 55 83	BUCK_SW1: 350 mA MAX, 50mOhm MAX
PP1V8_TOUCH_S2	VOLTAGE=1.8	83	BUCK_SW2: 200 mA MAX, 125mOhm MAX
PP1V2_S2	VOLTAGE=1.2	23 33 67 77 78 82 93 96 97 99	BUCK_SW3: 200 mA MAX, 125mOhm MAX
PP1V2_IO	VOLTAGE=1.2	23 33	BUCK_SW4: 890 mA MAX, 25mOhm MAX
PP1V2_S1	VOLTAGE=1.2	33	BUCK_SW5: 50 mA MAX, 125mOhm MAX
PP0V83_NAND	VOLTAGE=0.83	25	BUCK_SW6: 820 mA MAX, 50mOhm MAX

SYNCING: D52, D53, D54, DEV

DCR Requirement: <50mOhm MAX (30mOhm NOM) for Rin + Rout
Rin = DCR from XW3420 (PP0V9_S1 feedback) to U3300.N1 (SW6 input)
Rout = DCR from U3300.M1 (SW6 output) to U2900.G6 (NAND VDD)

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PMU - GPIOs + DIOs

See 50000123 for IO settings

AMUX CAPS

AMUX_RCAM_PVDD → C3673 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

AMUX_PMU_FROM_CAM_PMU → C3671 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

AMUX_PMU_FROM_GECKO → NOSTUFF C3672 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

RESET_IN3: Enabled only in PMU awake state

VBUS_DETECT: OTP programmed to be active low

FORCE_SYNC: SCAN_ACTIVE can tap into 1.2V or 1,8V side, whichever is easier

LDO13_EN: Wired to Ada (D52/D54)
LDO13_EN: GND (D53)

AMUX_A7 tied to GND for AMUX calibration

MEMS Oscillator #1 (Active)

PP1V8_ALWAYS → C3653 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

Y3601 32.768KHZ-50PPM CSP 197S00228 (VDD, NC, CLKOUT, GND)

PACK_OPTION=D53,DEV BOMOPTION=32K:MEMS1

MEMS Oscillator #2 (Active)

PP1V8_ALWAYS → C3654 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

Y3602 32.768KHZ-50PPM CSP 197S00228

CLK_PMU_XTAL2_XOUT_32K_R → R3652 0.00 0% 1/32W MF 01005 ROOM=SOC

PACK_OPTION=D53 BOMOPTION=32K:MEMS2

XTAL Oscillator (Passive)

Y3600 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM CRITICAL 197S00013 BOMOPTION=32K:XTAL

OMIT_TABLE C3651 22PF 2% 16V C0G 01005 ROOM=PMU

OMIT_TABLE C3652 22PF 2% 16V C0G 01005 ROOM=PMU

XW3600 SHORT-20L-0.05MM-SM OMIT NO_XNET_CONNECTION

RADAR #: 50214461

Note: only 1 32K option may be stuffed at once

33 PP1V2_S2 → R3661 20.0K 5% 1/32W MF 01005 ROOM=PMU

U3300 TMLL69A0 WLCSP SYM 4 OF 5 — 998-19244 CRITICAL — ROOM=PMU

IO_SOC_TO_PMU_WDOG_RESET	RESET_IN1	L12
IO_PMU_FROM_KRAKEN_RESET	RESET_IN2	M11
IO_SOC_TO_PMU_SOCHOT_RESET_L	RESET_IN3	L11
NC_DEV_PMU_SHDN_1V8	SHDN	L10
NC_DEV_PMU_CRASH_L_1V8	CRASH*	M10
IO_PMU_KRAKEN_TO_DOTARA_RESET_L_1V8	FAULT_OUT*	L7
IO_PMU_TO_SYSTEM_RESET_L	RESET*	N9
IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY	ACTIVE_READY	L8
IO_PMU_TO_NAND_SYSTEM_ALIVE	SYS_ALIVE	M9
GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	VBUS_DETECT	R14
NC_DEV_PMU_REQUEST_DFU	REQUEST_DFU	K13
IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	FORCE_DFU	N15
CLK_PMU_TO_AOP_32K	SLEEP_32K	T5
CLK_PMU_TO_TOUCH_32K_1V8	OUT_32K	R7
IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8	FORCE_SYNC	T13
IO_KRAKEN_TO_PARROT_PMU_USB_EN	LDO1_EN	N13
GND	LDO13_EN	P6

AMUX: AMUX_SOC_TO_PMU_AMUX_OUT (F9), IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8 (E11), AMUX_PMU_TO_ADC_IN (E10), AMUX_PMU_FROM_GECKO (F12), AMUX_RCAM_PVDD (E8), IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA (F13), GND (E9), GND (E12), AMUX_PMU_AY (G13); AMUX_A0 … AMUX_A7, AMUX_AY; AMUX_B0 … AMUX_B7, AMUX_BY

GPIO: GPIO_AP_TO_AMUX_PMU_SYNC (E7), AMUX_PMU_FROM_DISPLAY (F10), DOTARA_SUPER_GPIO_1V8 (F8), AMUX_PMU_FROM_CAM_PMU (G11), GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8 (G8), GPIO_PMU_TO_AMUX_PMU_SUPER_TP (G9), CLK_AP_TO_PMU_TST_CLKOUT (H9), CLK_GPIO_S4_PMU_TO_WLAN_R1_32K (H8), AMUX_PMU_BY (G12)

DFT: GND (M7), SWD_NUB_TO_PMU_TOUCH_SWCLK (M6), GND (T2), GND (E5); DFT_CTRL0, DFT_CTRL1, VSS_DFT_2, VPP

SPMI: SPMI0_NUB_TO_PMU_DOTARA_CLK (P14), SPMI0_NUB_BI_PMU_DOTARA_DATA (N14); SPMI_SCLK, SPMI_SDATA

32KHZ OSCILLATOR: CLK_PMU_XTAL1_XIN_32K (T1), CLK_PMU_XTAL2_XOUT_32K (U1), VSS_PMU_XTAL (U3), IO_PMU_XTAL_SEL_1V5 (T3); XIN, XOUT, VSS, NXTAL_MEMS

1V2 LOGIC INPUT POWER: 33 PP1V2_S4 → C3640 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU → VDDIO1V2 (P13)

XTAL LAYOUT NOTES
1. Flood plane of VSS_PMU_XTAL on the layer beneath the XTAL (Y3600)
2. Drop via for VSS42 (U3300.U3) directly to the VSS_PMU_XTAL plane
3. Drop 2nd via under U3300.U3 from VSS_PMU_XTAL to XW3600
4. Tie XW3600 directly from via to GND plane

MEMS vs XTAL Select

33 29 PP1V5_VLDOINT

XTAL Select:
1V5 = MEMS (Active)
GND = XTAL (Passive)

R3650 0.00 0% 1/32W MF 01005 ROOM=SOC — PACK_OPTION=D53,DEV BOMOPTION=32K:MEMS1&32K:MEMS2

PACK_OPTION=D52,D54 → R3651 0.00 0% 1/32W MF 01005 ROOM=SOC — PACK_OPTION=D53,DEV BOMOPTION=32K:XTAL

THROTTLERS: VDD_MAIN_SNS, UVWARN*, VDD_BOOST_UVLO*, CPU_TRIGGER0*, CPU_TRIGGER1*, GPU_TRIGGER0*, GPU_TRIGGER1*

ADC: IBAT, VBAT, BRICK_ID1, BRICK_ID2, ADC_IN

BUTTONS: BUTTON1, BUTTON2, BUTTON3, BUTTON4, BUTTONO1, BUTTONO2, DBLCLICK_DET

GPIO: HV,HLD (S4) GPIO1; HLD (S4) GPIO2; SWDIO GPIO3; HLD (S4) GPIO4–GPIO8; GPIO9–GPIO16; GPIO17–GPIO24; HV,SEQ GPIO25

HLD (S4) = Hold Capable; HV = High Voltage; SEQ = Sequenced

NTC: TDEV1–TDEV5, TCAL

REFERENCES: VREF_ADC, VREF, IREF, VSS_REF

K9	PMU_VDD_MAIN_SNS	
P8	IO_AP_FROM_PMU_PRE_UVLO_L	OUT 23
T7	NC_DEV_PMU_VDD_BOOST_UVLO_L	33
U15	NC_DEV_PMU_CPU_TRIGGER0	OUT 23
T14	IO_AP_FROM_PMU_SW_SHDN_L	OUT 23
R13	NC_DEV_PMU_GPU_TRIGGER0	OUT 23
U14	NC_DEV_PMU_GPU_TRIGGER1	OUT 23
J9	PMU_VDD_MAIN_SENSE_N	
J10	PMU_VDD_MAIN_SENSE_P	
F11	IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA	IN 30 57 65
G14	ANALOG_PMU_VDD_MAIN_SENSE_FILT	
H10	AMUX_PMU_TO_ADC_IN (CKPLUS_WAIVE=SINGLE_COMP_NET)	30
K15	IO_BUTTON_VOL_DOWN_L_1V8	IN 72
M13	IO_BUTTON_SIDE_L_1V8	IN 72
N12	IO_BUTTON_VOL_UP_L_1V8	IN 72
M12	IO_BUTTON_RINGER_A_1V8	IN 72
L14	NC_DEV_PMU_DOWN_BUTTONO_L	33
L13	NC_DEV_PMU_SIDE_BUTTONO_L	33
M14	GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L	OUT 33 89
P7	NC_DEV_PMU_GPIO_1	32
R12	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	32
P12	SWD_NUB_BI_PMU_SWDIO	32
P11	GPIO_S4_PMU_TO_R1_RESET_L	32
U12	GPIO_S4_PMU_TO_WLAN_REG_ON	32
T12	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	32
R11	NC_DEV_PMU_GPIO_7	32
N11	GPIO_PMU_FROM_WLAN_HOST_WAKE	32
N10	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	32
T11	GPIO_PMU_TO_CCG2B_RESET_L	32
U11	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	32
U10	GPIO_PMU_FROM_CODEC_WAKE_L	32
T10	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	32
R10	GPIO_PMU_NFC_TO_ARCAMP_RESET_L	32
N8	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	32
M8	GPIO_PMU_NFC_TO_ARCAMP_TRIG	32
P10	I2C2_AOP_SCL	32
T9	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8	32
R9	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8	32
R8	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	32
P9	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	32
T8	GPIO_SEQ_PMU_TO_NFC_EN	32
U5	GPIO_SEQ_PMU_TO_BOOST_EN_1V8	32
T6	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	32
R6	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8	32
H13	NTC_FOREHEAD_P	43
H12	NTC_RADIO_BB_P	44 93
J13	NTC_RADIO_PA_P	44 96
J12	NTC_AP_P	43
H11	NTC_BATTERY_P	43
G10	ANALOG_PMU_TCAL	
J8	ANALOG_PMU_VREF_ADC	
K10	ANALOG_PMU_VREF	
J11	ANALOG_PMU_VSS_REF	
K11	ANALOG_PMU_VSS_REF	

GPIO01 requires 200k PD if used (glitch mitigation)

GPIO25 requires 200k PD if used (glitch mitigation)

VDD_MAIN_SNS: Drop single via to VDD_MAIN plane, place XW3650 directly at the via to the plane

NO_XNET_CONNECTION ROOM=PMU OMIT XW3650 SHORT-20L-0.05MM-SM — 2 PP_VDD_MAIN 1 — 28 33

BATTERY CURRENT SENSE FILTER

NO_XNET_CONNECTION C3670 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU

R3671 1.00K 1% 1/32W MF 01005 ROOM=PMU — PMU_VDD_MAIN_SENSE_R_N — IN 35

R3670 1.00K 1% 1/32W MF 01005 ROOM=PMU — PMU_VDD_MAIN_SENSE_R_P — IN 35

BATTERY VOLTAGE SENSE FILTER

CRITICAL R3603 9.53K 1% 1/32W MF 01005 ROOM=PMU — ANALOG_PMU_VDD_MAIN_SENSE — IN 71

RADAR#: 48731558

C3603 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

PMU GPIO Pulls

33 PP1V8_ALWAYS → R3610 100K 5% 1/32W MF 01005 ROOM=PMU — 89 34 33 32 GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8

36 32 GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8 → R3600 200K 1% 1/32W MF 01005 ROOM=PMU

REFERENCE PIN LAYOUT NOTES

1. Surface route IREF (U3300.J11) to VSS_REF (U3300.K11)
2. Drop via under VSS_REF (U3300.K11) to XW3646
3. Tie XW3646 directly from via to GND plane
4. Place XW3647 near U3300.J7

MAKE_BASE=TRUE

C3610 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

OMIT XW3646 SHORT-20L-0.05MM-SM ROOM=PMU

TCAL RESISTOR MUST BE 0.1%

R3620 3.92K 0.1% 1/32W TF 01005 ROOM=PMU

C3699 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU — ANALOG_PMU_VSS_VREF_ADC

OMIT XW3647 SHORT-20L-0.05MM-SM ROOM=PMU

SYNCING: D52, D53, D54, DEV

32K Compensation Caps

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00378	2	CAP,C0G,22PF,2%,16V,01005	C3651, C3652	CRITICAL	32K:XTAL
117S0161	1	RES,MF,0 OHM,1/32W,01005	C3651	CRITICAL	32K:MEMS1&32K:MEMS2
131S00342	1	CAP,CER,NP0/C0G,1PF,+/-0.1PF,16V,01005	C3652	CRITICAL	32K:MEMS1&32K:MEMS2

PAGE TITLE: SYS PWR: PMU: GPIO (4/5)

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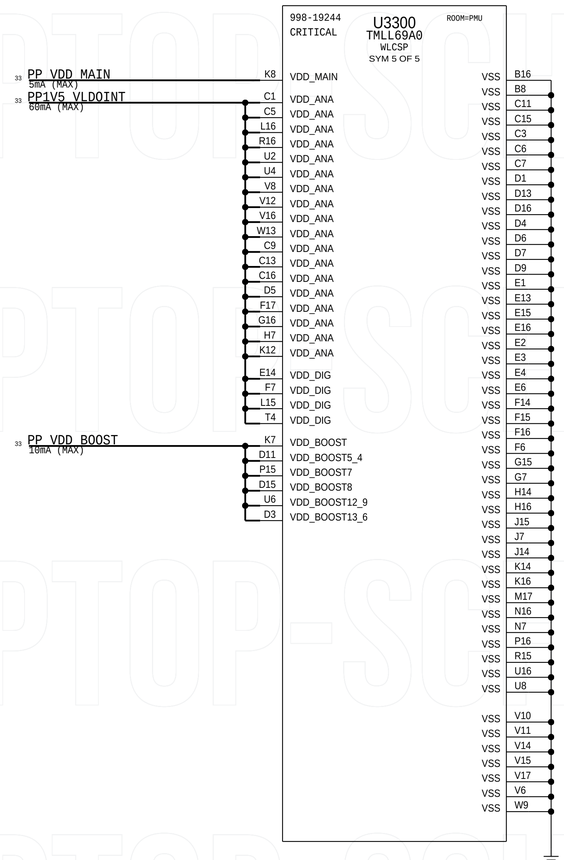

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SYS PWR: PMU: Misc (5/5)
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PMU GPIOs

PMU_GPIO1	30	NC_DEV_PMU_GPIO_1	NC_DEV_PMU_GPIO_1		33	
PMU_GPIO2	30	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L MAKE_BASE=TRUE	OUT	59	89
PMU_GPIO3	30	SWD_NUB_BI_PMU_SWDIO	SWD_NUB_BI_PMU_SWDIO	OUT	33	
PMU_GPIO4	30	GPIO_S4_PMU_TO_R1_RESET_L	GPIO_S4_PMU_TO_R1_RESET_L MAKE_BASE=TRUE	OUT	98	
PMU_GPIO5	30	GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO_S4_PMU_TO_WLAN_REG_ON MAKE_BASE=TRUE	OUT	95	
PMU_GPIO6	30	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K CKPLUS_WAIVE=SINGLE_COMP_NET MAKE_BASE=TRUE	OUT	30	89 93 98
PMU_GPIO7	30	NC_DEV_PMU_GPIO_7	NC_DEV_PMU_GPIO_7		33	
PMU_GPIO8	30	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE MAKE_BASE=TRUE	IN	95	
PMU_GPIO9	30	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L MAKE_BASE=TRUE	IN	95	
PMU_GPIO10	30	GPIO_PMU_TO_CCG2B_RESET_L	GPIO_PMU_TO_CCG2B_RESET_L MAKE_BASE=TRUE	OUT	66	89
PMU_GPIO11	30	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8 MAKE_BASE=TRUE	IN	30	33 34 89
PMU_GPIO12	30	GPIO_PMU_FROM_CODEC_WAKE_L	GPIO_PMU_FROM_CODEC_WAKE_L MAKE_BASE=TRUE	IN	58	89
PMU_GPIO13	30	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	GPIO_PMU_TO_AMUX_PMU_SUPER_TP CKPLUS_WAIVE=SINGLE_COMP_NET MAKE_BASE=TRUE	OUT	30	
PMU_GPIO14	30	GPIO_PMU_NFC_TO_ARCAMP_RESET_L	GPIO_PMU_NFC_TO_ARCAMP_RESET_L MAKE_BASE=TRUE	OUT	61	
PMU_GPIO15	30	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L MAKE_BASE=TRUE	OUT	25	89
PMU_GPIO16	30	GPIO_PMU_NFC_TO_ARCAMP_TRIG	GPIO_PMU_NFC_TO_ARCAMP_TRIG MAKE_BASE=TRUE	OUT	61	
PMU_GPIO17	30	I2C2_AOP_SCL	I2C2_AOP_SCL MAKE_BASE=TRUE	IN	14	21
PMU_GPIO18	30	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8 MAKE_BASE=TRUE	OUT	82	
PMU_GPIO19	30	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8 MAKE_BASE=TRUE	OUT	64	82
PMU_GPIO20	30	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8 MAKE_BASE=TRUE	OUT	38	89
PMU_GPIO21	30	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	GPIO_SEQ_PMU_TO_BBPMU_RESET_L MAKE_BASE=TRUE	OUT	95	
PMU_GPIO22	30	GPIO_SEQ_PMU_TO_NFC_EN	GPIO_SEQ_PMU_TO_NFC_EN MAKE_BASE=TRUE	OUT	99	
PMU_GPIO23	30	GPIO_SEQ_PMU_TO_BOOST_EN_1V8	GPIO_SEQ_PMU_TO_BOOST_EN_1V8 MAKE_BASE=TRUE	OUT	36	89
PMU_GPIO24	30	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8 MAKE_BASE=TRUE	OUT	64	89
PMU_GPIO25	30	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8 MAKE_BASE=TRUE	OUT	30	36

SYNCING: D52, D53, D54, DEV

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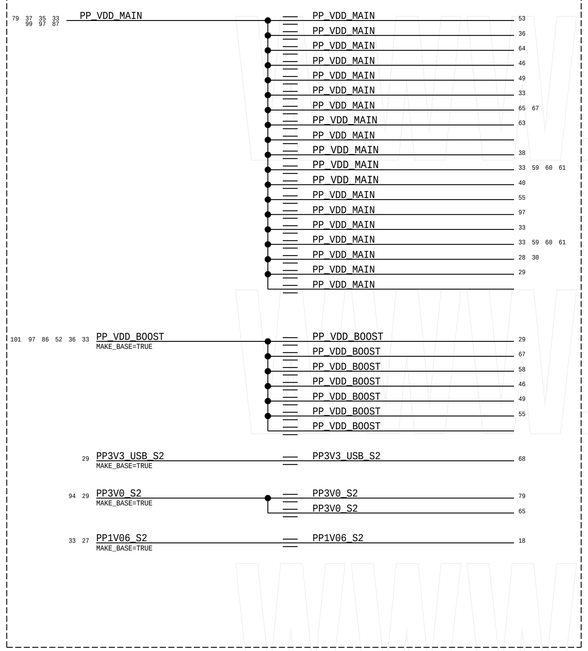
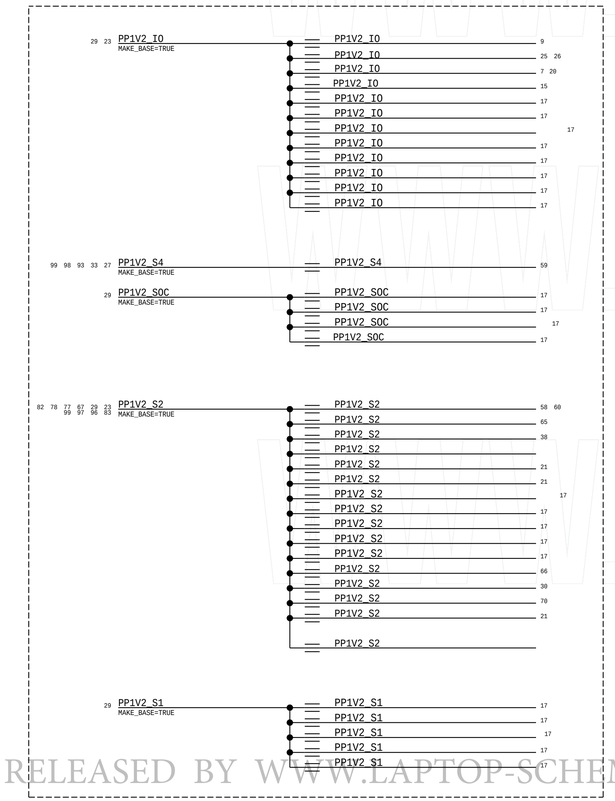
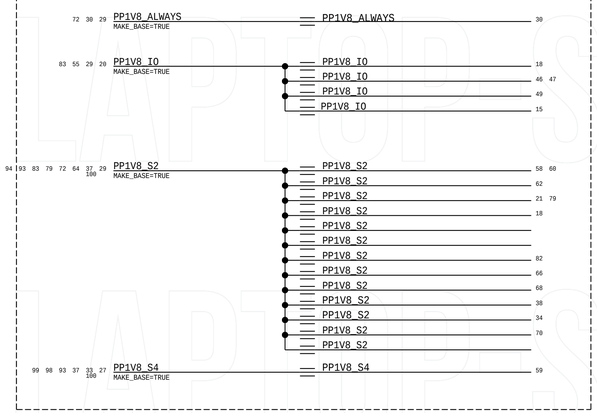
PP Misc Domains



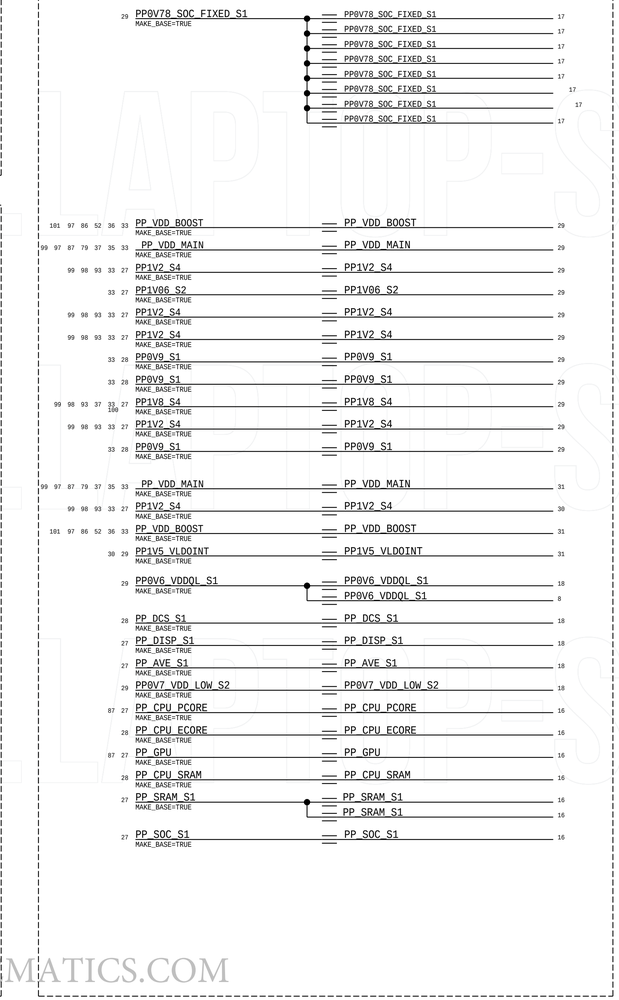
PP1V2 Domains



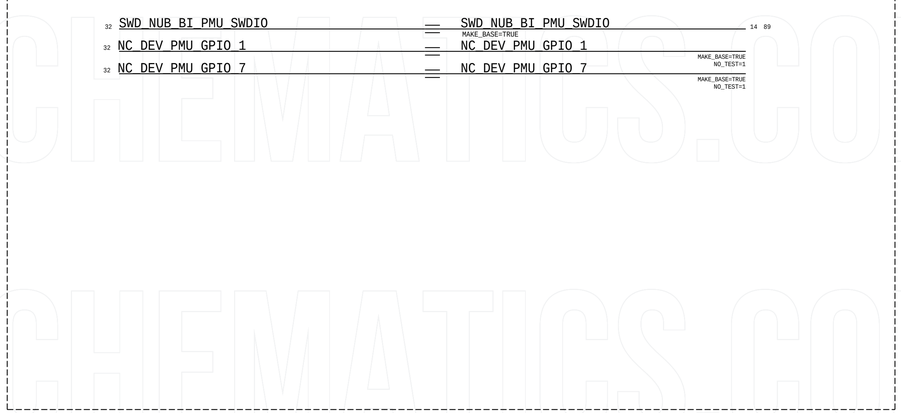
PP1V8 Domains



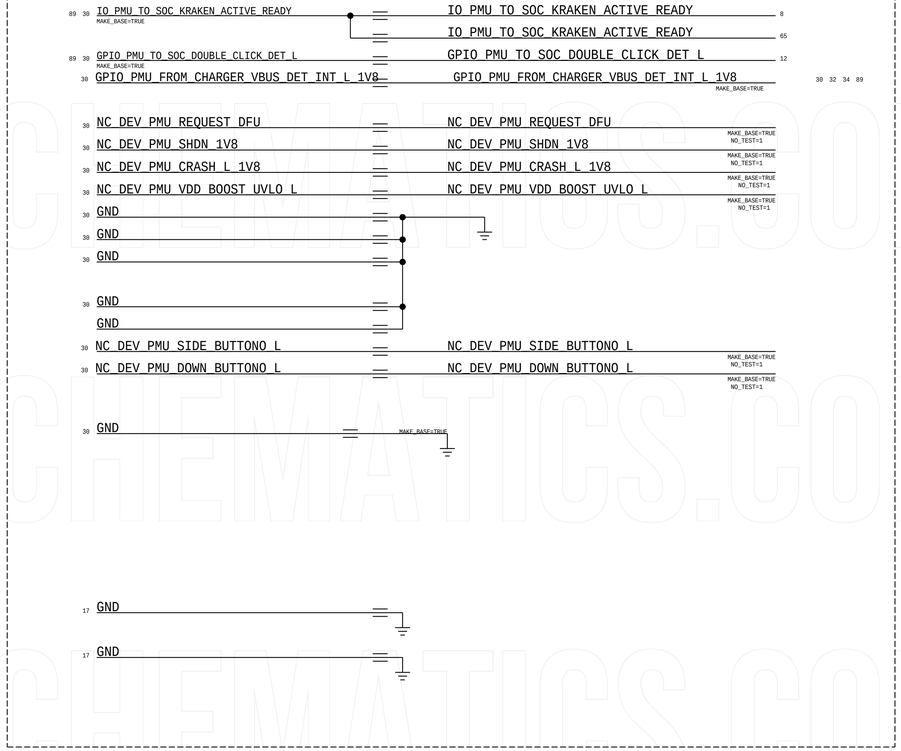
SOC + PMU Power Assignments



DEV Board Compatability



PMU Dedicated IO Assignments



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YANGTZE CHARGER
(Veridian Charger Control)

SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S01341	152S01241	BOARD_ID:D54	L4000,L4001	IND,1.0UH,20%,5.6A,28MO,H=0.90,3030	[D54 ALT]
152S01292	152S01229	[illegible]	L4000,L4001	IND,1.0UH,20%,5.2A,34MO,H=0.65,3225	[D52/D53 ALT]
152S01342	152S01254	BOARD_ID:D52	L4000	IND,1.0UH,20%,5.2A,34MO,H=0.65,3225	[D52 ALT]

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ANALOG_CHARGER_BAT_VDD_MAIN_SENSE

PP_VBUS1_E75
VOLTAGE=20.0

PP_VBUS2_DOTARA
VOLTAGE=20.0

PP_CHARGER_PMID

PP_VAR_USB_RVP

I2C2_SMC_SDA_1V8

I2C2_SMC_SCL_1V8

PP1V8_S2

RADAR #: 51315970

VBUS1_VALID: Internal PU

IO_KRAKEN_TO_CHARGER_VBUS1_VALID_L_1V8

GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8

U4000
SN2611A0-2C
DSBGA
ROOM=CHARGER
353S02307
CRITICAL

PP6V0_CHARGER_LDO_INTERNAL
VOLTAGE=6.0

LX_CHARGER_P1

LX_CHARGER_P2

PP_VDD_MAIN

NO_XNET_CONNECTION
C4040
0.1UF

NO_XNET_CONNECTION
C4044
0.1UF

C4001
1UF

C4041
220PF

C4003
220PF

NOSTUFF
C4004
220PF

C4005
2.2UF

C4006
220PF

C4007
220PF

NOSTUFF
C4008
220PF

C4010
4.7UF

C4010
4.7UF

CRITICAL
C4011
4.7UF

CRITICAL
C4012
4.7UF

C4022
220PF

C4023
220PF

C4024
220PF

C4025
220PF

C4060
220PF

C4061
2.2UF

C4062
2.2UF

CRITICAL
L4001
1.0UH-20%-5.6A-0.028OHM
PIPB030S-SM
152S01241

CRITICAL
L4001
1.0UH-20%-5.2A-0.034OHM
PIJF32250H-SM
152S01229

CRITICAL
L4000
1.0UH-20%-5.2A-0.034OHM
PIJF32250H-SM
152S01229

CRITICAL
L4000
1.0UH-20%-5.6A-0.028OHM
PIPB030S-SM
152S01241

CRITICAL
L4000
1.0UH-20%-4.2A-0.061OHM
PIPB3225KE-SM
152S01254

C4045
220PF

C4042
220PF

C4043
330PF

CRITICAL
C4090
15UF

CRITICAL
C4091
15UF

CRITICAL
C4092
15UF

Int= Interrupción

SYNCING: D52, D53, D54

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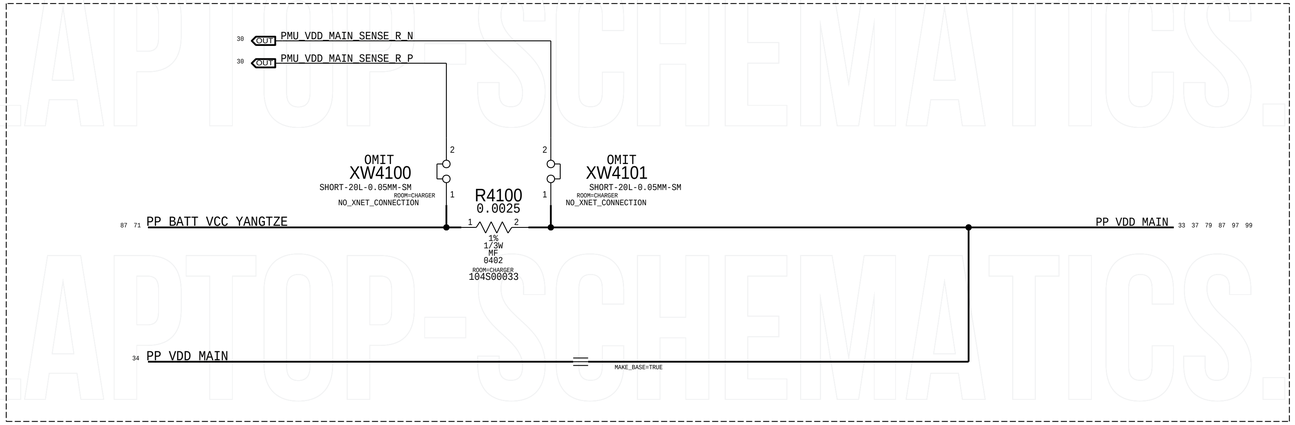
CHARGER SENSE RESISTOR



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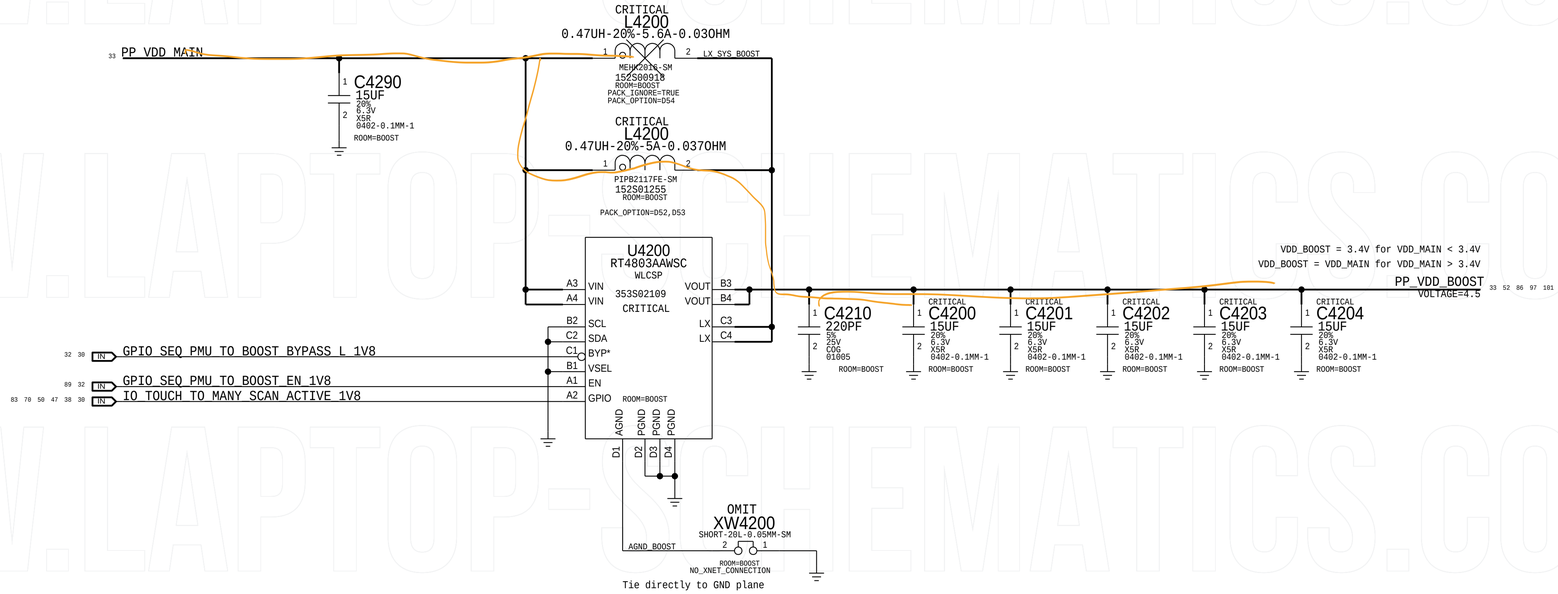
BOOST

SUBSYSTEM SPECIFIC BOM TABLES

Boost

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01124	353S02109	?	U4200	IC,SN61280E,BOOST,3.6V,4.5A,CSP16



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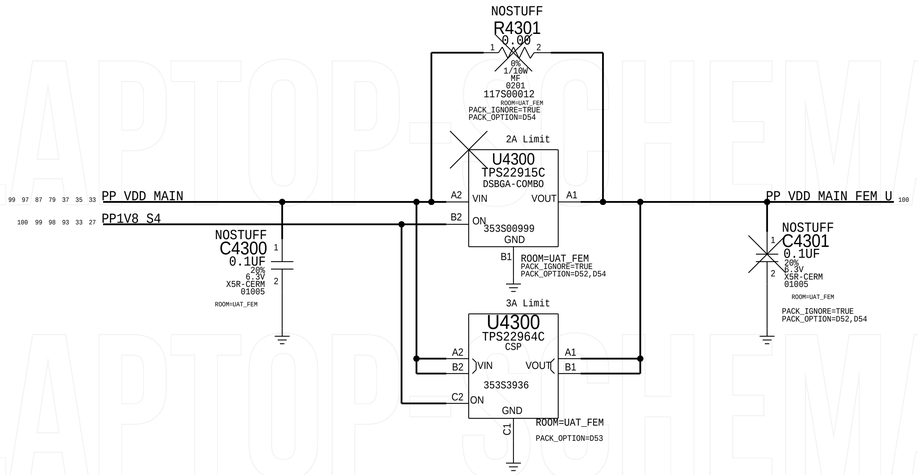
WiFi FEM VDD_MAIN Load Switches

LOAD SWITCH

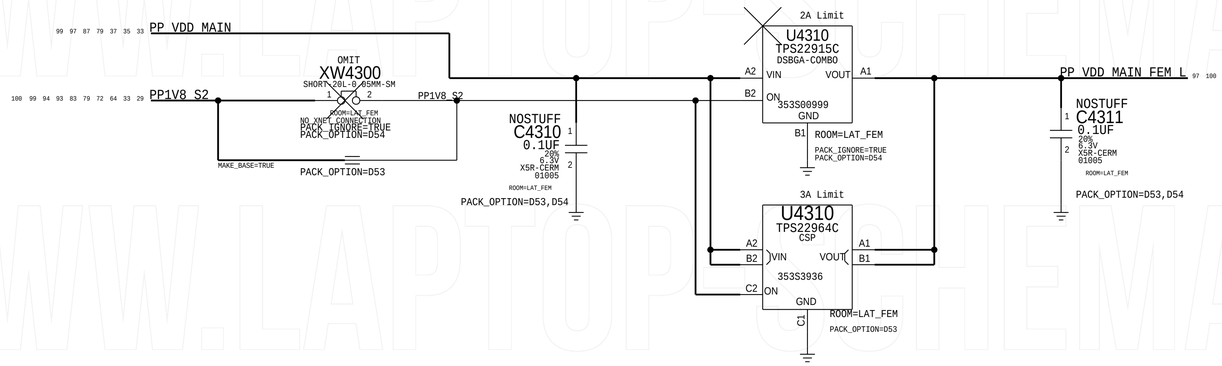
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01007	353S00999	?	ALL	IC,LOAD SWITCH, 1.5A,ON-SEMI

CRITICAL PART#	COMMENT
353S00999	IC,LOAD_SWITCH,2A,TI

UAT FEM Switch



LAT FEM Switch



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PAGE TITLE
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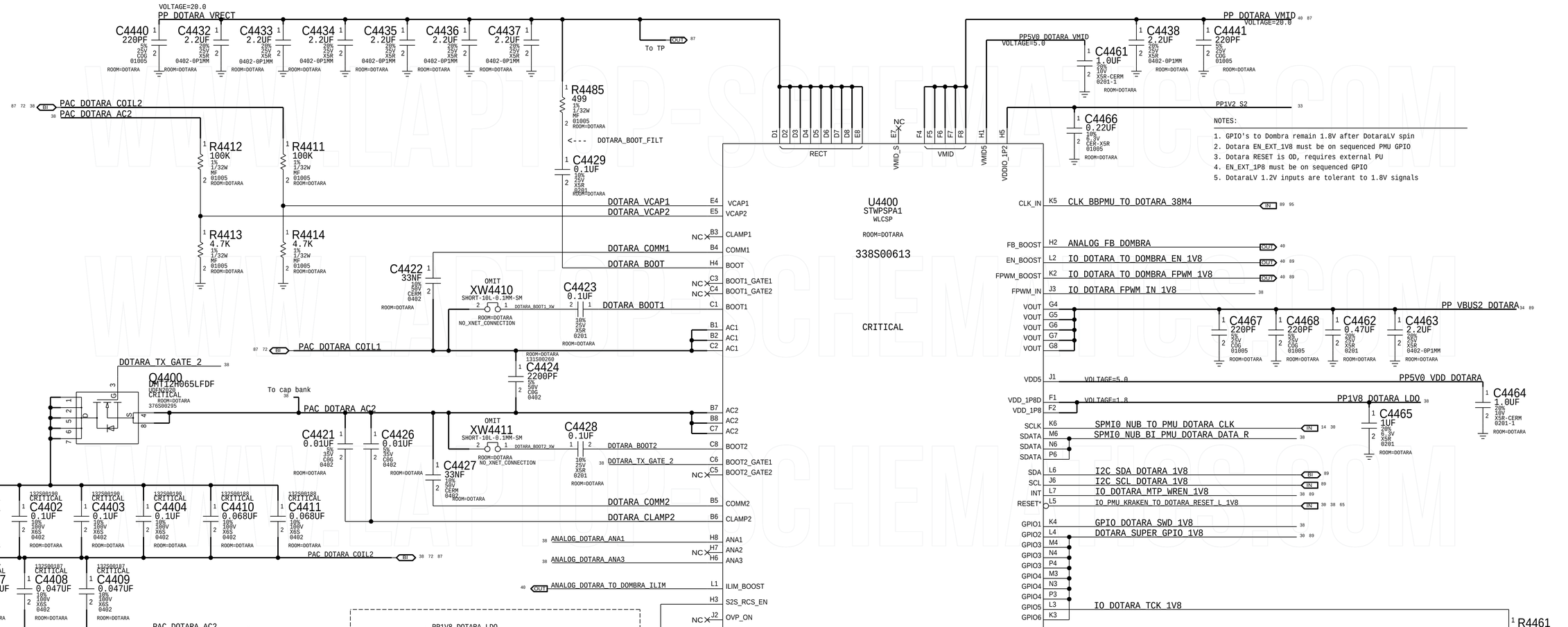
SUBSYSTEM SPECIFIC BOM TABLES

Dotara FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00362	376S00295	?	Q4400	NFET,120V,OnSemi

Dotara



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DOTARA ALIASES

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SYNCING: D52, D53, D54, DEV

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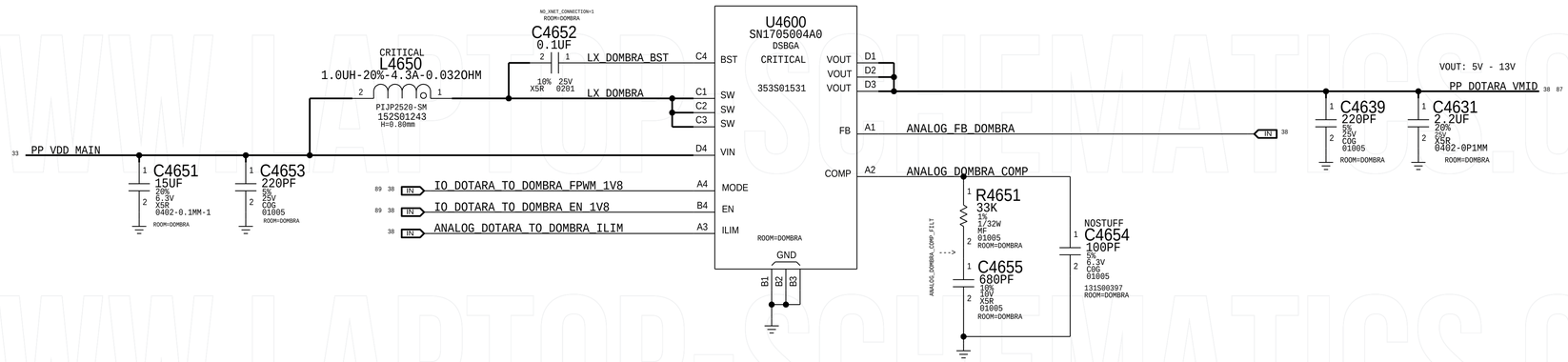
SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

Dombra



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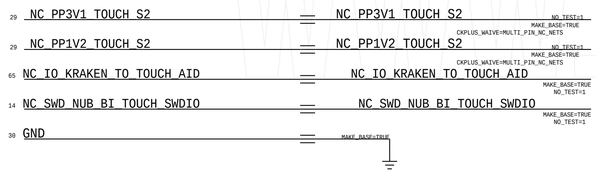
Cypher Touch Rails (unused on D53)



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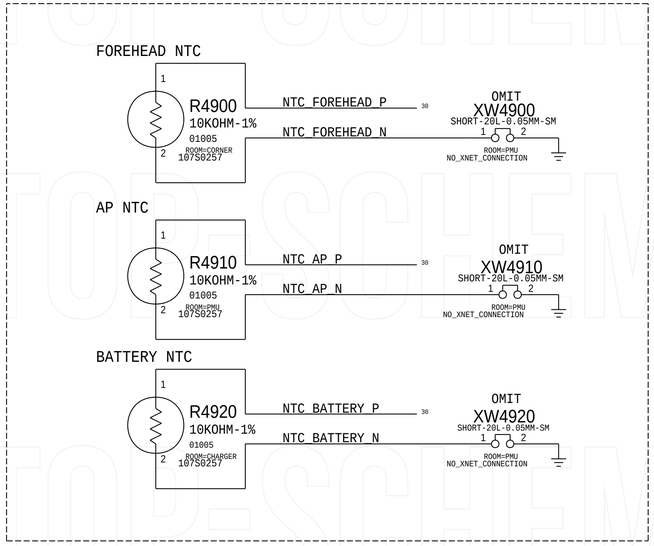
Top MLB NTCs

Place NTC XWs near PMU, route P/N differentially



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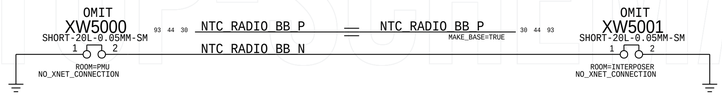
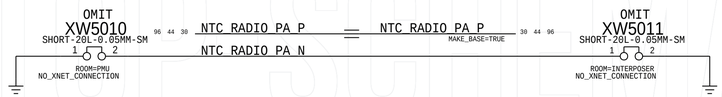
Bottom MLB NTCs

Place XW5x00 near PMU and XW5x01 near Interposer, route differentially

Baseband NTC Pair



PA NTC Pair



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D53G/P Variant Decoder

	D53G	D53P
SUPERFLEX-CAM2	None	SWide
SINGLEFLEX-CAM	SWide	Tele
BOMOPTION PRO	NOSTUFF	STUFF

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SUBSYSTEM SPECIFIC BOM TABLES

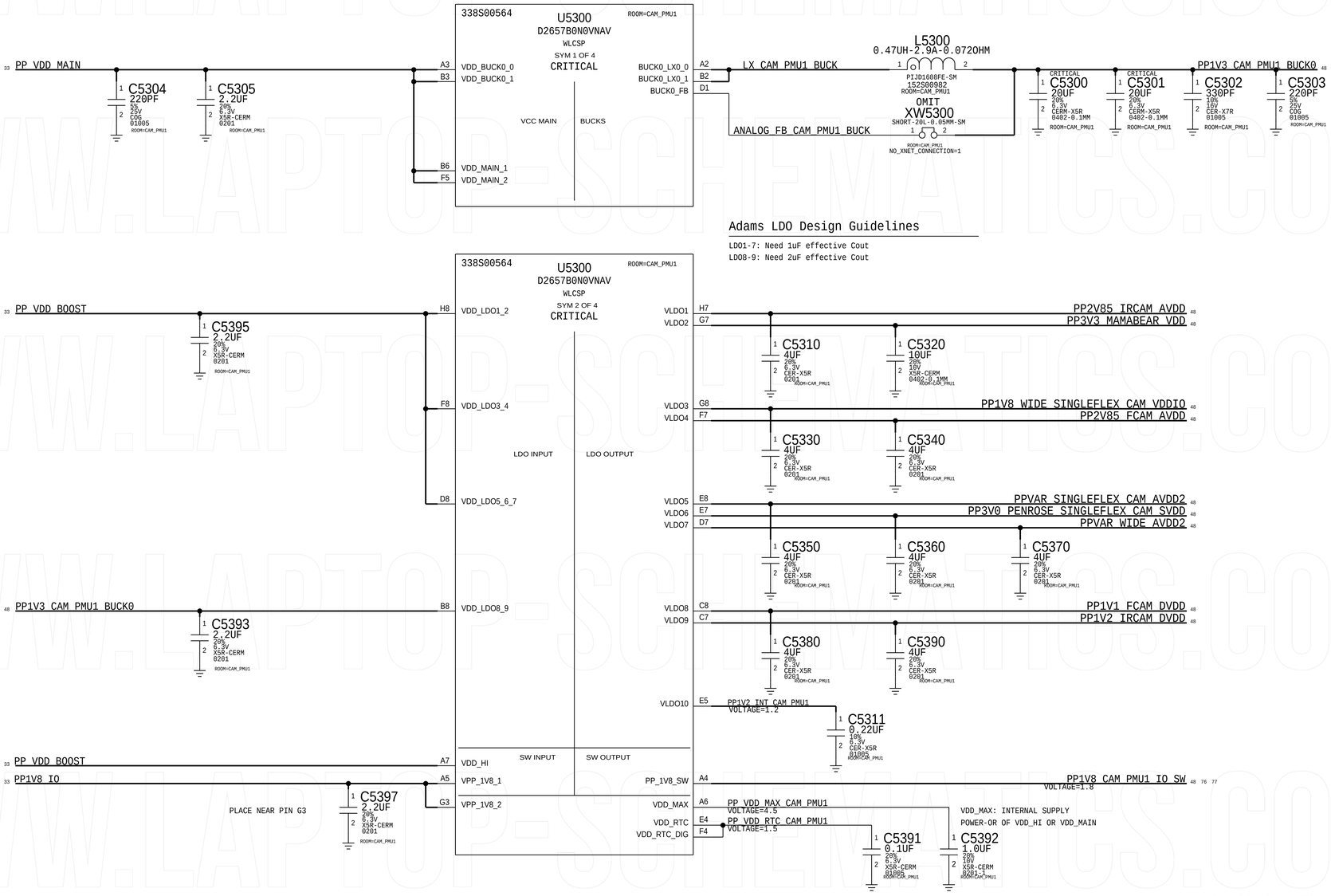
4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C5310,C5330,C5340,C5350,C5360,C5370,C5380,C5390)

(C5310,C5330,C5340,C5350,C5360,C5370,C5380,C5390)

CAMERA PMU1



SYNCING: D52, D53, D54

PAGE TITLE	CAMERA: PMU 1: Power (1/2)
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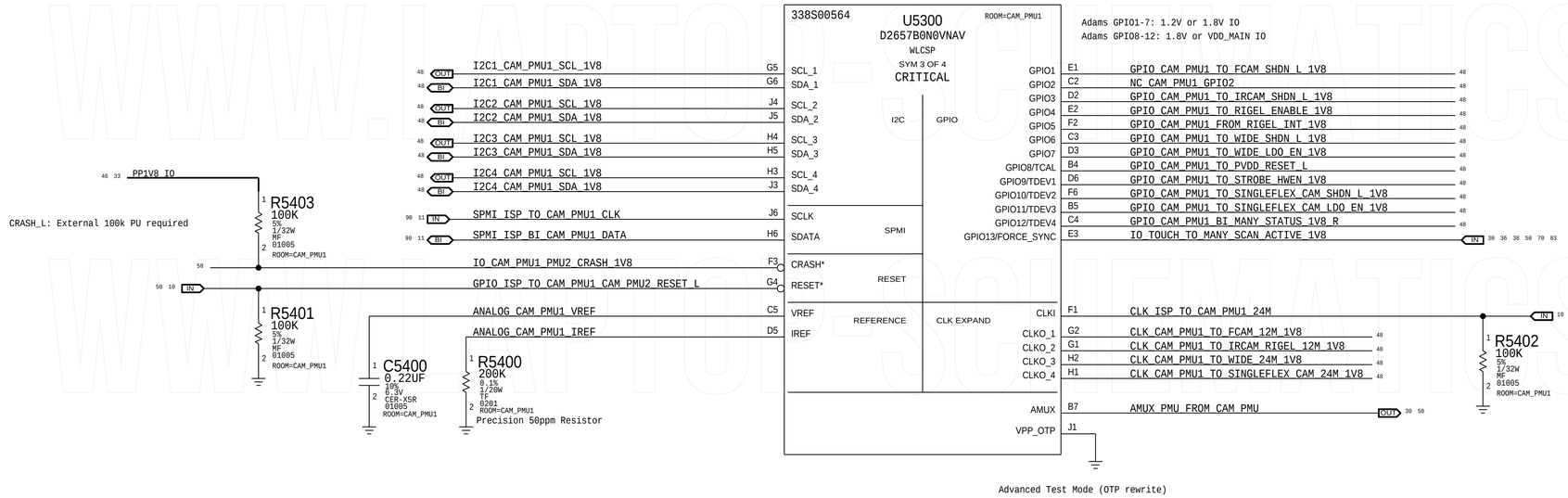
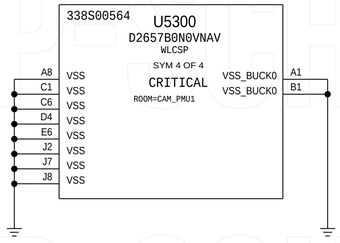
CAMERA PMU1





SYNCING: D52, D53, D54

PAGE TITLE
CAMERA: PMU 1: I/O (2/2)

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ADAMS #1 ALIASES

CAM_PMU1 I2C1: FCAM

77 76 48 46 PP1V8_CAM_PMU1_IO_SW

R5510 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5511 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

47 I2C1_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C1_CAM_PMU1_SCL_1V8 OUT 76

47 I2C1_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C1_CAM_PMU1_SDA_1V8 BI 76

MASTER	CAM PMU1	NUMBER	I2C1	DIAGS NUMBER	4	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
FCAM	1.8V	0x10	0x20,0x21	1MHz	FCAM MD Flex		

CAM_PMU1 I2C2: IRCAM/ROMEO/RIGEL

77 76 48 46 PP1V8_CAM_PMU1_IO_SW

R5520 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5521 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

47 I2C2_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C2_CAM_PMU1_SCL_1V8 OUT 77

47 I2C2_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C2_CAM_PMU1_SDA_1V8 BI 77

I2C2_CAM_PMU1_SCL_1V8 OUT 78

I2C2_CAM_PMU1_SDA_1V8 BI 78

I2C2_CAM_PMU1_SCL_1V8 OUT 55

I2C2_CAM_PMU1_SDA_1V8 BI 55

MASTER	CAM PMU1	NUMBER	I2C2	DIAGS NUMBER	5	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
IRCAM	1.8V	0x18	0x30,0x31	1MHz	Juliet Flex		
Romeo	1.8V	0x66	0xCC,0xCD	1MHz	Romeo Flex		
Rigel	1.8V	0x55	0xAA,0xAB	1MHz	Top MLB		

CAM_PMU1 I2C3: WIDE

74 73 48 PP1V8_WIDE_SINGLEFLEX_CAM_VDDIO

R5530 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5531 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

47 I2C3_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C3_CAM_PMU1_SCL_1V8 OUT 74

47 I2C3_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C3_CAM_PMU1_SDA_1V8 BI 74

MASTER	CAM PMU1	NUMBER	I2C3	DIAGS NUMBER	6	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Wide	1.8V	0x10	0x20,0x21	1MHz	RCAM MO Flex		
Lorentz	1.8V	0x74	0xE8,0xE9	1MHz	RCAM MO Flex		

CAM_PMU1 I2C4: SINGLEFLEX-CAM/LEX/STROBE

74 73 48 PP1V8_WIDE_SINGLEFLEX_CAM_VDDIO

R5540 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5541 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

47 I2C4_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C4_CAM_PMU1_SCL_1V8 OUT 73

47 I2C4_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C4_CAM_PMU1_SDA_1V8 BI 73

I2C4_CAM_PMU1_SCL_1V8 OUT 96 97

I2C4_CAM_PMU1_SDA_1V8 BI 96 97

I2C4_CAM_PMU1_SCL_1V8 OUT 97

I2C4_CAM_PMU1_SDA_1V8 BI 97

MASTER	CAM PMU1	NUMBER	I2C4	DIAGS NUMBER	7	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Tele (D53P)	1.8V	0x20	0x40,0x41	1MHz	RCAM ED Flex		
SWide (D53G)	1.8V	0x20	0x40,0x41	1MHz	RCAM BR Flex		
Raman (D53P)	1.8V	0x1C	0x38,0x39	1MHz	RCAM ED Flex		
NOTE: Tele vs Swide depends on P vs G variant (see page 52)							
Lex	1.8V	0x75	0xEA,0xEB	1MHz	Bottom MLB		
Strobe	1.8V	0x65	0xCA,0xCB	1MHz	Bottom MLB		

SIGNAL

GPIO_1	47 GPIO_CAM_PMU1_TO_FCAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_FCAM_SHDN_L_1V8	MAKE_BASE=TRUE OUT 76
GPIO_2	47 NC_CAM_PMU1_GPIO2	NC_CAM_PMU1_GPIO2	MAKE_BASE=TRUE
GPIO_3	47 GPIO_CAM_PMU1_TO_IRCAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_IRCAM_SHDN_L_1V8	NO_TEST=1 MAKE_BASE=TRUE OUT 77
GPIO_4	47 GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	MAKE_BASE=TRUE OUT 55 89
GPIO_5	47 GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	MAKE_BASE=TRUE IN 30 55 89
GPIO_6	47 GPIO_CAM_PMU1_TO_WIDE_SHDN_L_1V8	GPIO_CAM_PMU1_TO_WIDE_SHDN_L_1V8	MAKE_BASE=TRUE OUT 74
GPIO_7	47 GPIO_CAM_PMU1_TO_WIDE_LDO_EN_1V8	GPIO_CAM_PMU1_TO_WIDE_LDO_EN_1V8	MAKE_BASE=TRUE OUT 52 90
GPIO_8	47 GPIO_CAM_PMU1_TO_PVDD_RESET_L	GPIO_CAM_PMU1_TO_PVDD_RESET_L	MAKE_BASE=TRUE OUT 96
GPIO_9	47 GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	MAKE_BASE=TRUE OUT 89 93
GPIO_10	GPIO_CAM_PMU1_TO_SINGLEFLEX_CAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_SINGLEFLEX_CAM_SHDN_L_1V8	MAKE_BASE=TRUE OUT 73
GPIO_11	GPIO_CAM_PMU1_TO_SINGLEFLEX_CAM_LDO_EN_1V8	GPIO_CAM_PMU1_TO_SINGLEFLEX_CAM_LDO_EN_1V8	MAKE_BASE=TRUE OUT 52 90
GPIO_12	47 GPIO_CAM_PMU1_BI_MANY_STATUS_1V8_R	GPIO_CAM_PMU1_BI_MANY_STATUS_1V8_R	MAKE_BASE=TRUE
GPIO_13	Camera PMU1 GPIO13 intentionally not aliased		
CLKO_1	47 CLK_CAM_PMU1_TO_FCAM_12M_1V8	CLK_CAM_PMU1_TO_FCAM_12M_1V8	MAKE_BASE=TRUE OUT 76
CLKO_2	47 CLK_CAM_PMU1_TO_IRCAM_RIGEL_12M_1V8	CLK_CAM_PMU1_TO_IRCAM_RIGEL_12M_1V8	MAKE_BASE=TRUE OUT 55 77
CLKO_3	47 CLK_CAM_PMU1_TO_WIDE_24M_1V8	CLK_CAM_PMU1_TO_WIDE_24M_1V8	MAKE_BASE=TRUE OUT 74
CLKO_4	47 CLK_CAM_PMU1_TO_SINGLEFLEX_CAM_24M_1V8	CLK_CAM_PMU1_TO_SINGLEFLEX_CAM_24M_1V8	MAKE_BASE=TRUE OUT 73

D52/D53: PVDD Reset -> Lex
D54: PVDD Reset -> Alex

R5505 10K 5% 1/32W MF 01005 ROOM=CAM_PMU1

1 — 2 IO_RIGEL_BI_GRIEVOUS_STATUS_1V8 BI 55 79

R5506 10K 5% 1/32W MF 01005 ROOM=CAM_PMU1

1 — 2 IO_RIGEL_BI_MAMABEAR_STATUS_1V8 BI 55 78

POWER

VLDO1	46 PP2V85_IRCAM_AVDD	PP2V85_IRCAM_AVDD	VOLTAGE=2.9 MAKE_BASE=TRUE 77
VLDO2	46 PP3V3_MAMABEAR_VDD	PP3V3_MAMABEAR_VDD	VOLTAGE=3.3 MAKE_BASE=TRUE 78
VLDO3	46 PP1V8_WIDE_SINGLEFLEX_CAM_VDDIO	PP1V8_WIDE_SINGLEFLEX_CAM_VDDIO	VOLTAGE=1.8 MAKE_BASE=TRUE 48 73 74
VLDO4	46 PP2V85_FCAM_AVDD	PP2V85_FCAM_AVDD	VOLTAGE=2.9 MAKE_BASE=TRUE 76
VLDO5	46 PPVAR_SINGLEFLEX_CAM_AVDD2	PPVAR_SINGLEFLEX_CAM_AVDD2	VOLTAGE=3.0 MAKE_BASE=TRUE 73
VLDO6	46 PP3V0_PENROSE_SINGLEFLEX_CAM_SVDD	PP3V0_PENROSE_SINGLEFLEX_CAM_SVDD	VOLTAGE=3.0 MAKE_BASE=TRUE 52 73 80
VLDO7	46 PPVAR_WIDE_AVDD2	PPVAR_WIDE_AVDD2	VOLTAGE=3.0 MAKE_BASE=TRUE 74
VLDO8	46 PP1V1_FCAM_DVDD	PP1V1_FCAM_DVDD	VOLTAGE=1.1 MAKE_BASE=TRUE 76
VLDO9	46 PP1V2_IRCAM_DVDD	PP1V2_IRCAM_DVDD	VOLTAGE=1.2 MAKE_BASE=TRUE 77
VLDO10	Camera PMU1 LDO10 unused		
BUCK0	46 PP1V3_CAM_PMU1_BUCK0	PP1V3_CAM_PMU1_BUCK0	VOLTAGE=1.4 MAKE_BASE=TRUE 46
			PP1V3_CAM_PMU1_BUCK0 49
			52

SYNCING: NONE

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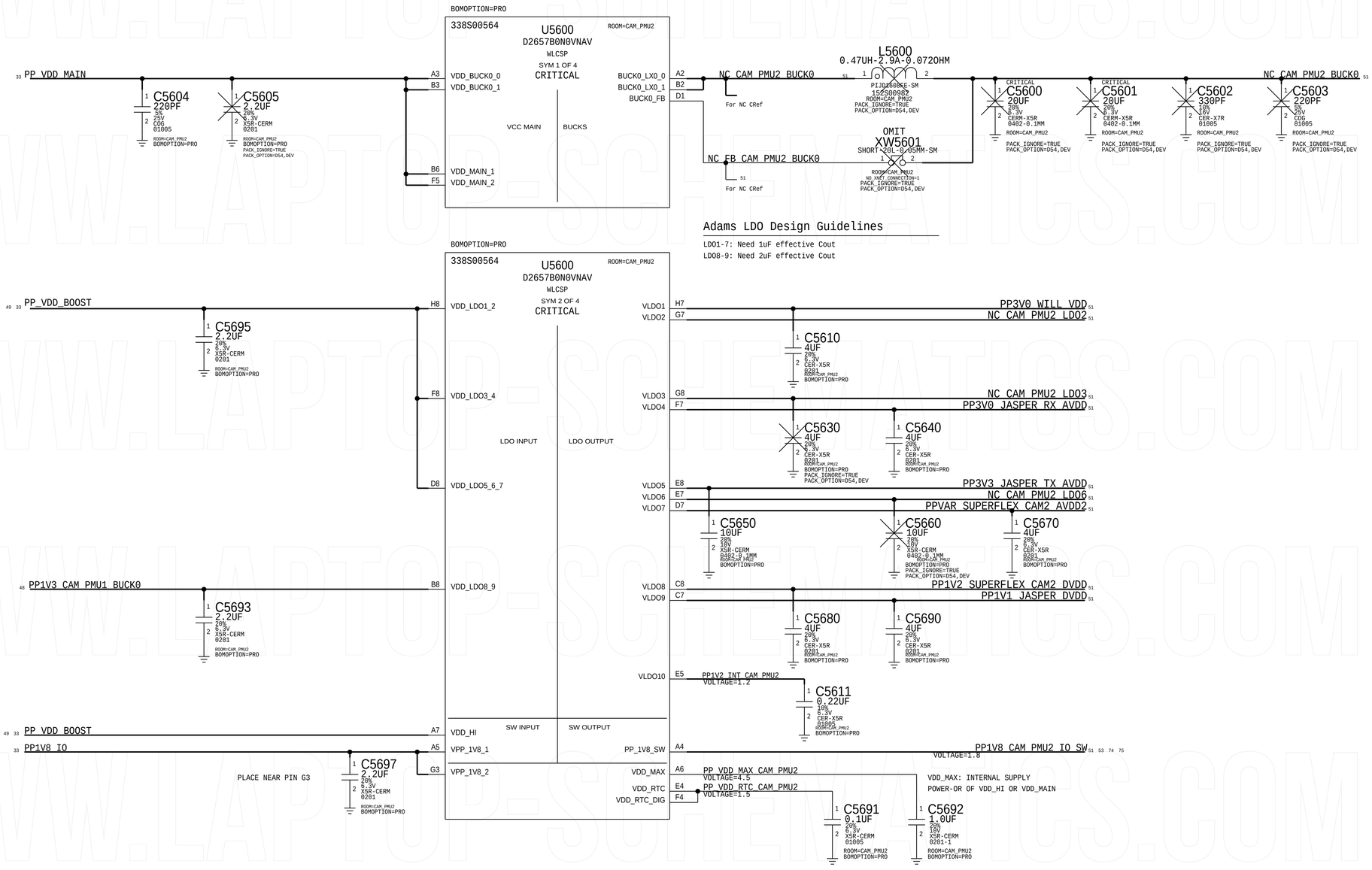
SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C5610,C5630,C5640,C5660,C5670,C5680,C5690)
(C5610,C5630,C5640,C5660,C5670,C5680,C5690)

CAMERA PMU2



SYNCING: D53, D54

PAGE TITLE	CAMERA: PMU 2: Power (1/2)
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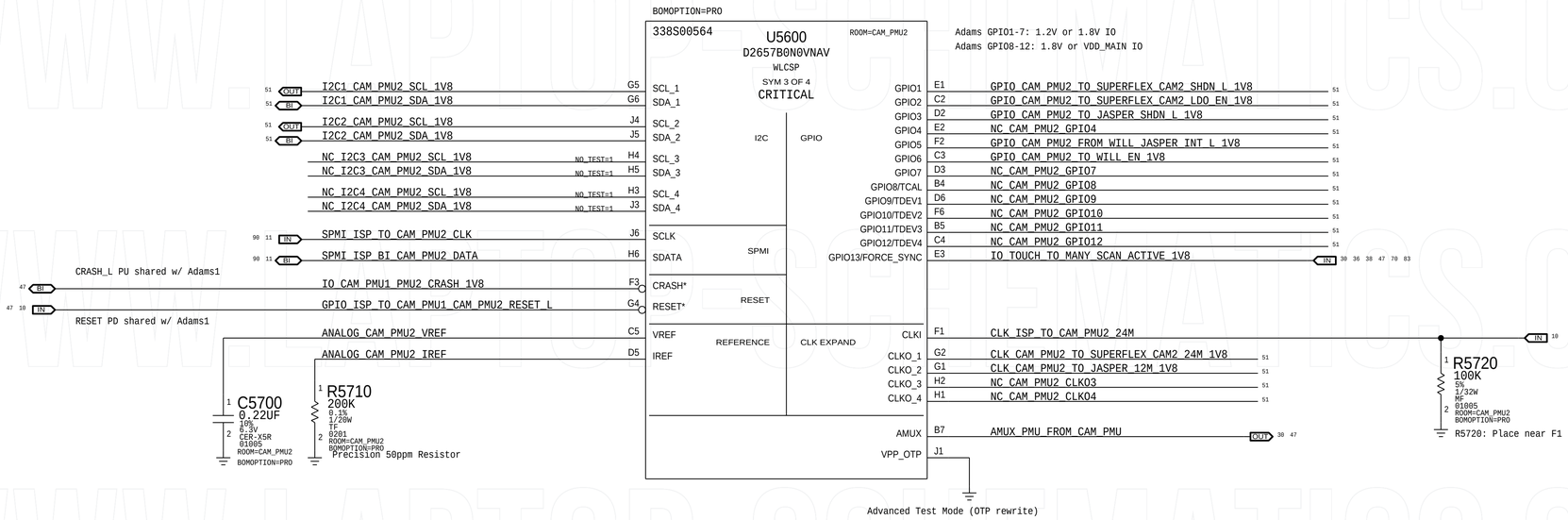
CAMERA PMU2



SYNCING: D53, D54

PAGE TITLE	CAMERA: PMU 2: I/O (2/2)
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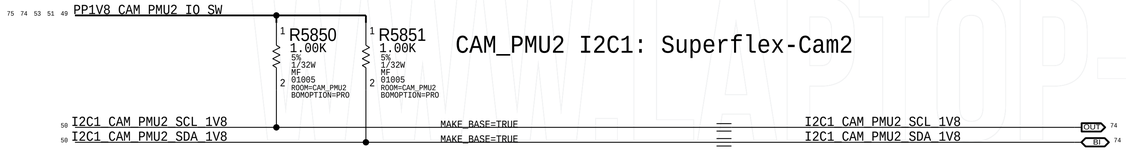
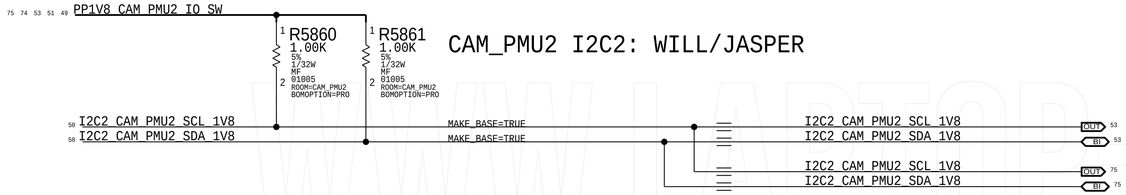
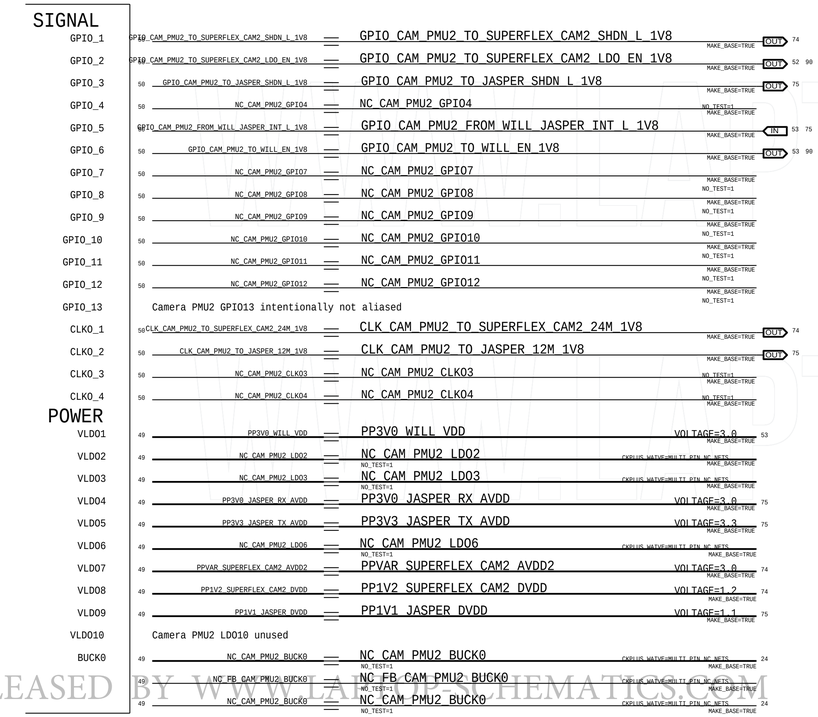
ADAMS #2 ALIASES



MASTER	CAM PMU2	NUMBER	I2C1	DIAGS NUMBER	8	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
SWide (D53P)	1.8V	0x20	0x40,0x41	1MHz	RCAM MO Flex		



MASTER	CAM PMU2	NUMBER	I2C2	DIAGS NUMBER	9	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Will	1.8V	0x40	0x80,0x81	1MHz	Top MLB		
Periscope	1.8V	0x10	0x20,0x21	1MHz	Jasper Flex		
Riker (Main Core)	1.8V	0x33	0x66,0x67	1MHz	Jasper Flex		
Riker (OVP Core)	1.8V	0x34	0x68,0x69	1MHz	Jasper Flex		
Jasper (EEPROM)	1.8V	0x51	0xA2,0xA3	1MHz	Jasper Flex		



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SUBSYSTEM SPECIFIC BOM TABLES

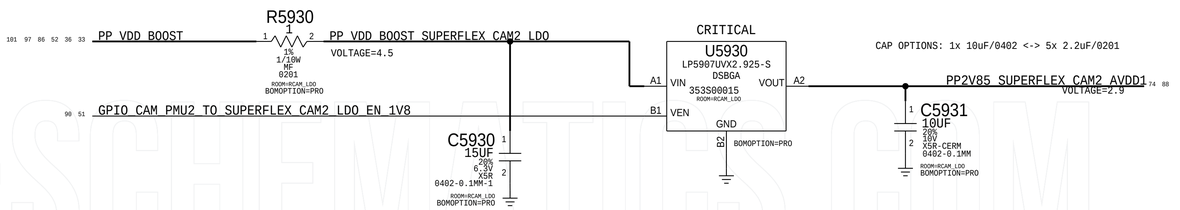
2.925V LDO

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02185	353S00015	?	ALL	IC,LDO,REG,2.925V,250MA,ONSEMI

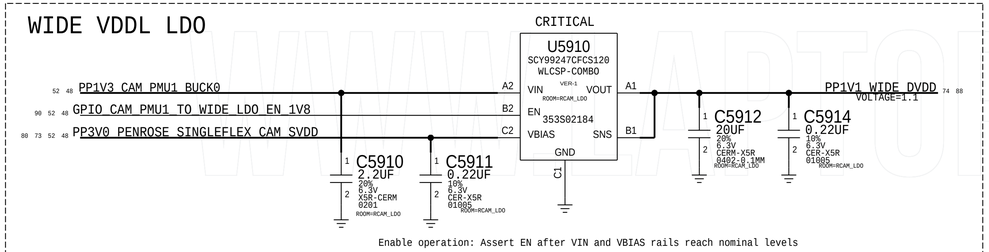
1.2V LDO

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02127	353S02184	?	ALL	IC,LDO,REG,1.20V,100MA,RICHTEK

SUPERFLEX-CAM2 VDDH1 LDO

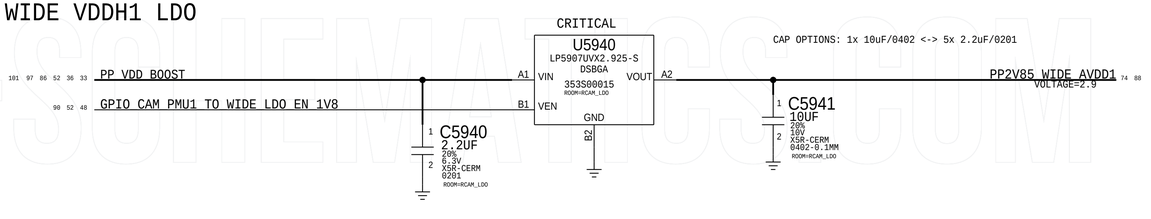


WIDE VDDL LDO

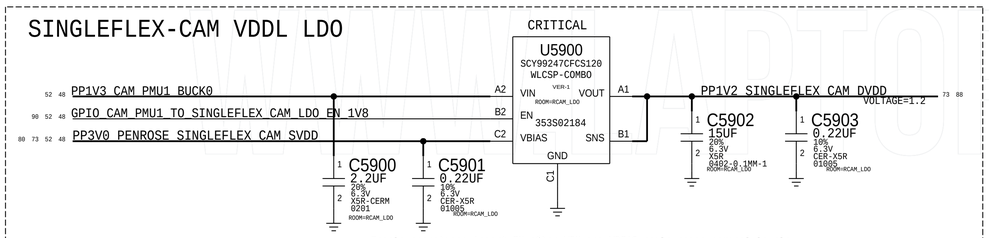


Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

WIDE VDDH1 LDO

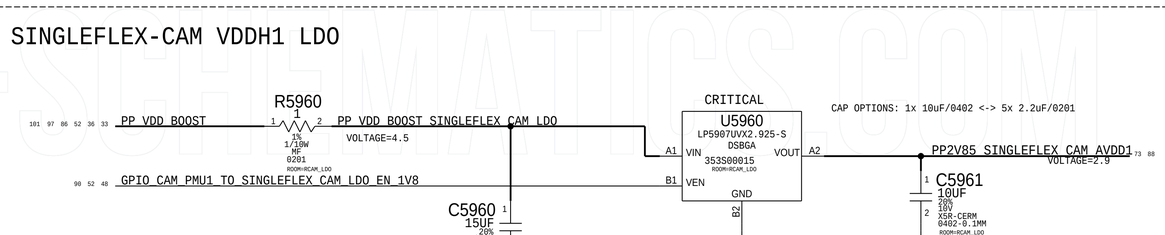


SINGLEFLEX-CAM VDDL LDO



Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

SINGLEFLEX-CAM VDDH1 LDO



SYNCING: NONE

PAGE TITLE	CAMERA: Discrete LDOs
DRAWING NUMBER	051-05215
SIZE	D
REVISION	4.6.0
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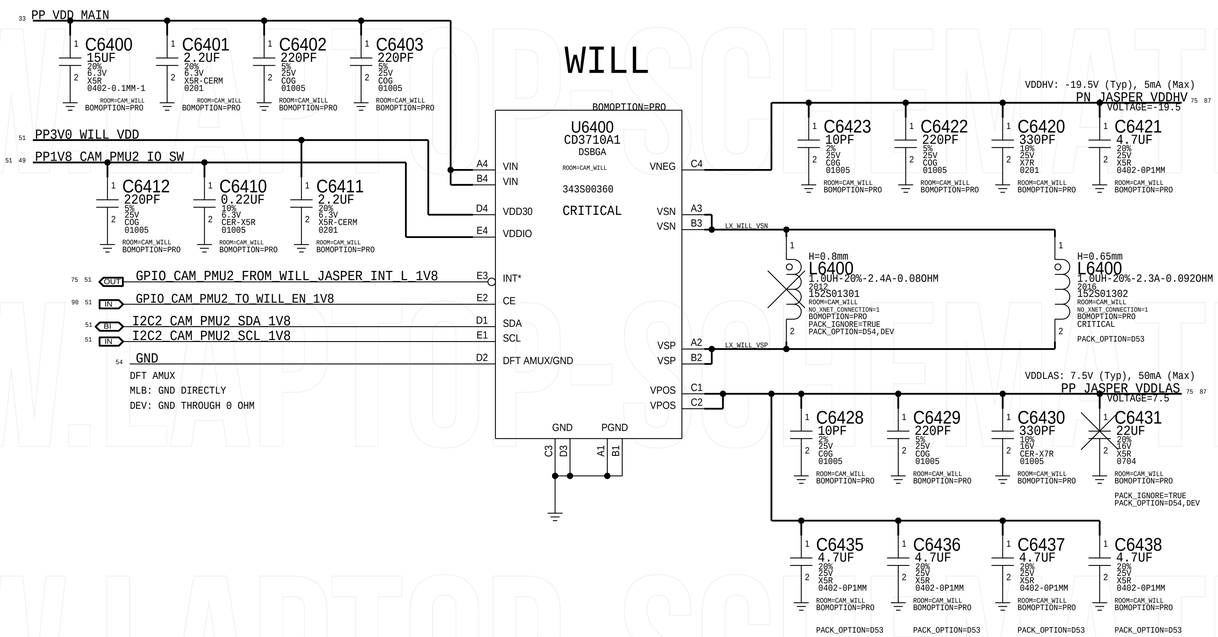
SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01343	152S01301	?	ALL	IND,MLD,1.0UH,20%,2.3A,52MOHM,H=0.8,2012

CRITICAL PART#	COMMENT
152S01301	IND,MLD,1.0UH,20%,2.3A,52MOHM,H=0.8,2012



SYNCING: D53, D54

PAGE TITLE	CAMERA: Will
DRAWING NUMBER	051-05215
SIZE	D
REVISION	4.6.0
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WILL DFT_AMUX (ALL)

53 GND

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PAGE TITLE
CAMERA: Will: Aliases

DRAWING NUMBER 051-05215
SIZE D
REVISION 4.6.0
BRANCH
PAGE 118 OF 191
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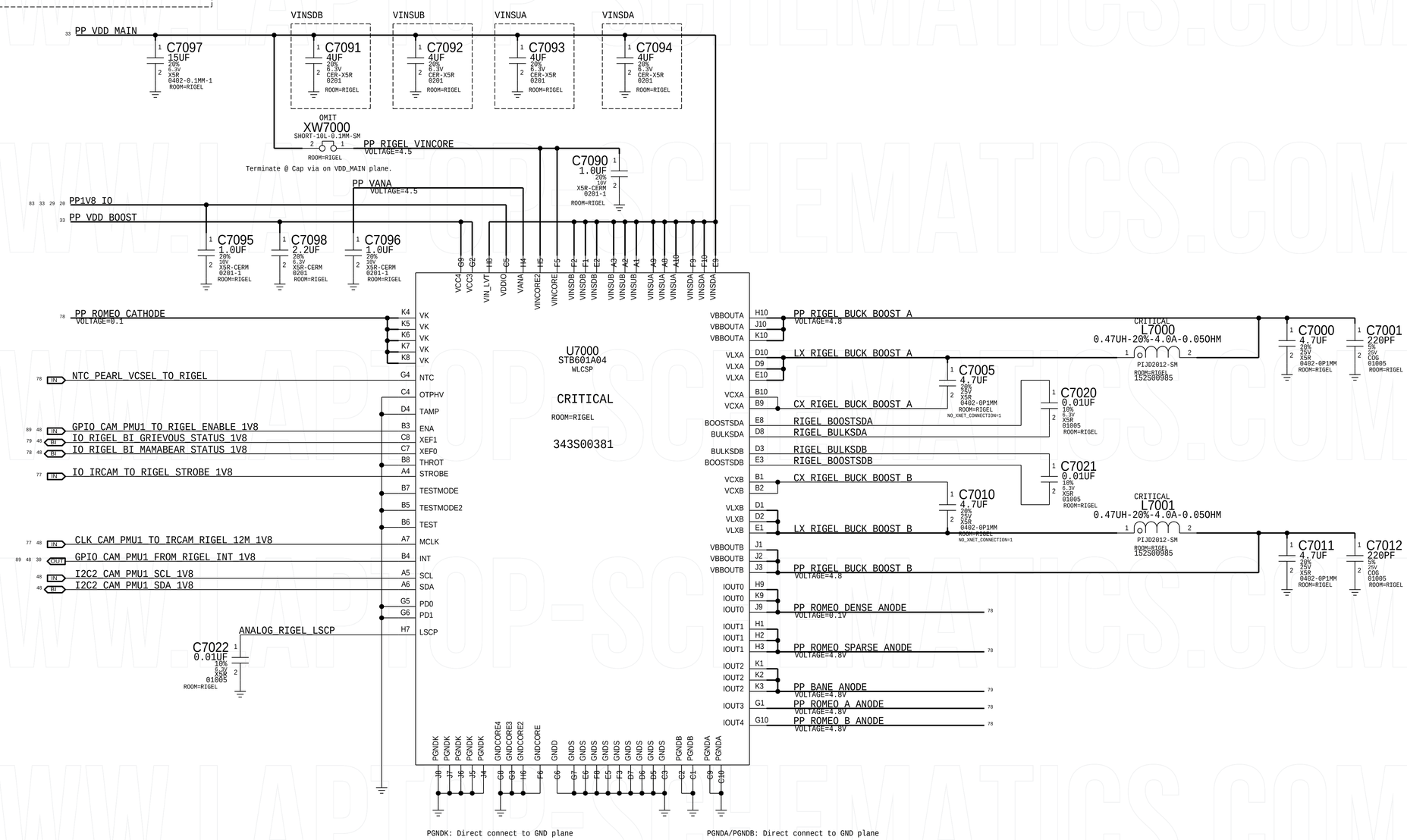
VCSEL DRIVER

RIGEL

SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR: Alt covered with PMU inductor BOM table



PGNDK: Direct connect to GND plane

PGNDA/PGNDB: Direct connect to GND plane

SYNCING: D52, D53, D54

PAGE TITLE	PEARL: VCSEL Driver
DRAWING NUMBER	051-05215
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SYNCING: D52, D53, D54

PAGE TITLE
PEARL: Aliases

DRAWING NUMBER 051-05215
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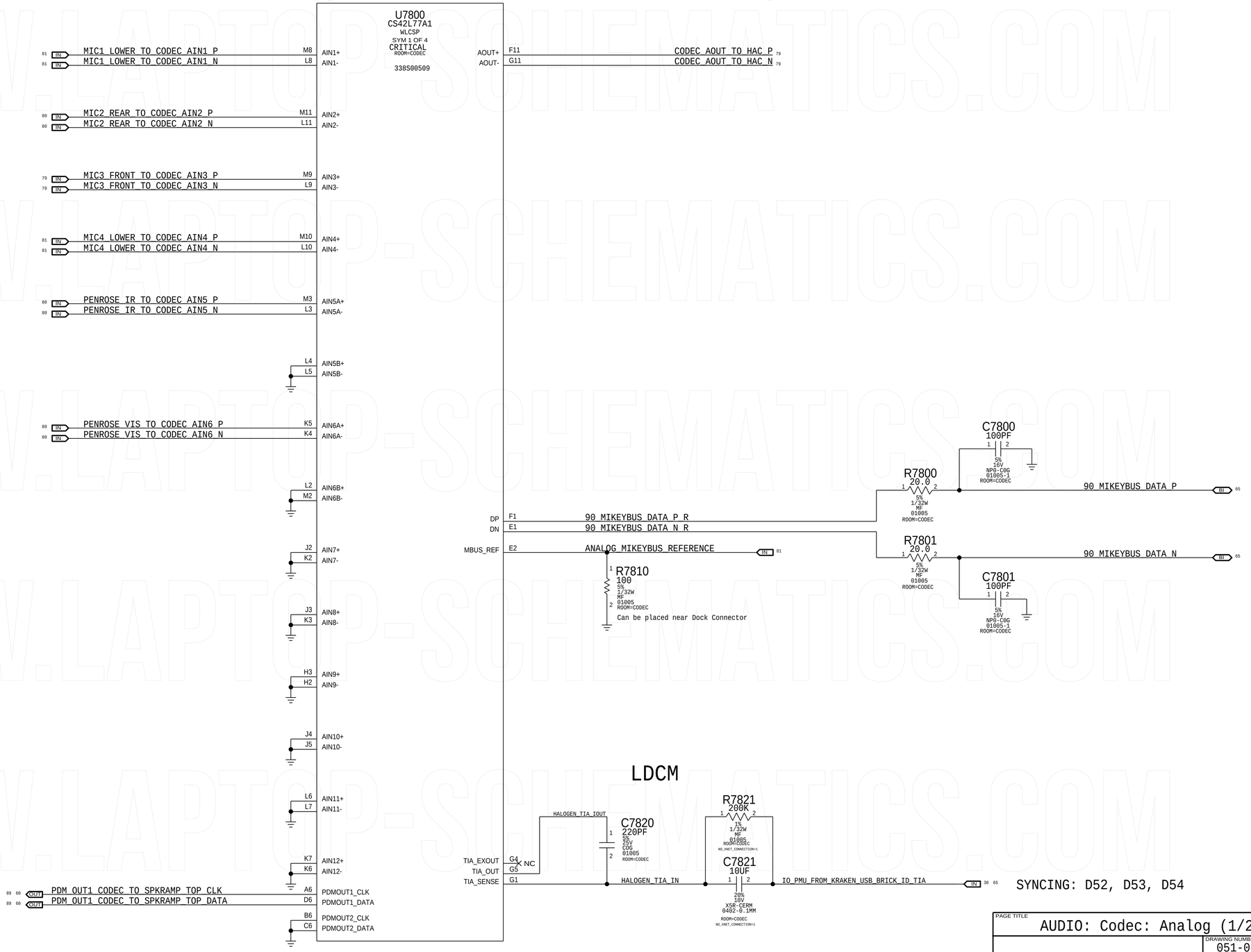
BRIGHTON AUDIO CODEC (ANALOG INPUTS & OUTPUTS)



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PAGE TITLE	AUDIO: Codec: Analog (1/2)
DRAWING NUMBER	051-05215
SIZE	D
REVISION	4.6.0
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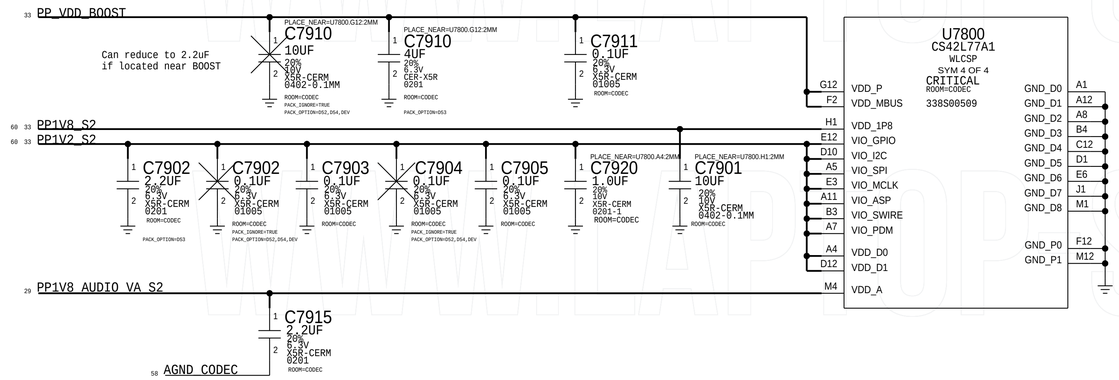
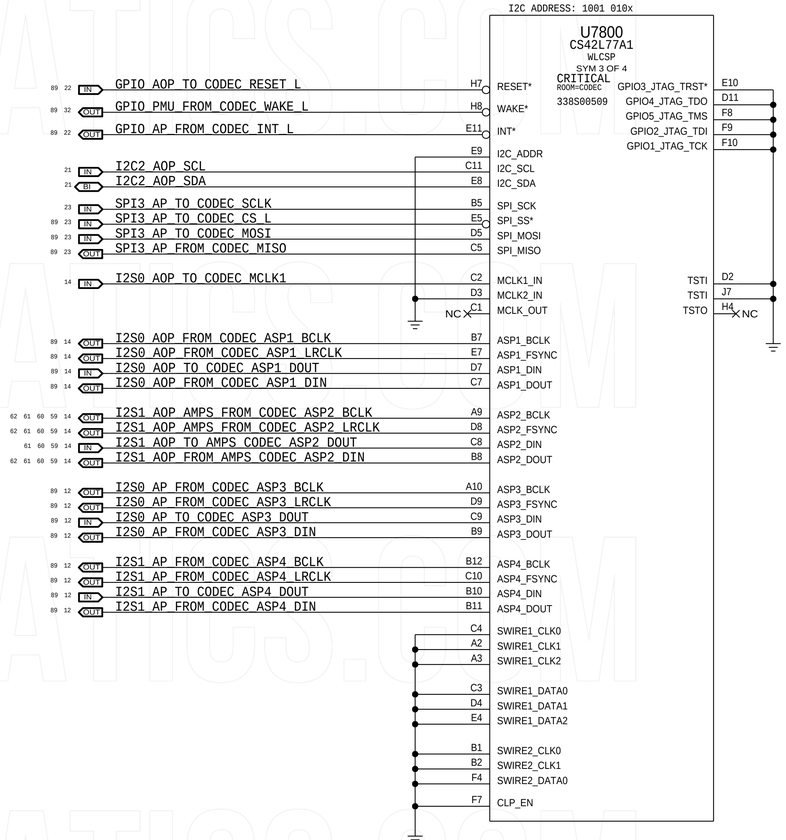
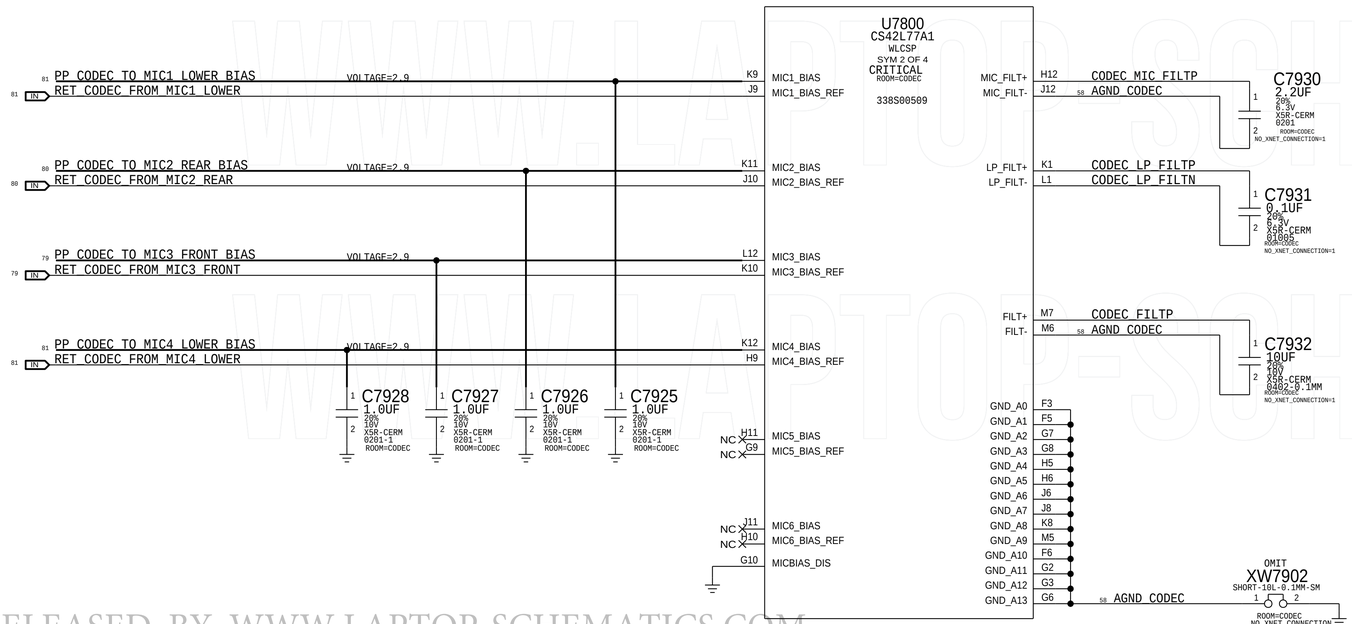
BRIGHTON AUDIO CODEC (POWER & I/O)







SYNCING: D52, D53, D54

PAGE TITLE	AUDIO: Codec: Power & I/O (2/2)
DRAWING NUMBER	051-05215
SIZE	D
REVISION	4.6.0
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BOT SPEAKER AMP

ALLSTON

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POWER DOMAIN NOTES:
1. Use S4 domain if possible, then GND VD_FILT_SEL
2. Can use S2 domain if routing constrained, then NC VD_FILT_SEL

59 33 PP1V2_S4
C8008 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK

33 PP1V8_S4
C8007 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK

PP_VA_BOT_SPK_INTERNAL
VOLTAGE=1.8
C8006 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK
AGND_BOT_SPK 59

59 33 PP1V2_S4

ANALOG_BOT_SPK_FILT
C8009 1.0UF 20% 6.3V X5R 0201-1 ROOM=BOT_SPK NO_XNET_CONNECTION=1
AGND_BOT_SPK 59

U8000
CS35L27A
WLCSP
CRITICAL
338S00537

		VA	H2
		VL	H6
		VD_FILT	H7
		VP	H3
		CF1+	A5
		CF1+	B5
		CF1-	A7
		CF1-	B7
		CF2+	A3
		CF2+	B1
		CF2+	B2
		CF2-	A4
		CF2-	B4
		VBST	C1
		VBST	C2
		VSPK	D1
		VSPK	E1
		OUT+	E2
		OUT-	D2
		VSNS+	F2
		VSNS-	F1
	E7	VASP	
	F7	VSWIRE	
	H1	FILT+	
	F5	PDM1_CLK/SWIRE_CLK	
	F6	PDM1_DATA/SWIRE_SD1	
NC	G7	PDM2_CLK	
	G6	PDM2_DATA	
	F4	SWIRE_SD2	
	D5	SCL	
	D4	SDA	
	E6	MCLK	
	E5	SCLK	
	D6	SDIN	
	D7	FSYNC	
	E4	SDOUT	
	C3	VD_FILT_SEL	
	H4	RESET*	
NC	G4	INT*	
	H5	SYNC	
	G3	AD0/GPI	
	G2	AD1	
	G1	GNDA	
	A6	GNDB	
	B3	GNDB	
	B6	GNDB	
	C4	GNDB	
	G5	GNDD	
	D3	GNDP	
	E3	GNDP	
	F3	GNDP	

ROOM=BOT_SPK

I2C2_AOP_SCL
I2C2_AOP_SDA
I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN

VD_FILT_SEL: NC = internal LDO (use if S2 power domain)
GND = external power (use if S4 power domain)

GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L
IO_SPKRAMP_TO_SPKRAMP_SYNC
GPIO_BT_TO_BOT_SPKR_TRIG

R8050 100K 5% 1/32W MF 01005 ROOM=BOT_SPK

OMIT
XW8000 SHORT-10L-0.1MM-SM
ROOM=BOT_SPK NO_XNET_CONNECTION
AGND_BOT_SPK

Place off of Allston GND pin

Placement Notes:
A1,A2: 15uF (1x), 2.2uF(1x)
C5,C6,C7: 15uF (2x)

PP_VDD_MAIN 33 60 61
C8003 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK
CRITICAL C8000 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK
CRITICAL C8001 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK
CRITICAL C8002 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK
CRITICAL C8004 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK

CX_BOTSPK_P1_POS
CRITICAL C8030 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=BOT_SPK NO_XNET_CONNECTION=1
CX_BOTSPK_P1_NEG

CX_BOTSPK_P2_POS
CRITICAL C8040 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=BOT_SPK NO_XNET_CONNECTION=1
CX_BOTSPK_P2_NEG

VOLTAGE=12.0
PP_SPKRAMP_BOT_VBOOST
CRITICAL C8020 4.2UF 10% 10V X5R-CERM 0402-0.1MM ROOM=BOT_SPK
CRITICAL C8021 4.2UF 10% 10V X5R-CERM 0402-0.1MM ROOM=BOT_SPK
CRITICAL C8022 4.2UF 10% 10V X5R-CERM 0402-0.1MM ROOM=BOT_SPK
C8025 1UF 20% 10V CER-X5R 0201 ROOM=BOT_SPK
C8023 220PF 5% 25V C0G 01005 ROOM=BOT_SPK
C8024 2200PF 10% 16V X5R-CERM 01005 ROOM=BOT_SPK

SPKRAMP_BOT_TO_COIL_OUT_POS 61
SPKRAMP_BOT_TO_COIL_OUT_NEG 61
COIL_TO_SPKRAMP_BOT_VSENSE_POS 61
COIL_TO_SPKRAMP_BOT_VSENSE_NEG 61

SYNCING: D52, D53, D54

PAGE TITLE	AUDIO: Bot Speaker Amp
DRAWING NUMBER	051-05215
SIZE	D
REVISION	4.6.0
BRANCH	
PAGE	123 OF 191
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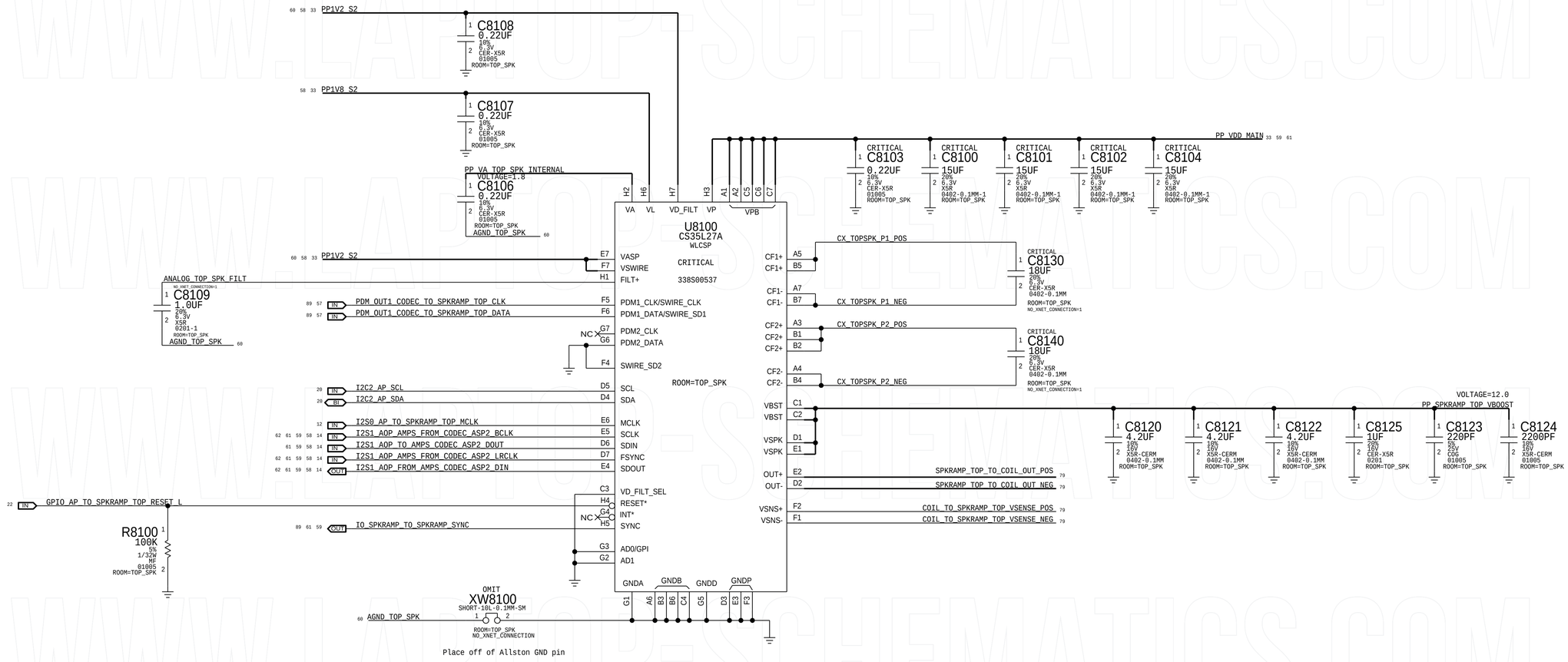
TOP SPEAKER AMP

ALLSTON



SYNCING: D52, D53, D54

PAGE TITLE	AUDIO: Top Speaker Amp
DRAWING NUMBER	051-05215
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ARC SPEAKER AMP

ALLSTON

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PLACEMENT NOTES:
C8308: Place near VD_FILT
C8307: Place near VL
C8306: Place near VA

61 PP1V2_ARCAMP_VD_FILT_INTERNAL VOLTAGE=1.2

C8308 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

61 PP1V8_ARCAMP_VA_VL_INTERNAL VOLTAGE=1.8

C8307 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

C8306 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

AGND_ARCAMP

PLACEMENT NOTES:
A1,A2: 15uF (1x), 2.2uF(1x)
C5,C6,C7: 15uF (3x)

C8303 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

CRITICAL C8300 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

CRITICAL C8301 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

CRITICAL C8302 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

CRITICAL C8304 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

PP_VDD_MAIN 33 59 60

61 H2 H6 H7 H3 A1 A2 C5 C6 C7

VA VL VD_FILT VP VPB

U8300
CS35L27A
WLCSP
CRITICAL
338S00537

61 PP1V2_ARCAMP_VD_FILT_INTERNAL → E7 VASP
F7 VSWIRE
H1 FILT+

ANALOG_ARCAMP_FILT

C8309 1.0UF 20% 6.3V X5R 0201-1 ROOM=ARC

AGND_ARCAMP 61 NO_XNET_CONNECTION=1

F5 PDM1_CLK/SWIRE_CLK
F6 PDM1_DATA/SWIRE_SD1
NC G7 PDM2_CLK
G6 PDM2_DATA
F4 SWIRE_SD2

21 IN I2C2_AOP_SCL → D5 SCL
21 BI I2C2_AOP_SDA → D4 SDA

ROOM=ARC

59 14 IN I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK → E6 MCLK
62 60 59 58 14 IN I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK → E5 SCLK
60 59 58 14 IN I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT → D6 SDIN
62 60 59 58 14 IN I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK → D7 FSYNC
62 60 59 58 14 OUT I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN → E4 SDOUT

VDD_FILT_SEL: NC = Internal VD_FILT LDO

NC C3 VD_FILT_SEL
H4 RESET*
NC G4 INT*
89 60 59 OUT IO_SPKRAMP_TO_SPKRAMP_SYNC → H5 SYNC
Option to remove SYNC connection

G3 AD0/GPI
61 PP1V8_ARCAMP_VA_VL_INTERNAL → G2 AD1

GNDA GNDB GNDD GNDP
G1 A6 B3 B6 C4 G5 D3 E3 F3

OMIT
XW8300
SHORT-10L-0.1MM-SM
61 AGND_ARCAMP 1 2
ROOM=ARC
NO_XNET_CONNECTION

Place off of Allston GND pin

CF1+ A5 CF1+ B5 ← CX_ARCAMP_P1_POS
CF1- A7 CF1- B7 ← CX_ARCAMP_P1_NEG

CRITICAL C8330 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC NO_XNET_CONNECTION=1

CF2+ A3 CF2+ B1 CF2+ B2 ← CX_ARCAMP_P2_POS
CF2- A4 CF2- B4 ← CX_ARCAMP_P2_NEG

CRITICAL C8340 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC NO_XNET_CONNECTION=1

VOLTAGE=12.0
PP_ARCAMP_VBOOST

VBST C1 VBST C2

CRITICAL C8320 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC

CRITICAL C8321 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC

CRITICAL C8322 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC

C8325 1UF 20% 10V CER-X5R 0201 ROOM=ARC

C8323 220PF 5% 25V C0G 01005 ROOM=ARC

C8324 2200PF 10% 16V X5R-CERM 01005 ROOM=ARC

VSPK D1 VSPK E1

OUT+ E2 → ARCAMP_TO_SOLENOID_OUT_POS 81
OUT- D2 → ARCAMP_TO_SOLENOID_OUT_NEG 81

VSNS+ F2 → SOLENOID_TO_ARCAMP_VSENSE_POS 81
VSNS- F1 → SOLENOID_TO_ARCAMP_VSENSE_NEG 81

99 IN GPIO_NFC_TO_ARCAMP_RESET_L

R8300 61.9K 1% 1/32W MF 01005 ROOM=ARC

32 IN GPIO_PMU_NFC_TO_ARCAMP_RESET_L

See Radar # 50911384 for R8300/R8301 values

32 IN GPIO_PMU_NFC_TO_ARCAMP_TRIG

99 IN GPIO_NFC_TO_ARCAMP_TRIG

R8301 61.9K 1% 1/32W MF 01005 ROOM=ARC

R8310 200K 1% 1/32W MF 01005 ROOM=ARC

R8311 200K 1% 1/32W MF 01005 ROOM=ARC

SYNCING: D52, D53, D54

PAGE TITLE
HAPTIC: Haptic Amp

DRAWING NUMBER 051-05215
SIZE D
REVISION 4.6.0
BRANCH
PAGE 125 OF 191
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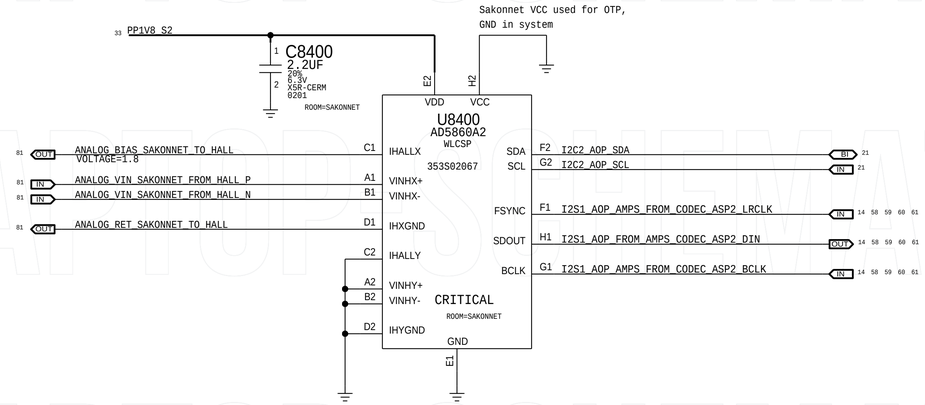
HALL SENSOR

SAKONNET



SYNCING: D52, D53, D54

PAGE TITLE	HAPTIC: Sakonnet
DRAWING NUMBER	051-05215
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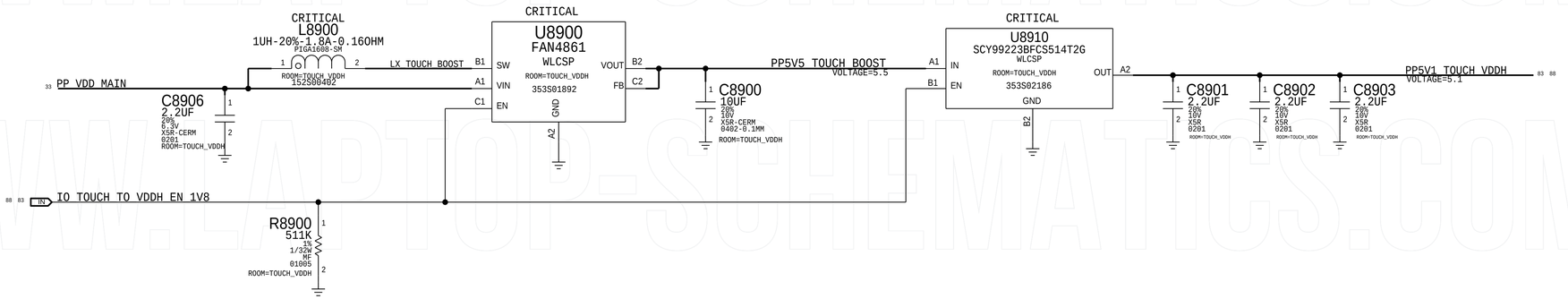
TOUCH

TOUCH POWER

SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00366	152S00402	?	ALL	IND,PWR,1.0UH,20%,1.6A,160MOHM,TAIYO,1608



SYNCING: D53

PAGE TITLE	TOP MODULE: Touch Power
DRAWING NUMBER	051-05215
SIZE	D
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DISPLAY PMIC

GALENA/CHELAN

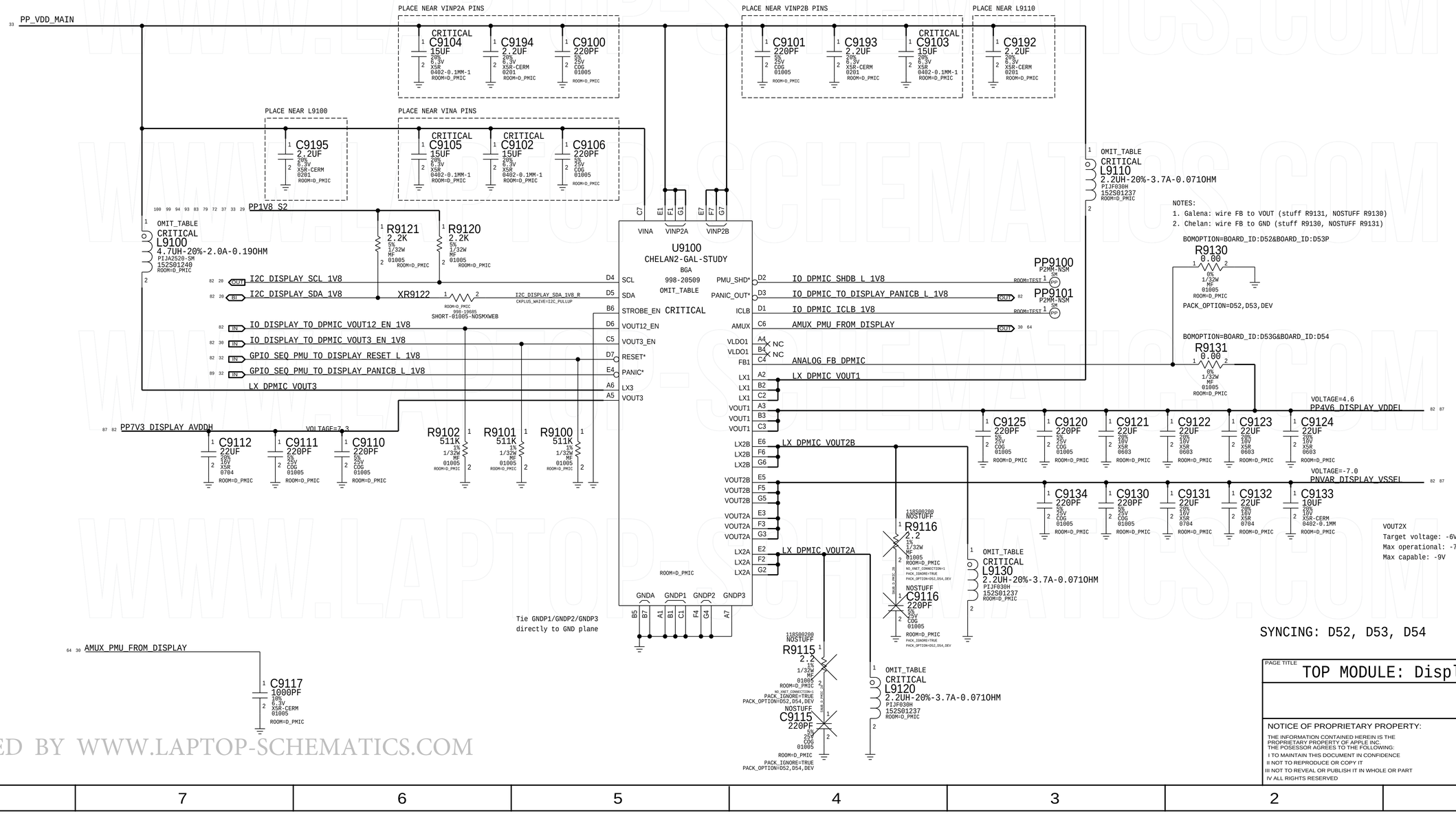
Galena/Chelan

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00655	1	Galena A2 OTP-1	U9100	CRITICAL	BOARD_ID:D53G&BOARD_ID:D54
338S00578	1	Chelan	U9100	CRITICAL	BOARD_ID:D52&BOARD_ID:D53P

Inductors

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S01355	1	Cyntec VOUT3 Inductor (6.8uH 2520 0.95mm)	L9100	CRITICAL	BOARD_ID:D52
152S01347	1	Cyntec VOUT3 Inductor (6.8uH 2520 1.0mm)	L9100	CRITICAL	BOARD_ID:D53P
152S01313	1	Cyntec VOUT3 Inductor (4.7uH 2520 1.0mm)	L9100	CRITICAL	BOARD_ID:D53G&BOARD_ID:D54
152S01237	3	Cyntec VOUT1/2 Inductor (2.2uH 3030 0.8mm)	L9110	CRITICAL	BOARD_ID:D52
152S01357	3	Cyntec VOUT1/2 Inductor (2.2uH 3030 0.95mm)	L9120, L9130	CRITICAL	BOARD_ID:D52
152S01314	3	Cyntec VOUT1/2 Inductor (2.2uH 3030 1.0mm)	L9110, L9120, L9130	CRITICAL	BOARD_ID:D53G&BOARD_ID:D53P&BOARD_ID:D54

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01356	152S01355	BOARD_ID:D52	L9100	Taiyo 6.8uH 2520 0.95mm
152S01346	152S01347	BOARD_ID:D53P	L9100	Taiyo 6.8uH 2520 1.0mm
152S01339	152S01313	BOARD_ID:D53G&BOARD_ID:D54	L9100	Taiyo 4.7uH 2520 1.0mm
152S01290	152S01237	BOARD_ID:D52	L9110	Taiyo 2.2uH 3030 0.8mm
152S01358	152S01357	BOARD_ID:D52	L9120,L9130	Taiyo 2.2uH 3030 0.95mm
152S01340	152S01314	BOARD_ID:D53G&BOARD_ID:D53P&BOARD_ID:D54	L9110,L9120,L9130	Taiyo 2.2uH 3030 1.0mm



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PAGE TITLE: TOP MODULE: Display Power

DRAWING NUMBER: 051-05215 | SIZE: D

REVISION: 4.6.0

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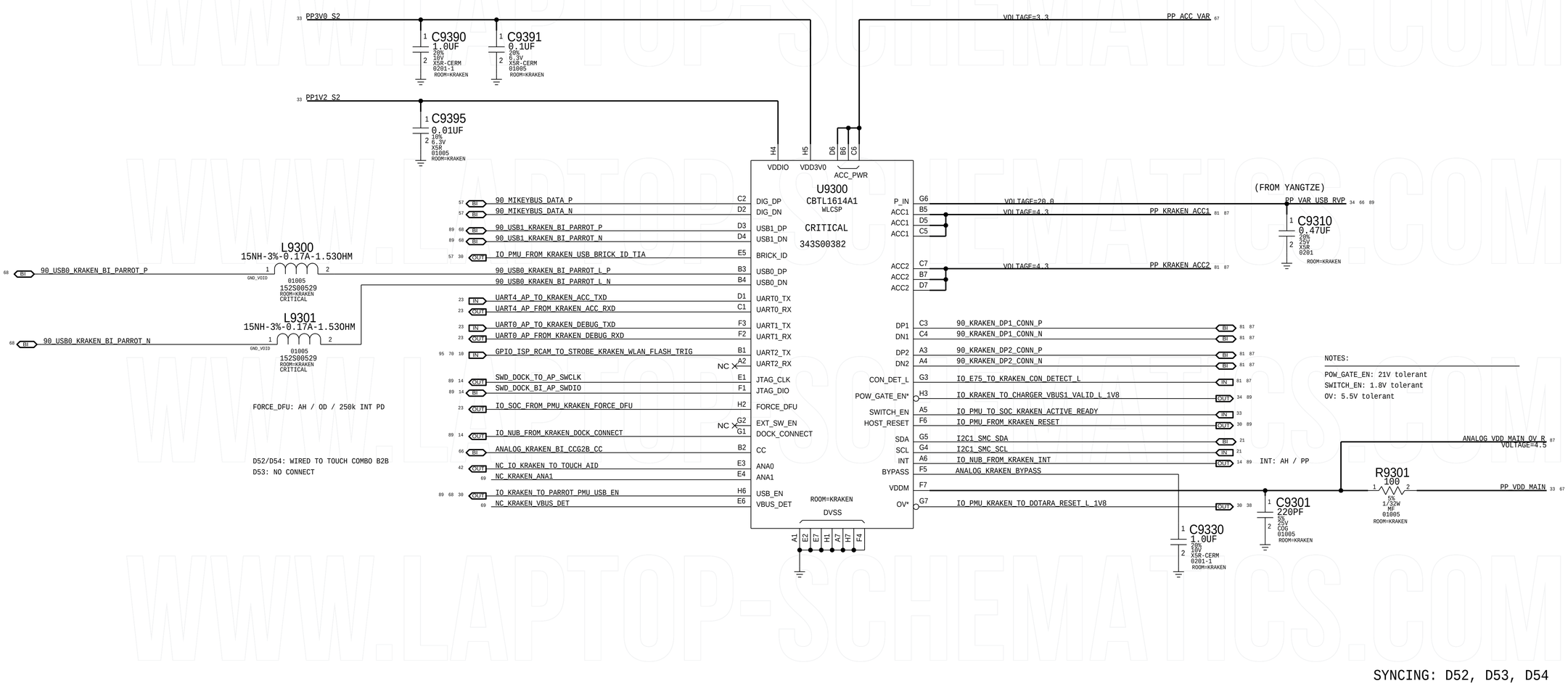
SUBSYSTEM SPECIFIC BOM TABLES

LIGHTNING CONTROLLER

KRAKEN

I2C Address: 0011010X



SYNCING: D52, D53, D54

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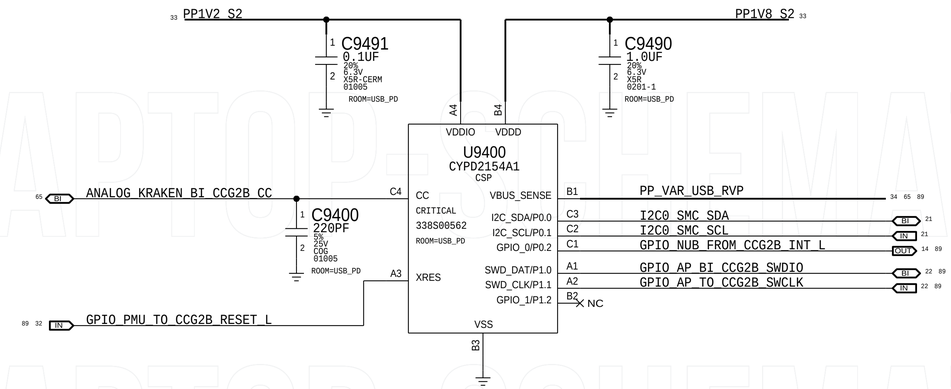
USB-PD

CCG2B



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ACCESSORY POWER

GECKO2

SUBSYSTEM SPECIFIC BOM TABLES

Inductor

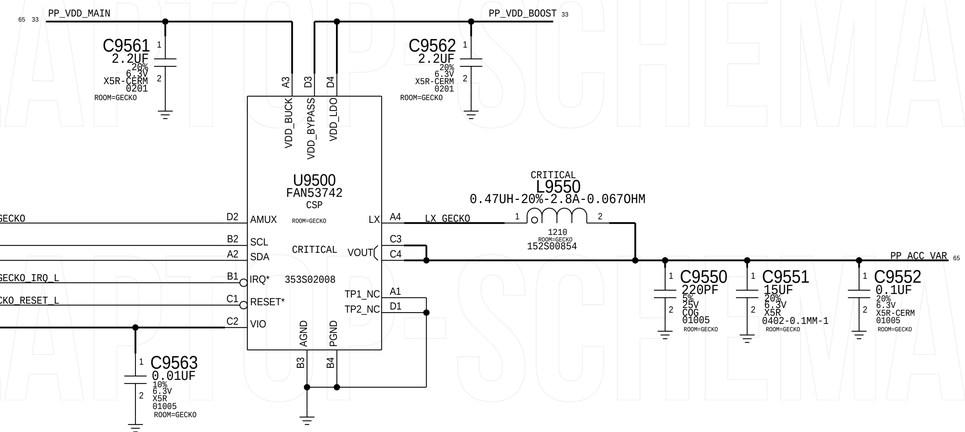
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01279	152S00854	?	L9550	IND,PWR,0.47UH,20%,2.7A,TY

Output Capacitor (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C9551)	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

I2C ADDRESS: 0X52



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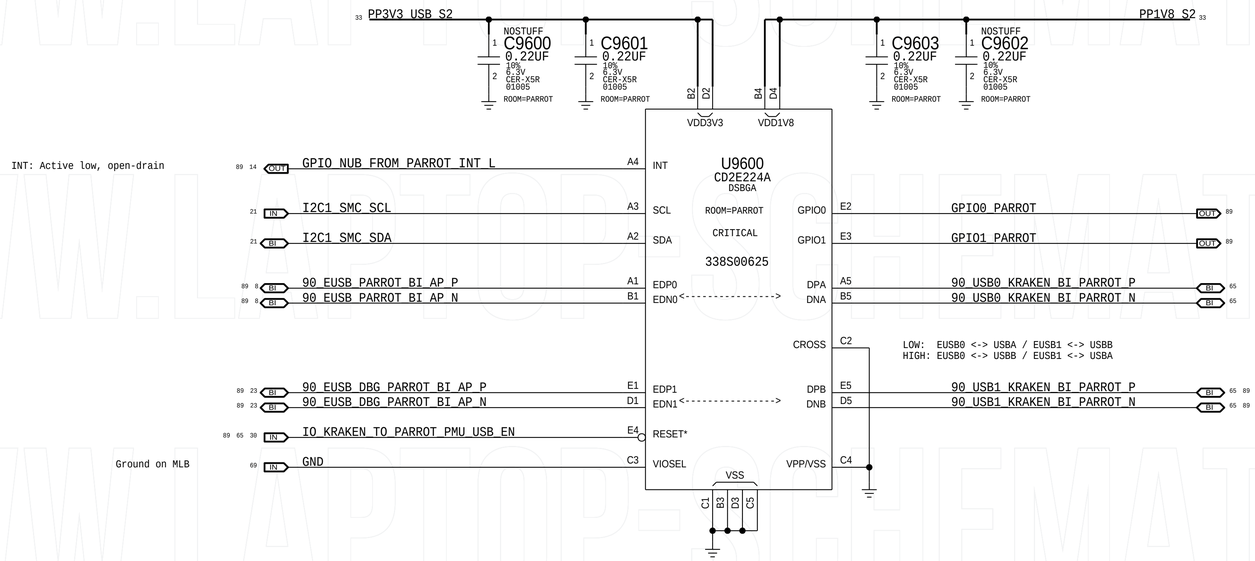
USB REPEATER

PARROT

[LAYOUT] Parrot layout guidelines:
1. 3.3V power pins are shorted together internally, as are 1.8V pins
2. Keep decoupling cap <3mm from power pin
3. Minimize coupling between 1.8V and 3.3V rails



PLACE PARROT NEAR SOC

SYNCING: D52, D53, D54, DEV

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65 NC_KRAKEN_VBUS_DET = NC_KRAKEN_VBUS_DET
MAKE_BASE=TRUE
NO_TEST=1

65 NC_KRAKEN_ANA1 = NC_KRAKEN_ANA1
MAKE_BASE=TRUE
NO_TEST=1

68 GND
LOW: 1.2V IO / HIGH: 1.8V IO

SYNCING: D52, D53, D54

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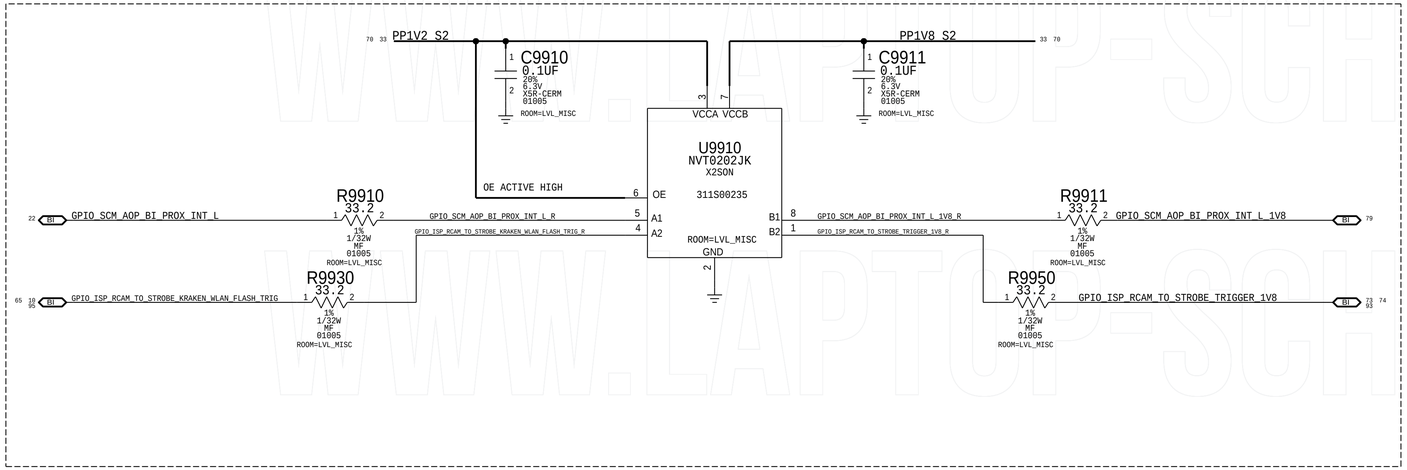
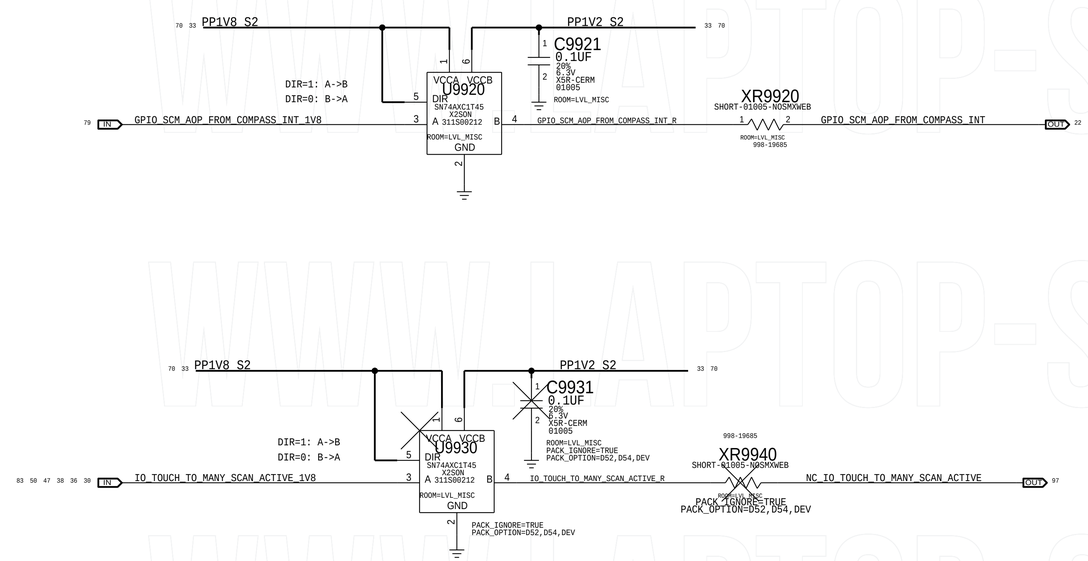
MISCELLANEOUS LEVEL TRANSLATORS

PROX INTERRUPT + STROBE TRIGGER



TOUCH SCAN ACTIVE + COMPASS INTERRUPT



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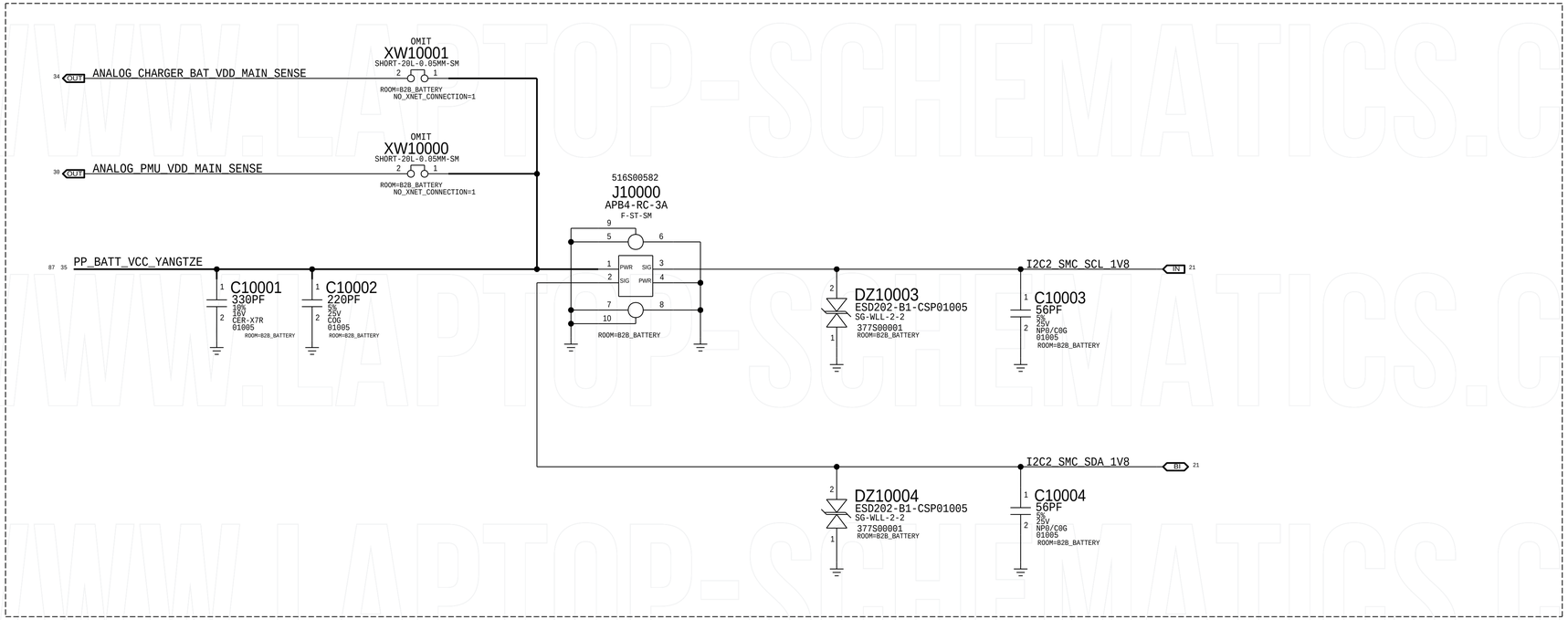
BATTERY B2B

BATTERY CONNECTOR



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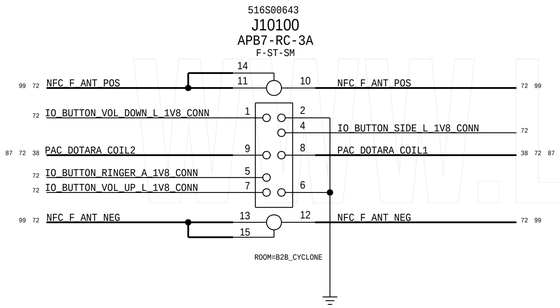
Cyclone B2B

CONNECTOR



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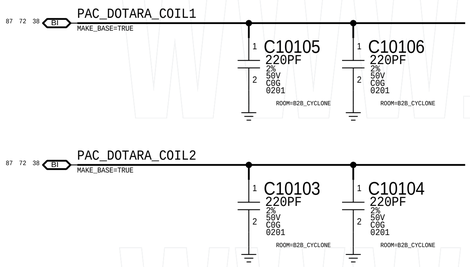

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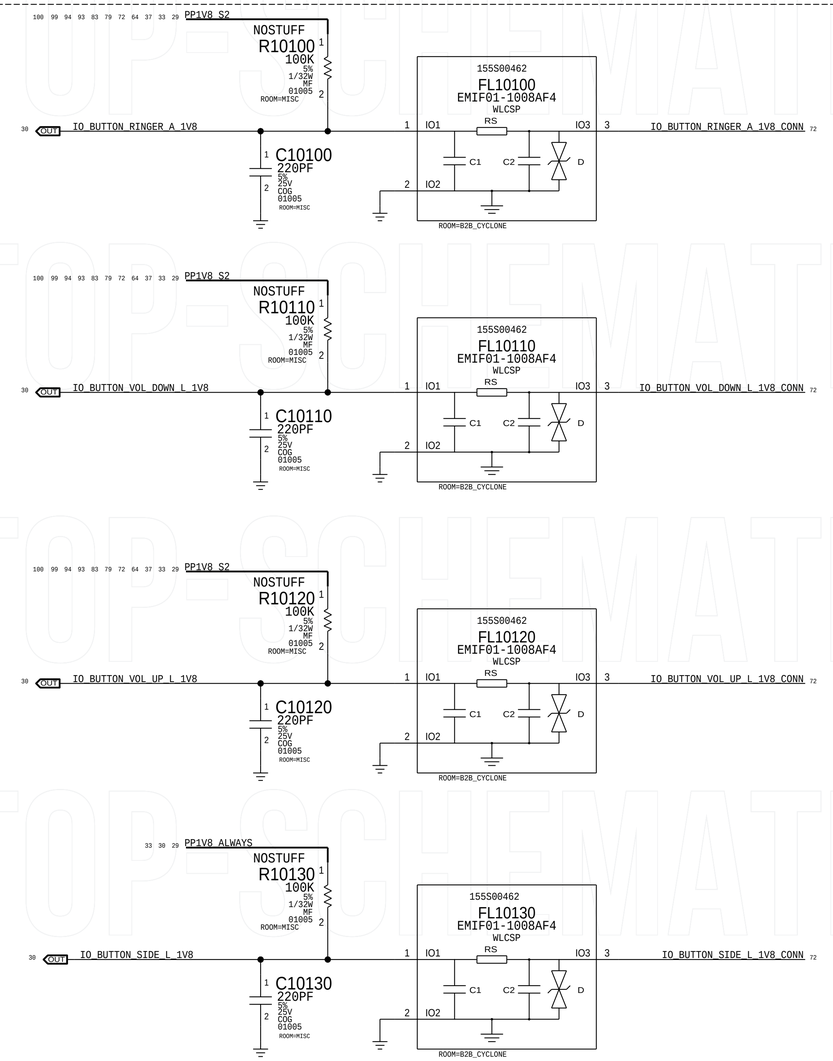

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SINGLE-FLEX CAMERA B2B

See page 52 for details

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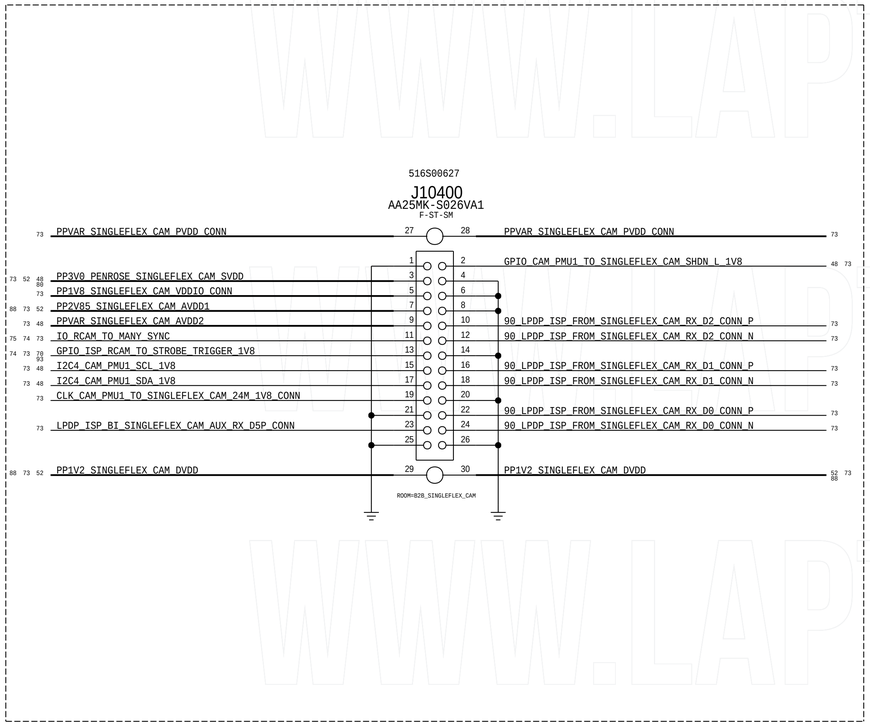

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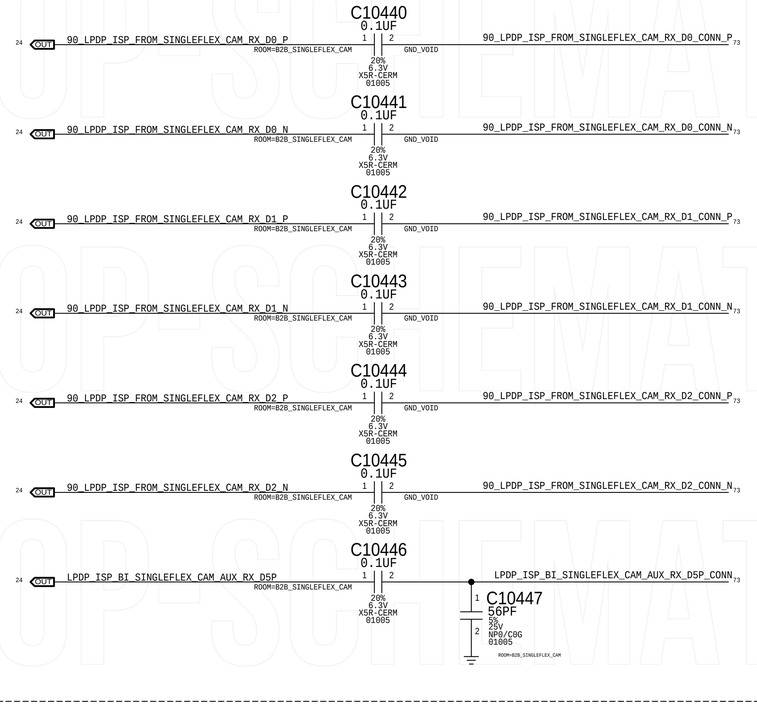

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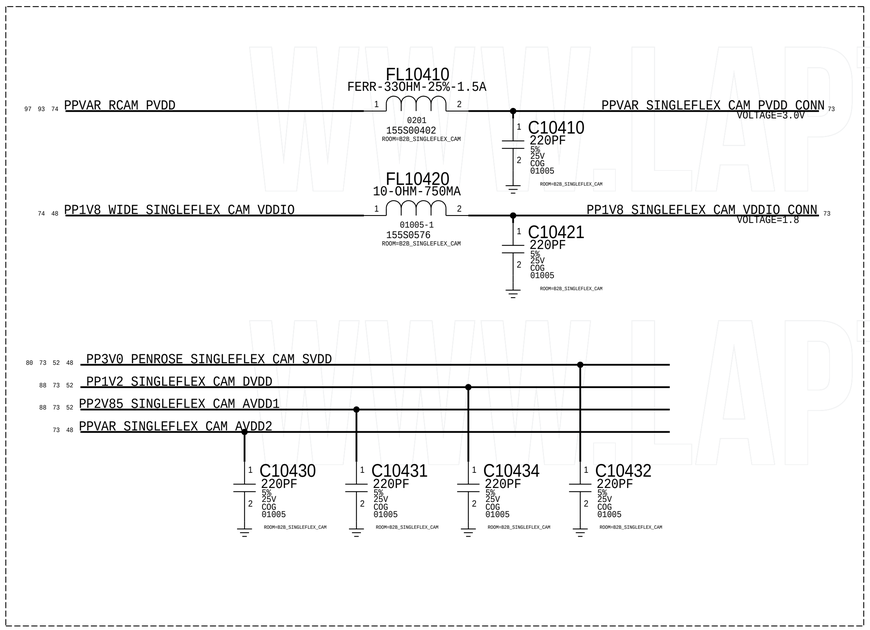

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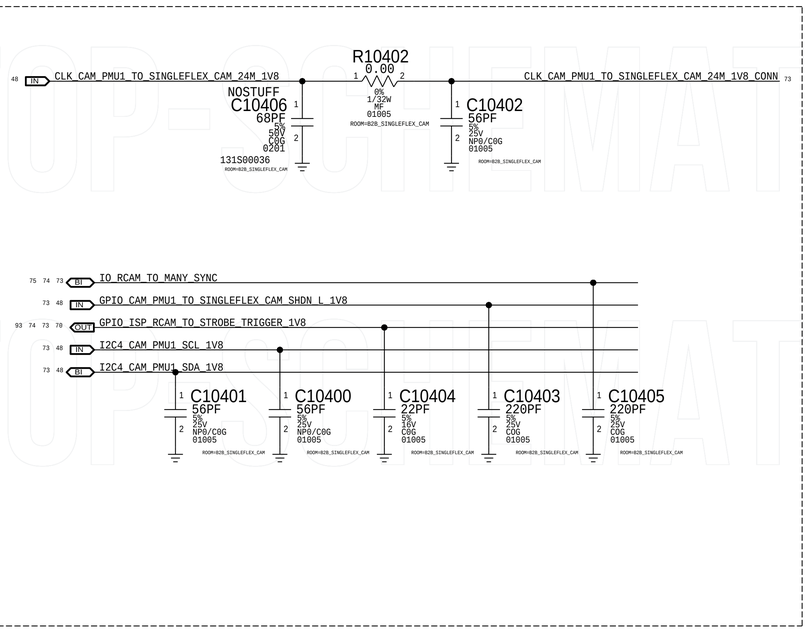

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SUPER-FLEX B2B

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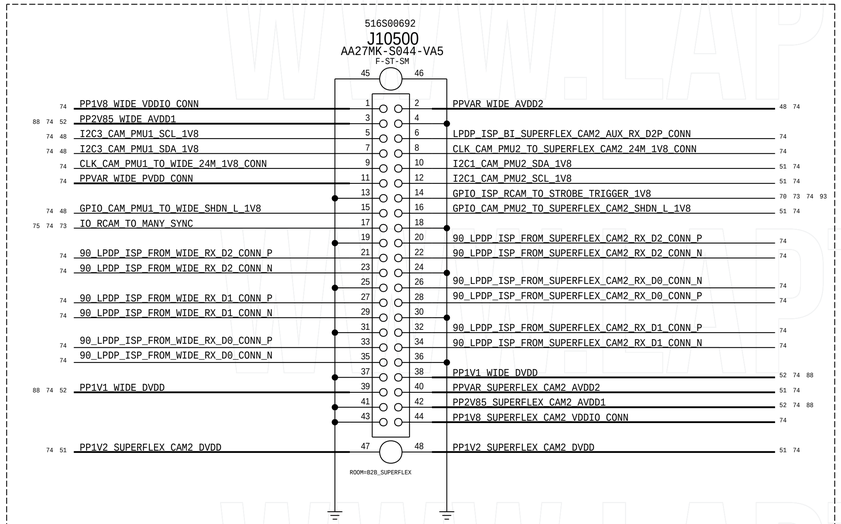

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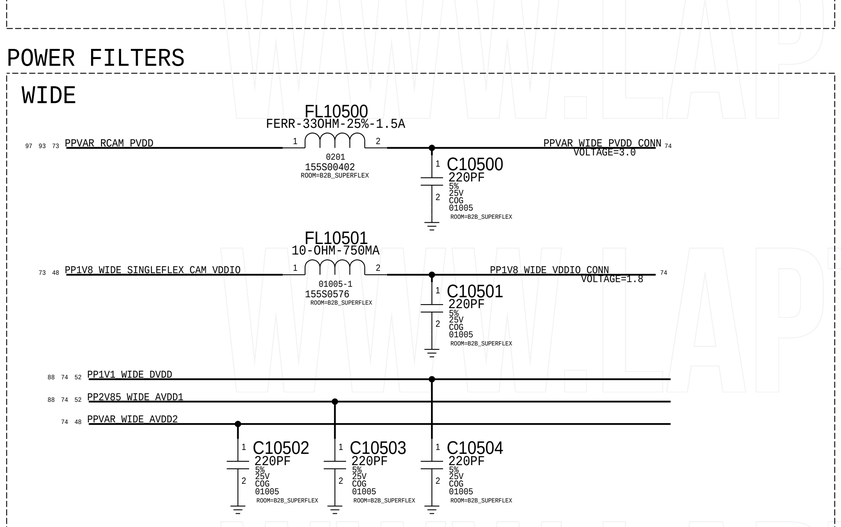

SUPERFLEX-CAM2

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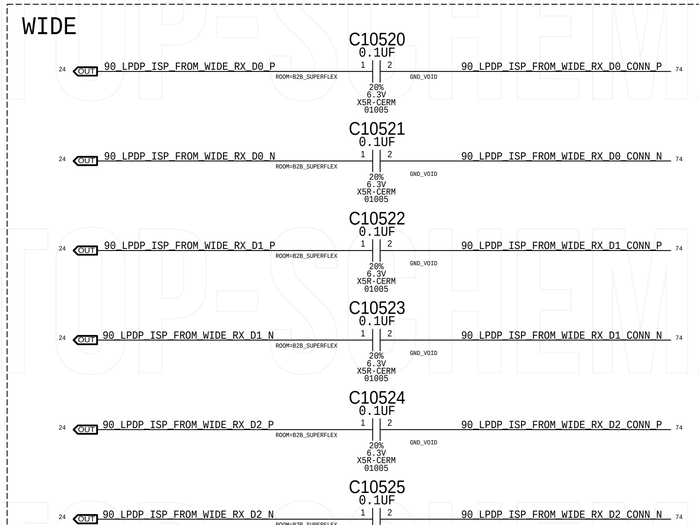

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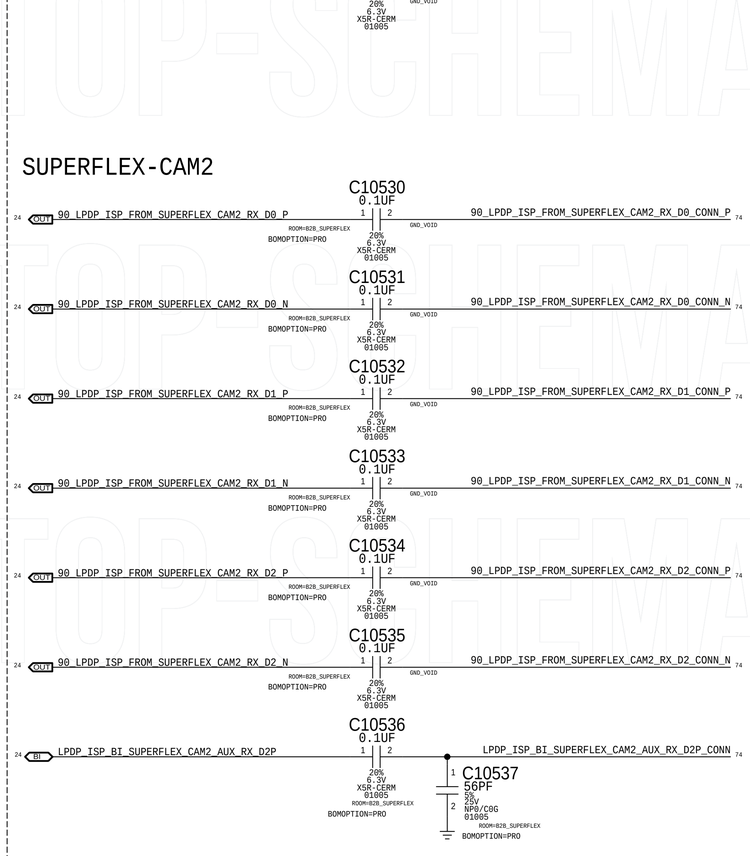

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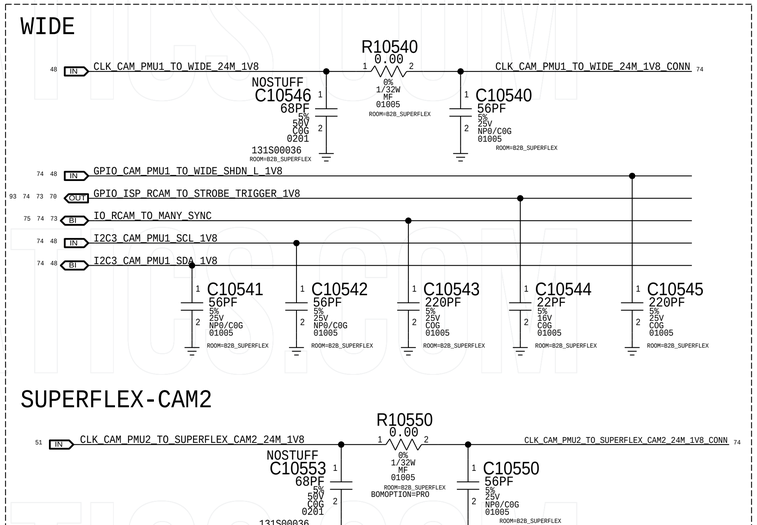

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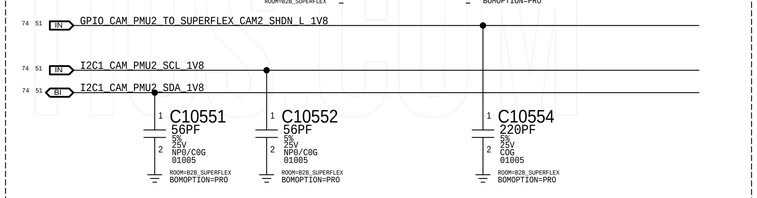

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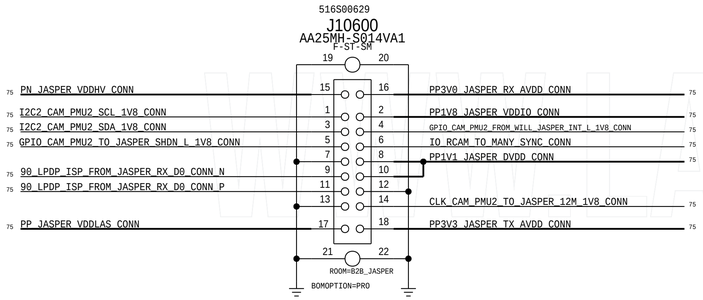
JASPER CAMERA B2B

JASPER CONNECTOR



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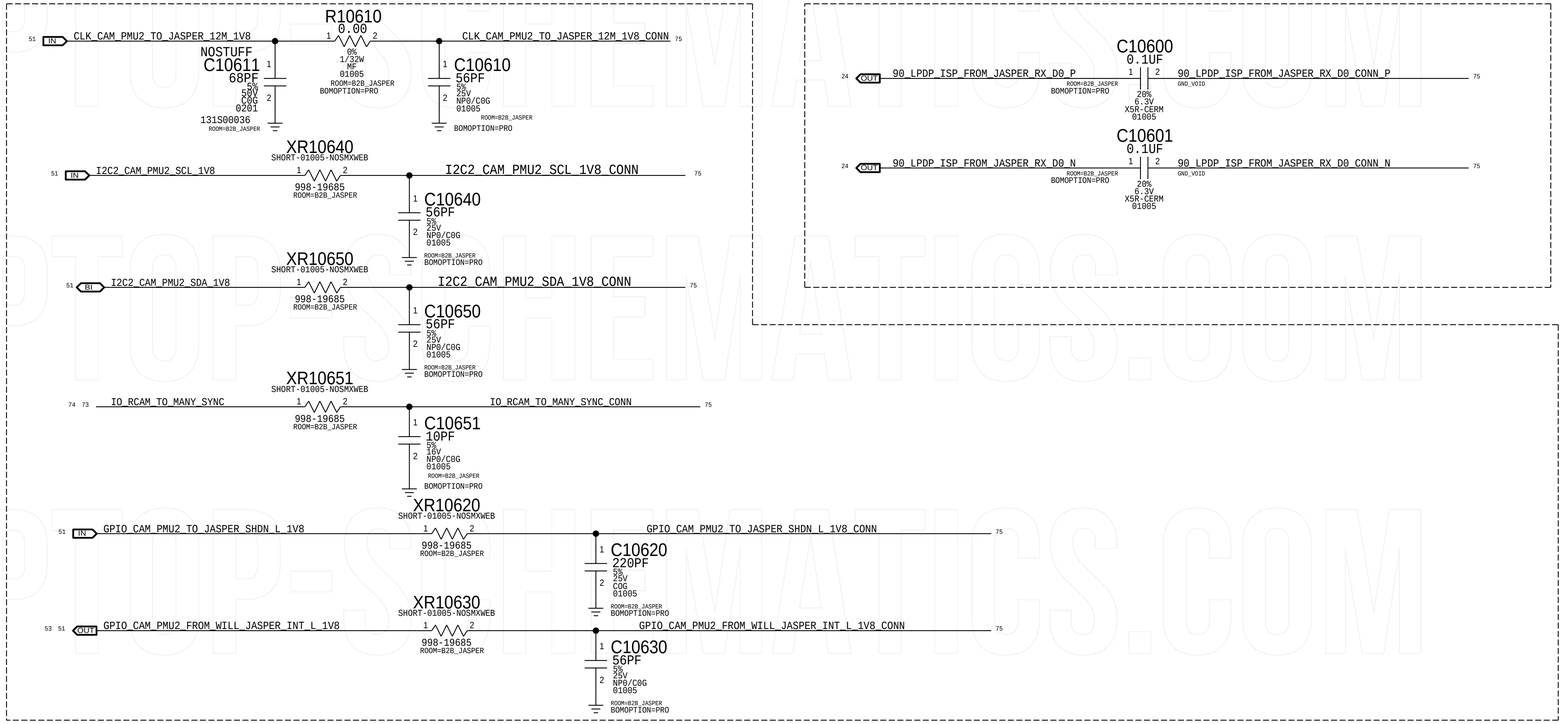

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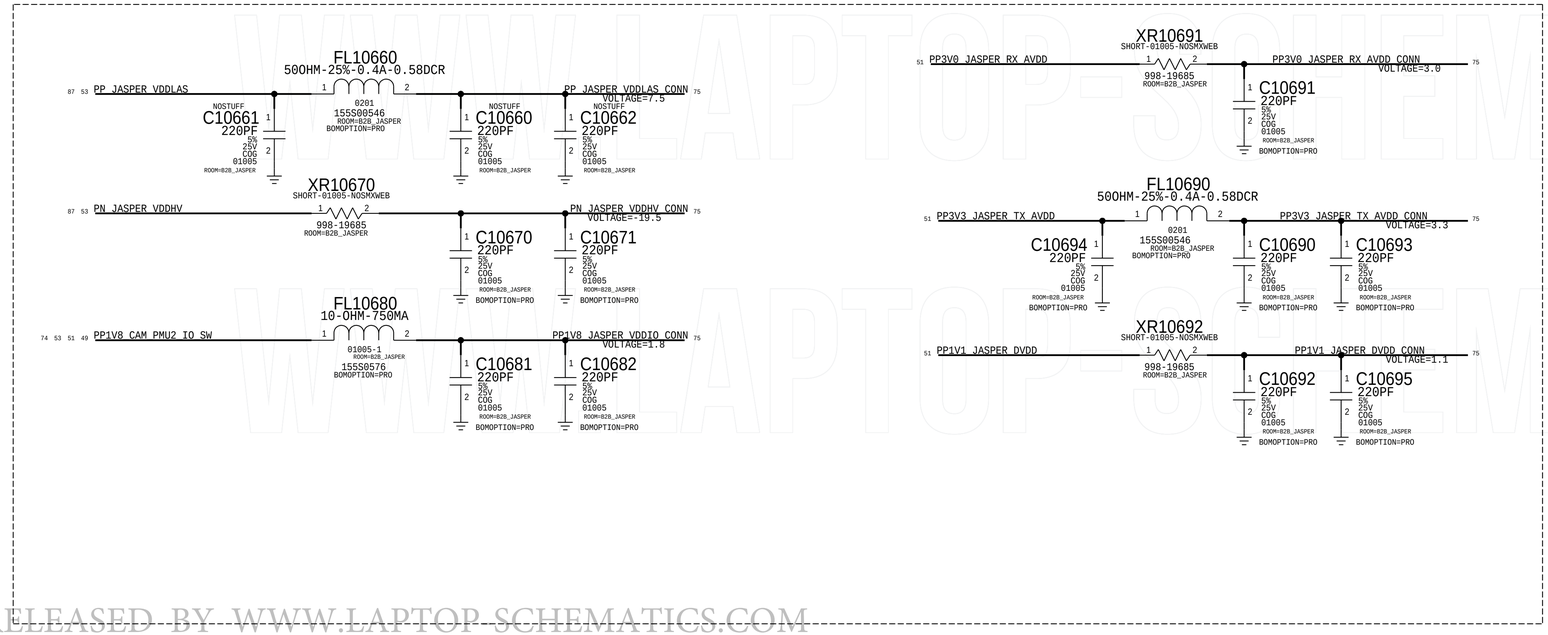
POWER FILTERS



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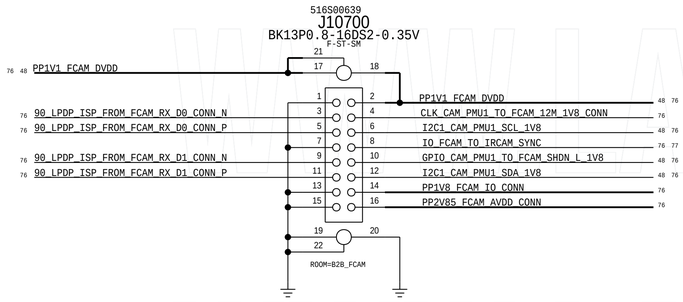
FCAM B2B

CONNECTORS



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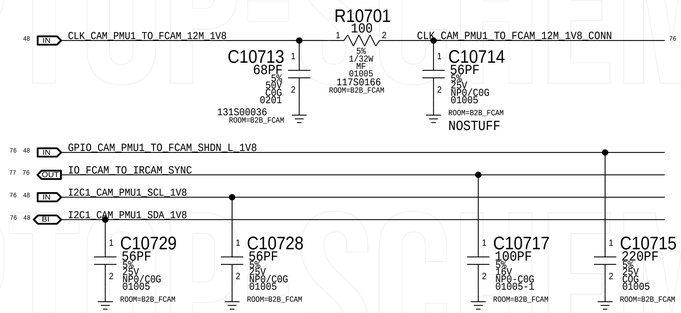

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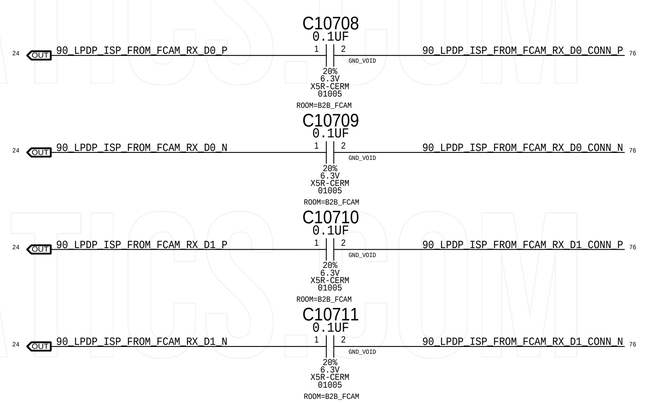

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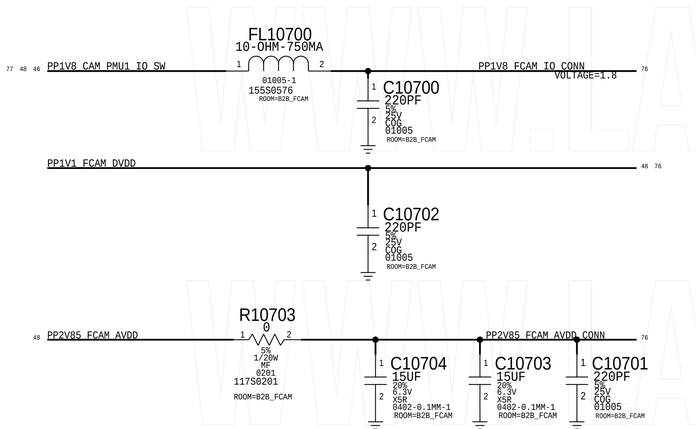

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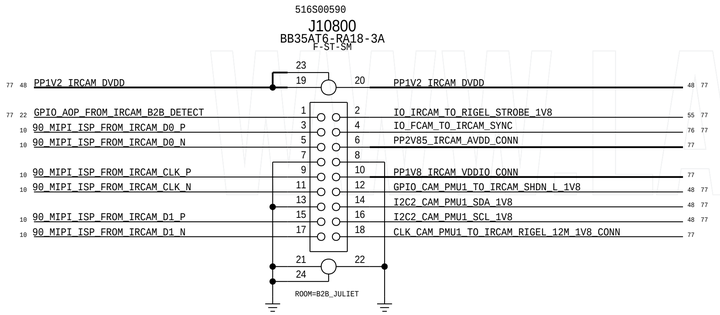
JULIET B2B

CONNECTOR



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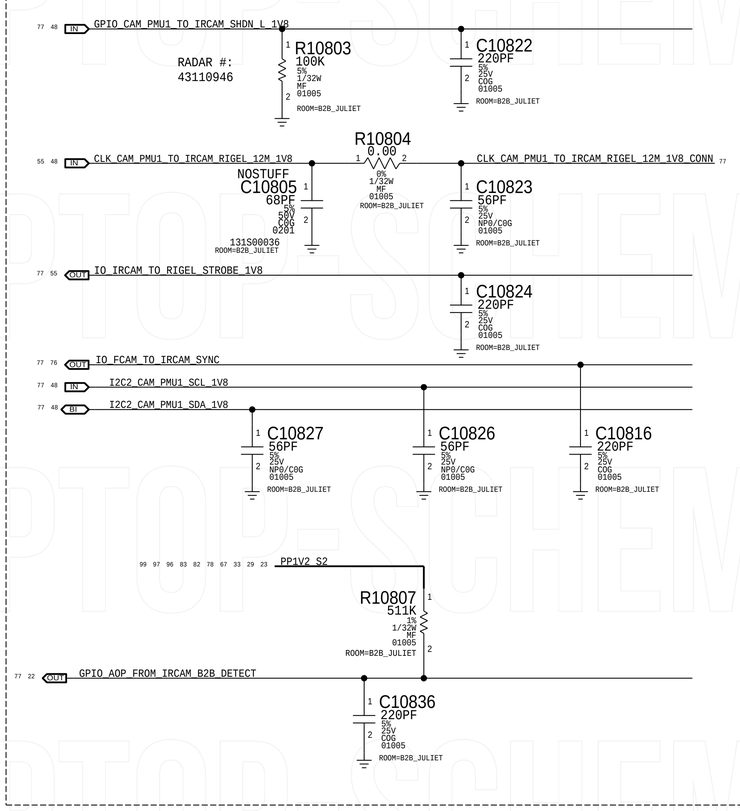

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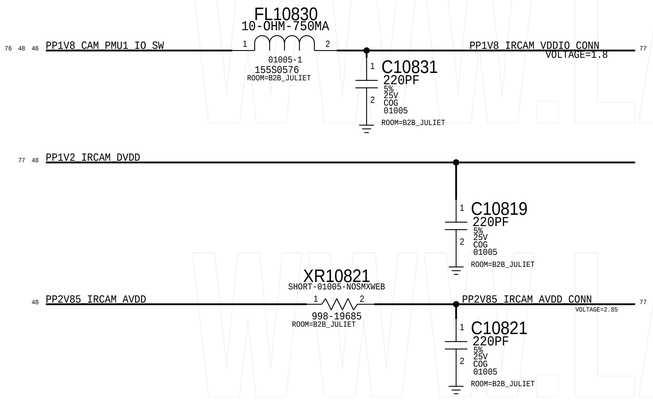

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PAGE TITLE
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ROMEO B2B

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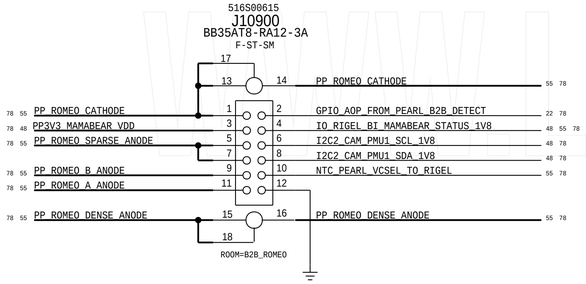

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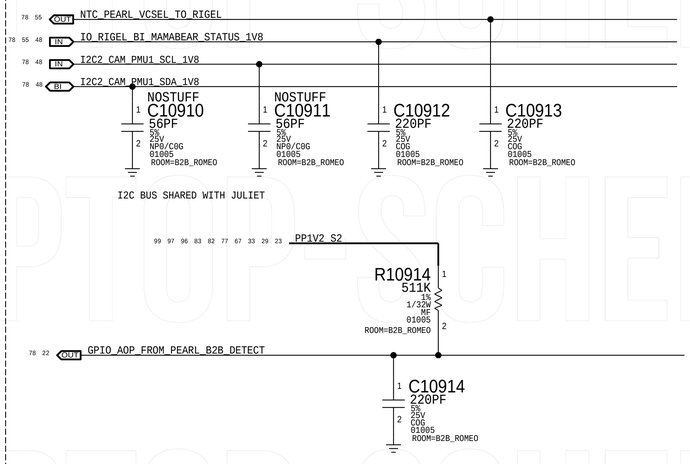

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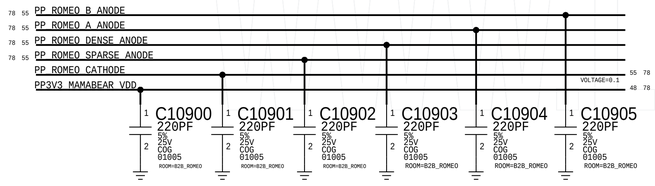

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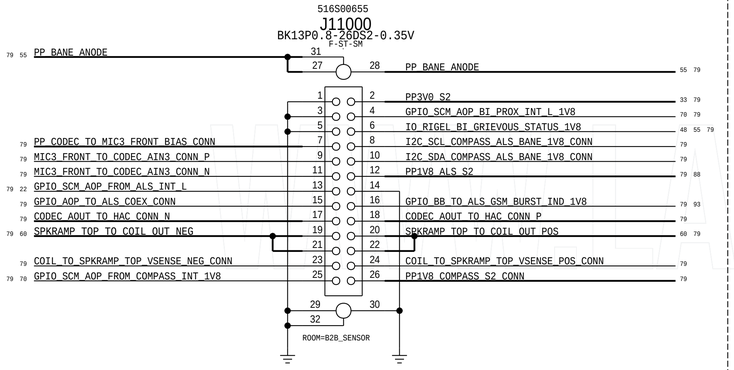

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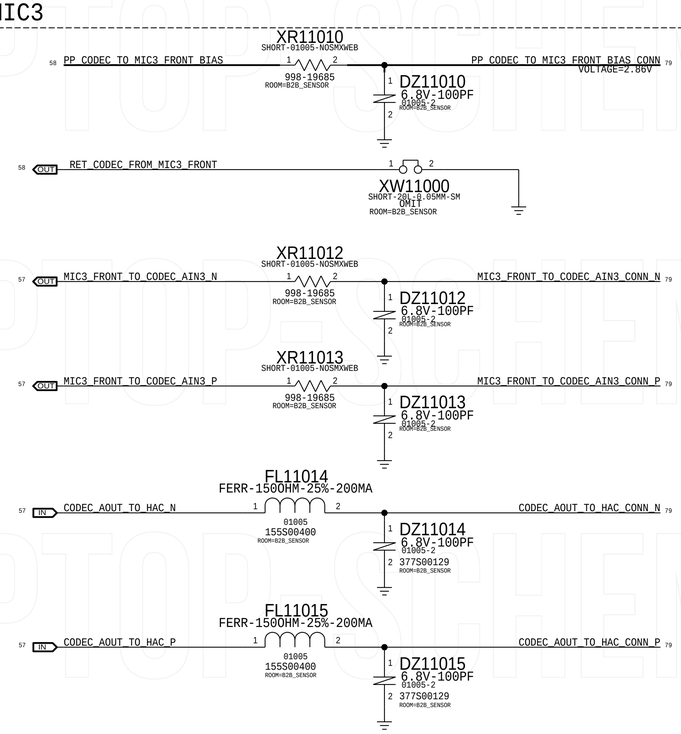

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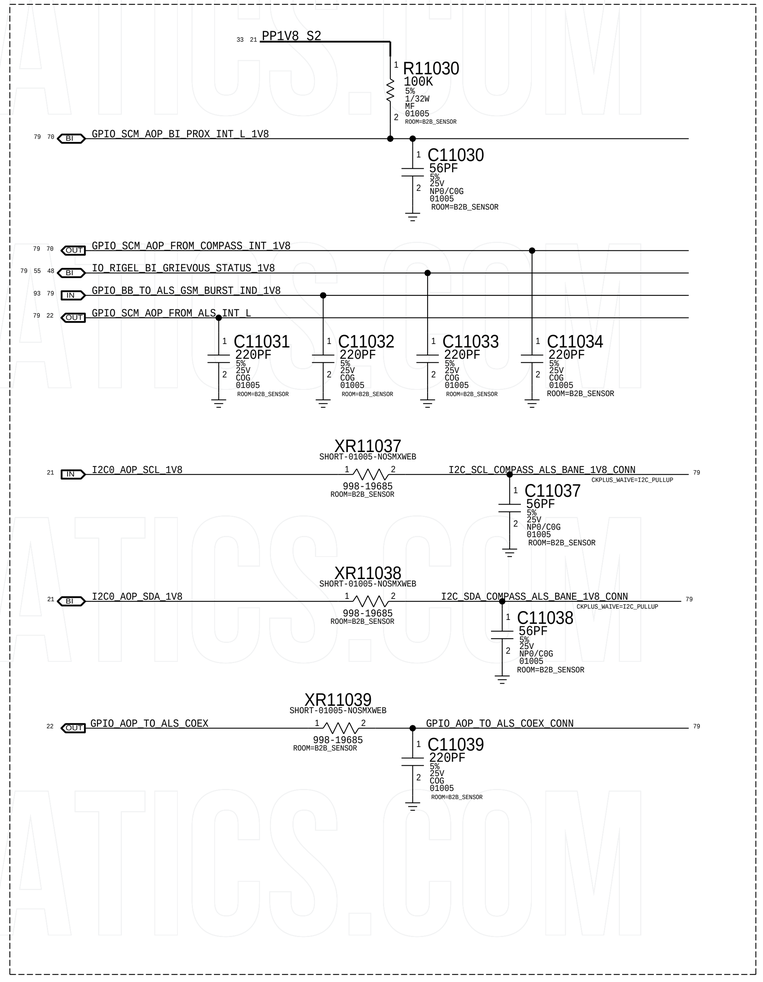

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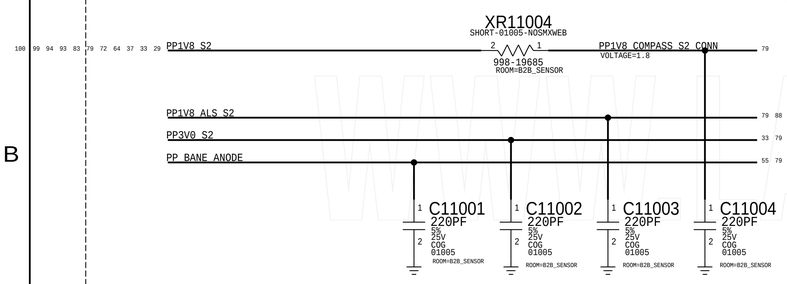
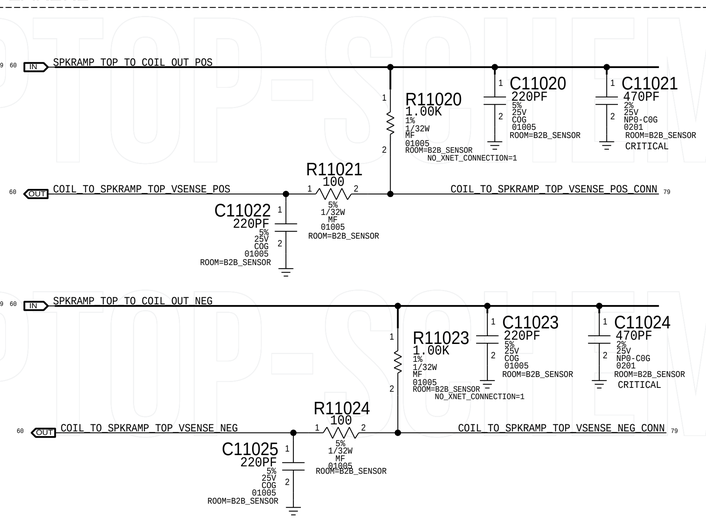
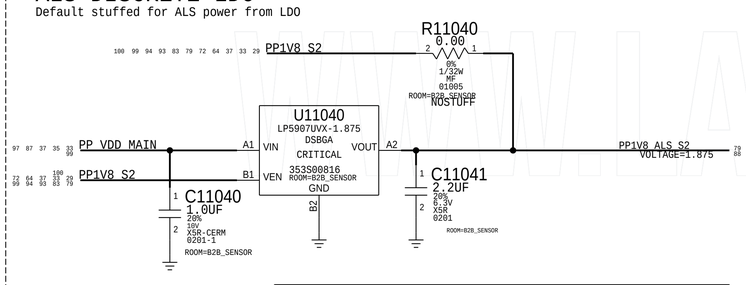


SPEAKER2



ALS DISCRETE LDO

Default stuffed for ALS power from LDO



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SYNCING: NONE

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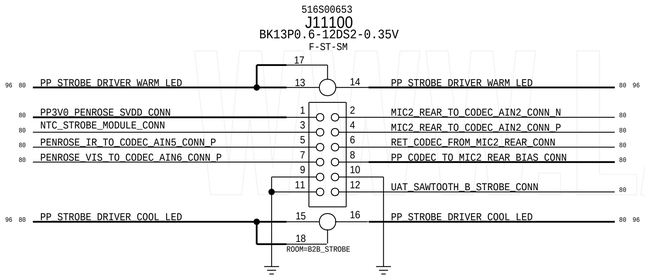

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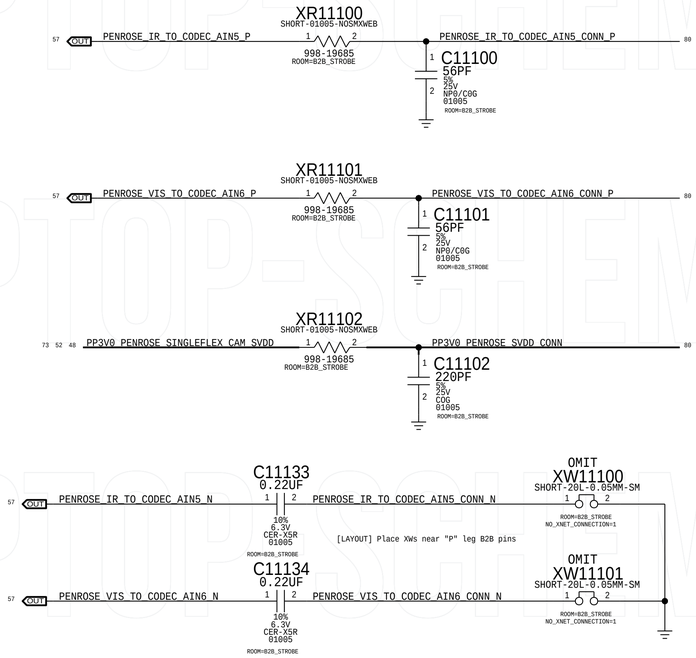
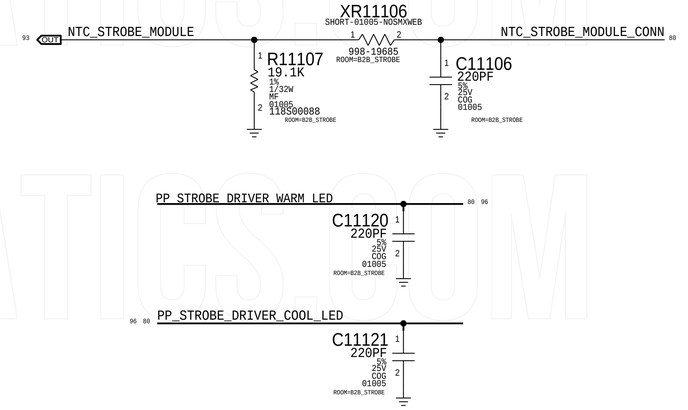


Strobe



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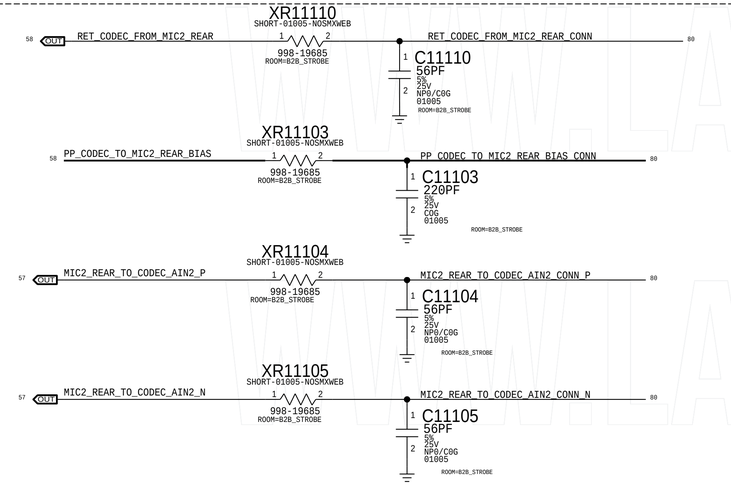
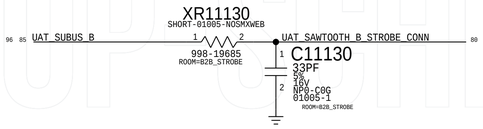


Change SuBus to Sawtooth for flex side per antenna team request



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DOCK B2B

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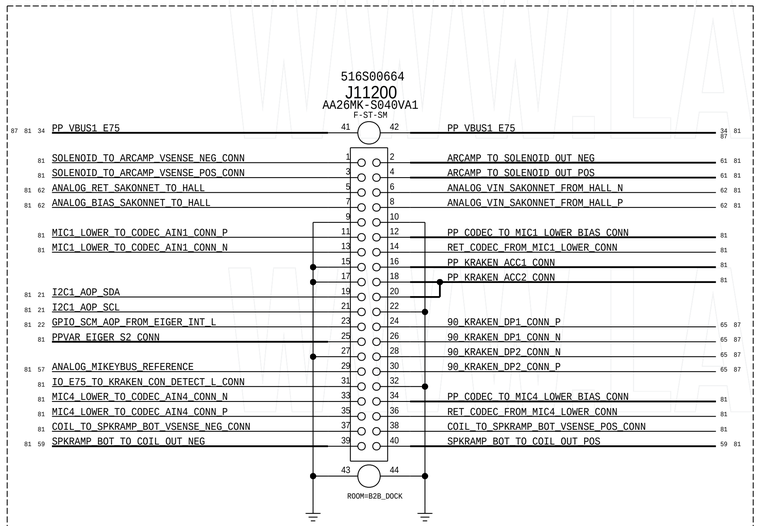

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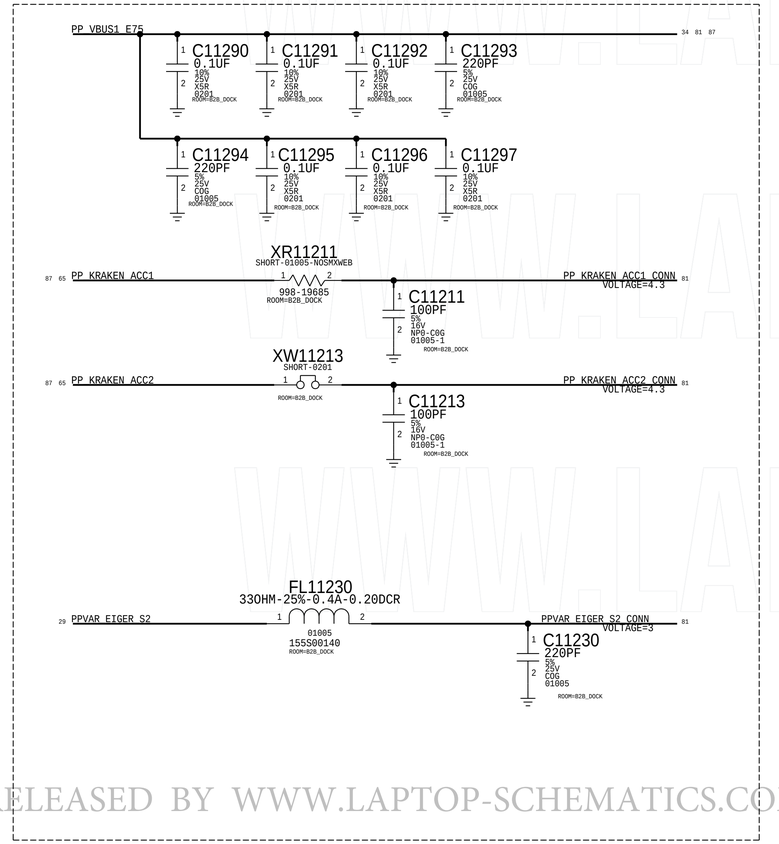
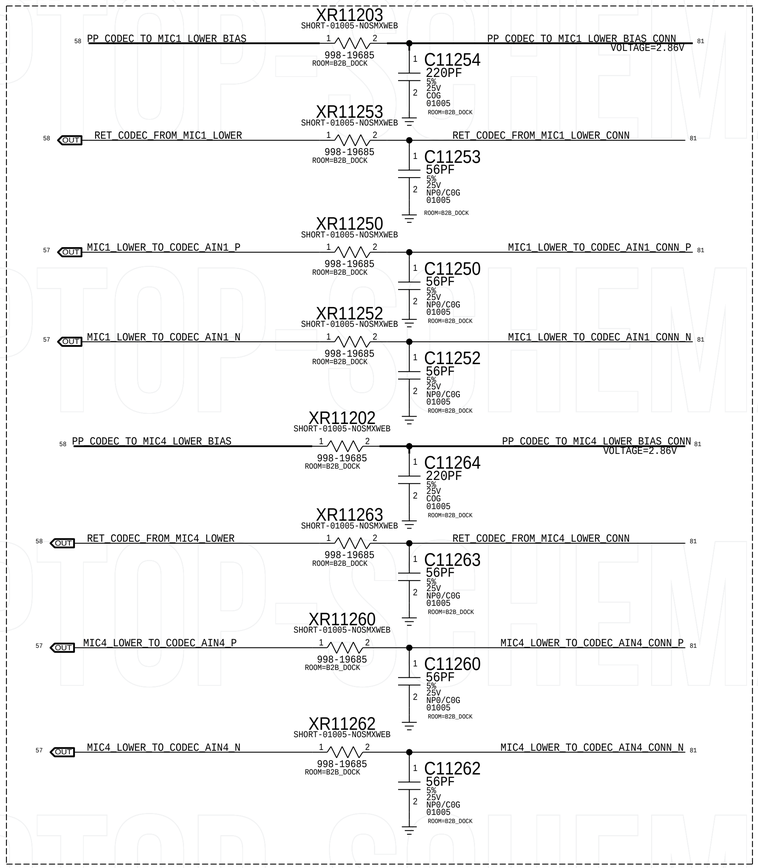


MIC1 + MIC4



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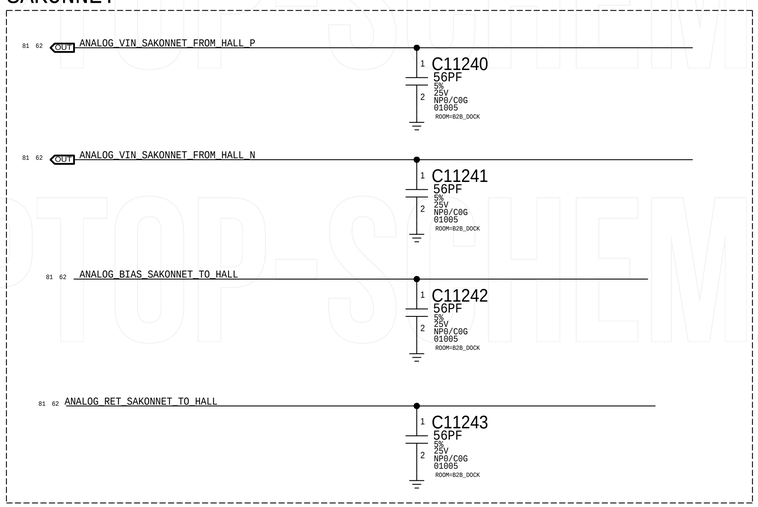
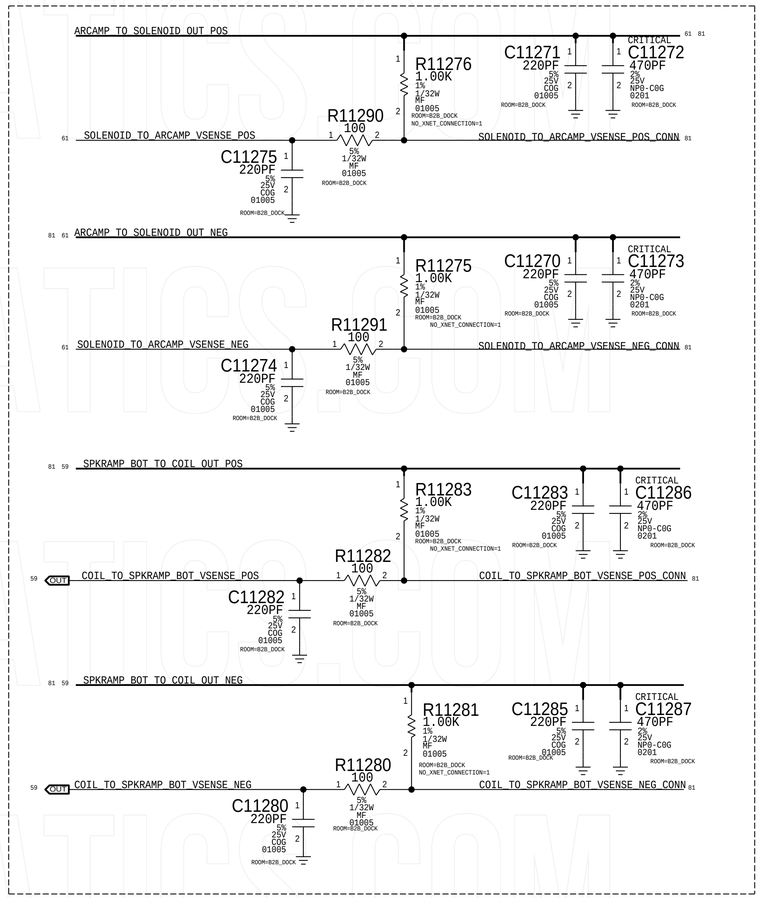


ARC + BOT SPEAKER



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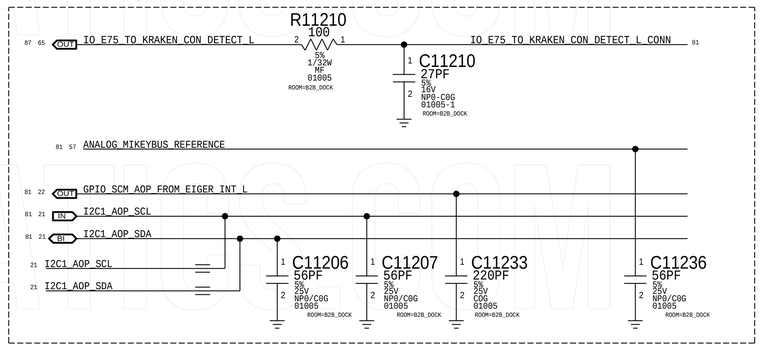

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DISPLAY B2B

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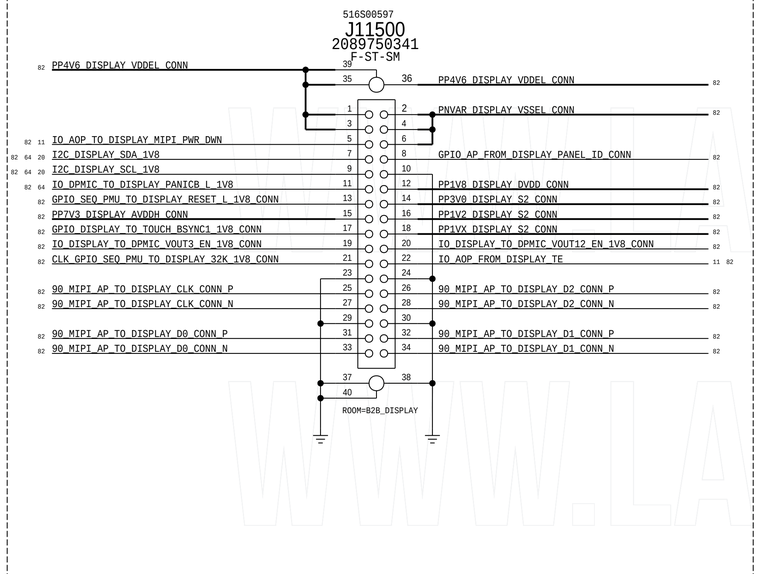

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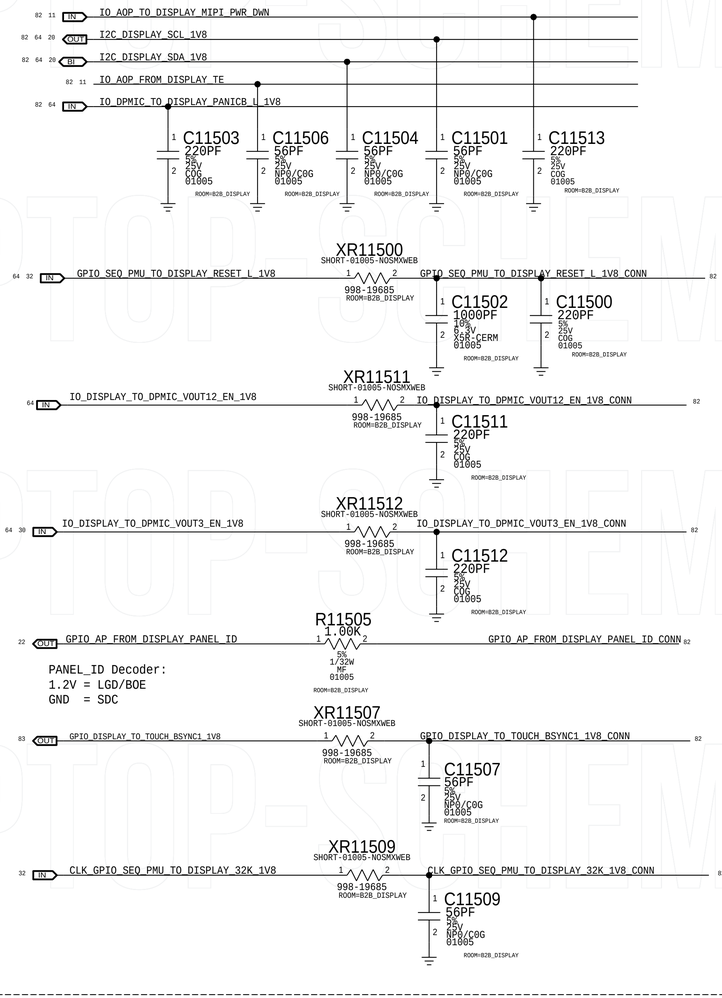

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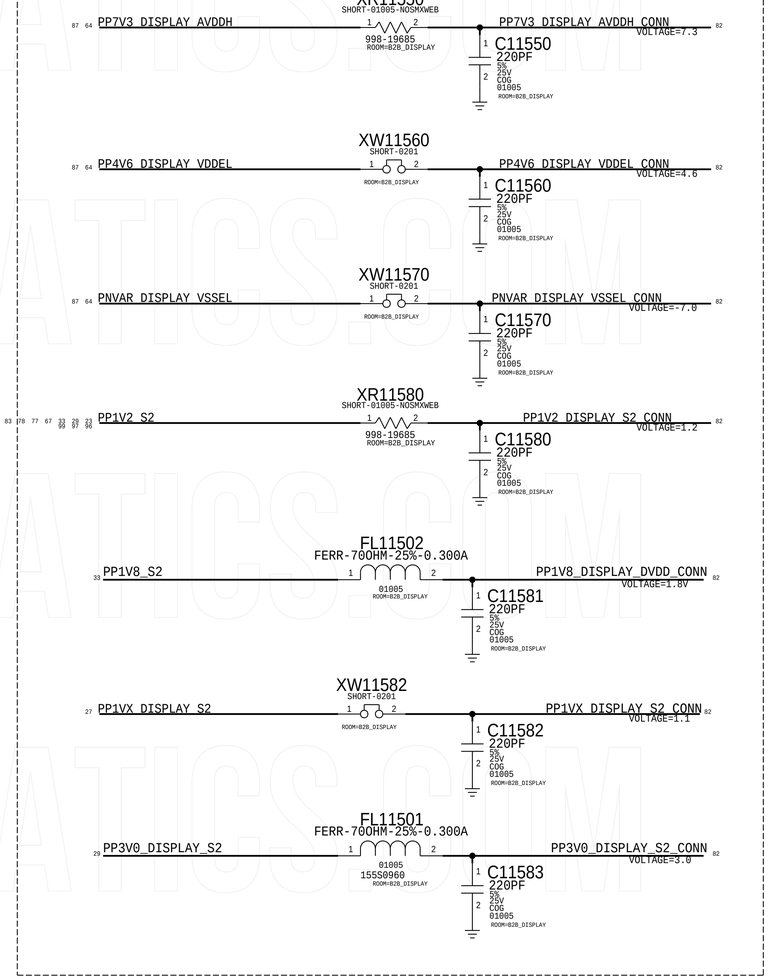

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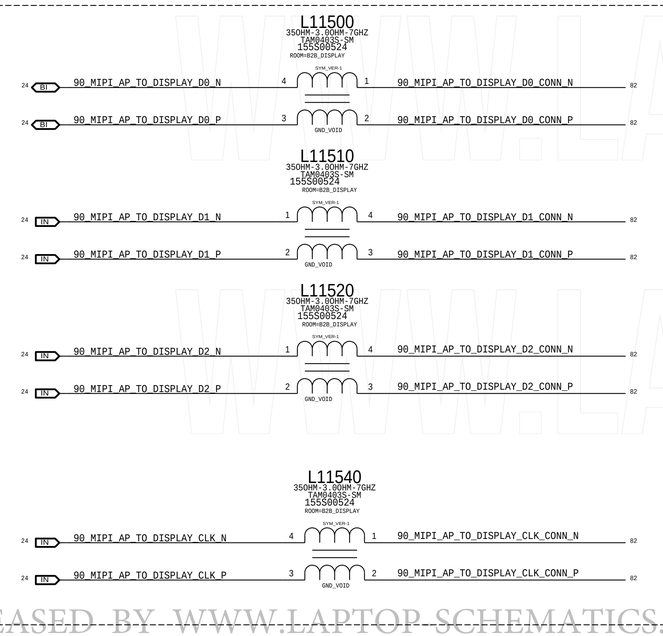

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TOUCH B2B

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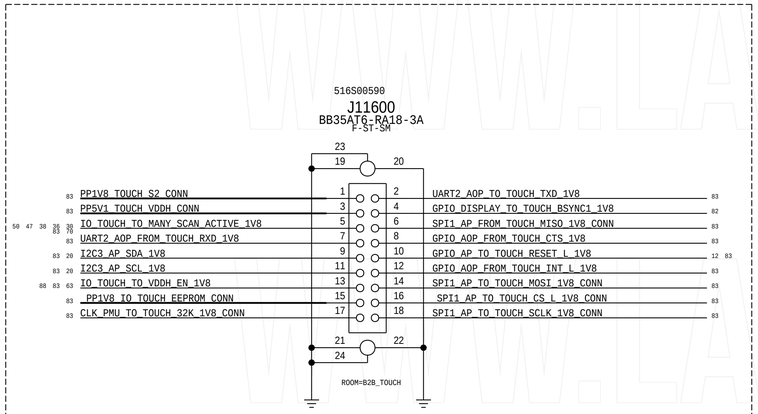

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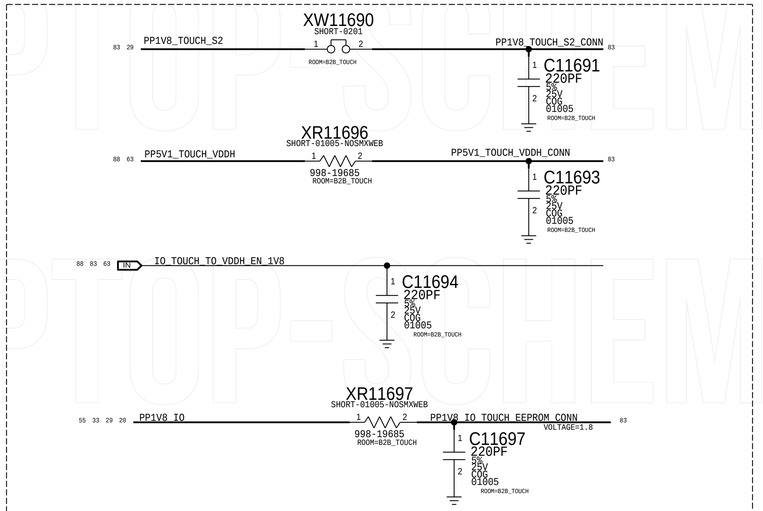

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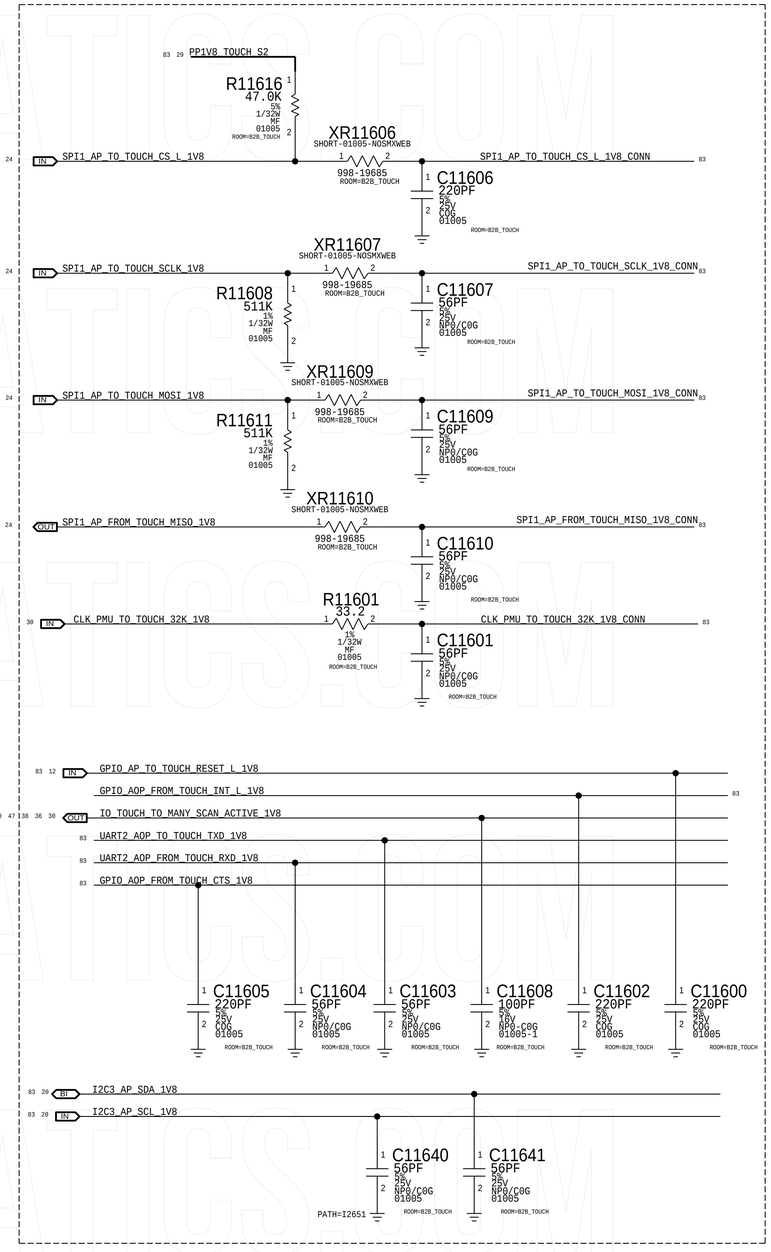

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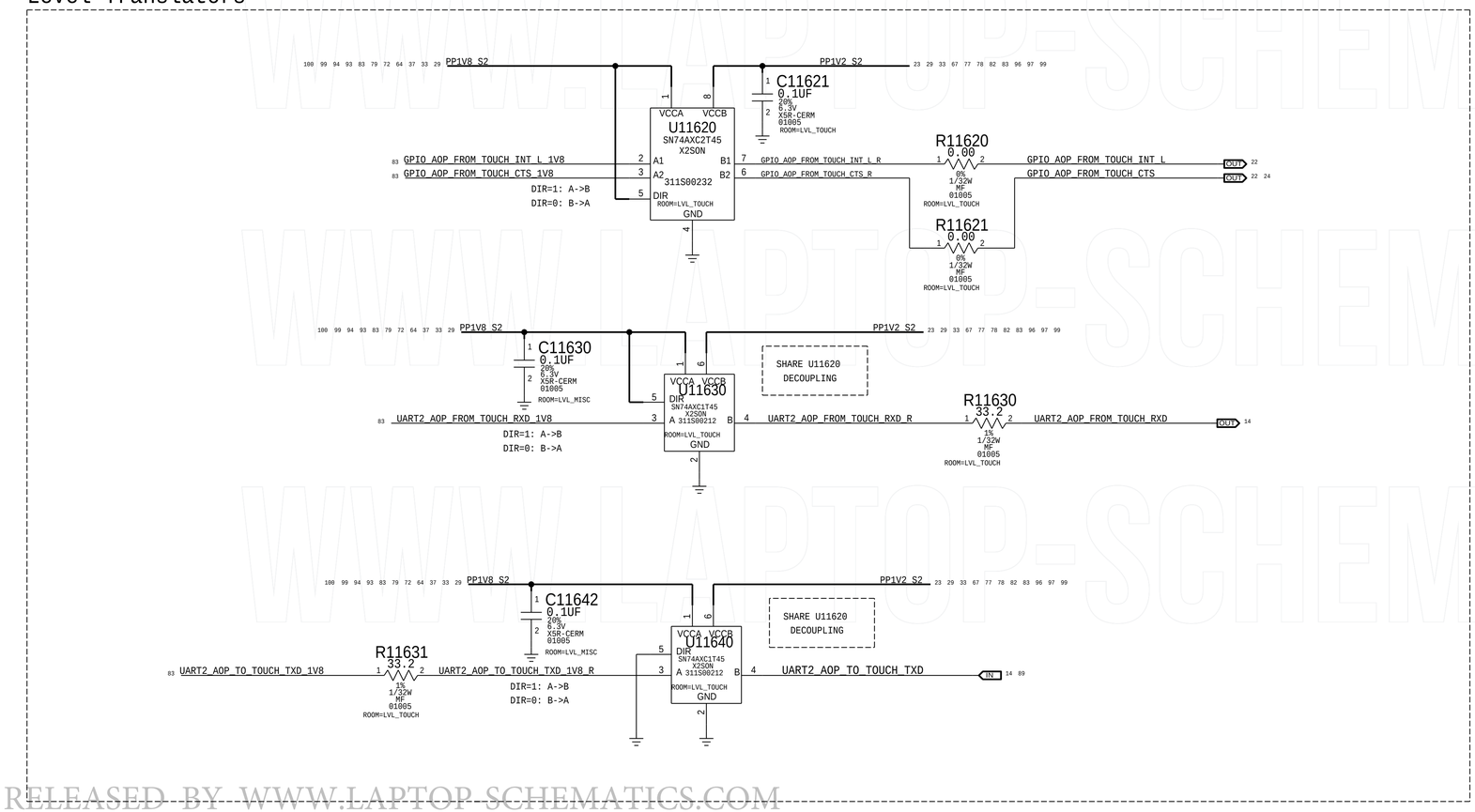

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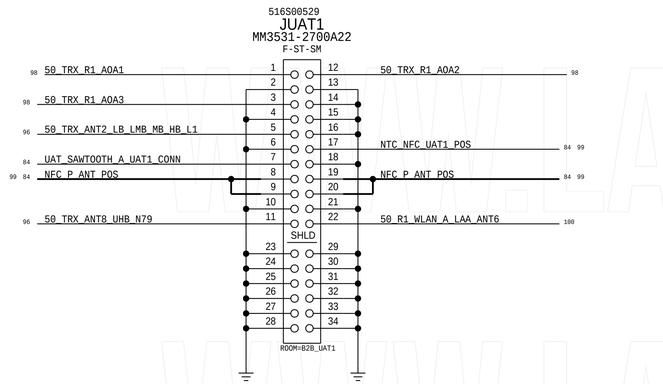
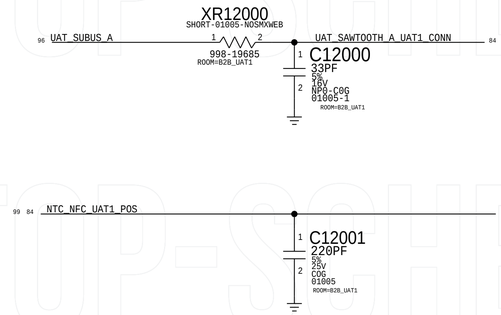
UAT1 B2B

CONNECTOR



IO FILTERS

Change SuBus to Sawtooth for flex side per antenna team request



Misc

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UAT2 B2B

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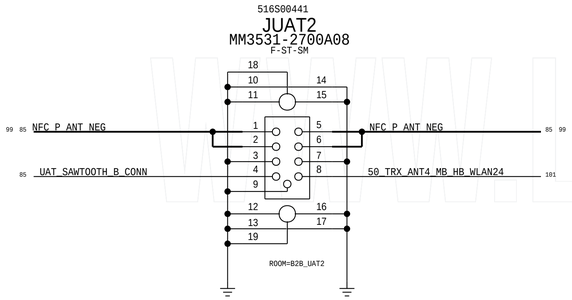

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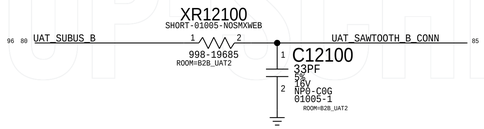

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Mechanical Parts

Standoffs

SB12500 — STDOFF-2.56OD1.4ID-0.855H-SM — 860-01491
SB12501 — STDOFF-2.56OD1.4ID-0.855H-SM — 860-01491
SB12503 — STDOFF-2.56OD1.4ID-0.855H-SM — 860-01491
SB12504 — STDOFF-2.56OD1.4ID-0.855H-SM — 860-01491
SB12505 — STDOFF-2.56OD1.4ID-0.855H-SM — 860-01491

Fiducials

Crosses

FD12500 — FID — 0P5SQ-CROSS-NSP — 998-04808
FD12501 — FID — 0P5SQ-CROSS-NSP — 998-04808
FD12502 — FID — 0P5SQ-CROSS-NSP — 998-04808
FD12503 — FID — 0P5SQ-CROSS-NSP — 998-04808
FD12504 — FID — 0P5SQ-CROSS-NSP — 998-04808
FD12505 — FID — 0P5SQ-CROSS-NSP — 998-04808

Squares

FD12510 — FID — 0P5SQ-SMP3SQ-NSP — 998-00557
FD12511 — FID — 0P5SQ-SMP3SQ-NSP — 998-00557
FD12512 — FID — 0P5SQ-SMP3SQ-NSP — 998-00557
FD12513 — FID — 0P5SQ-SMP3SQ-NSP — 998-00557
FD12514 — FID — 0P5SQ-SMP3SQ-NSP — 998-00557
FD12515 — FID — 0P5SQ-SMP3SQ-NSP — 998-00557

Underfill Dam

NAND

R12500 0.00 0% 1/32W MF 01005 ROOM=NAND CKPLUS_WAIVE=TERMSHORTED
R12501 0.00 0% 1/32W MF 01005 ROOM=NAND CKPLUS_WAIVE=TERMSHORTED
R12502 0.00 0% 1/32W MF 01005 ROOM=NAND CKPLUS_WAIVE=TERMSHORTED
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R12520 0.00 0% 1/32W MF 01005 ROOM=PMU CKPLUS_WAIVE=TERMSHORTED

SOC

R12530 0.00 0% 1/32W MF 01005 ROOM=SOC CKPLUS_WAIVE=TERMSHORTED
R12531 0.00 0% 1/32W MF 01005 ROOM=SOC CKPLUS_WAIVE=TERMSHORTED
R12532 0.00 0% 1/32W MF 01005 ROOM=SOC CKPLUS_WAIVE=TERMSHORTED

Codec

R12536 0.00 0% 1/32W MF 01005 ROOM=CODEC CKPLUS_WAIVE=TERMSHORTED
R12537 0.00 0% 1/32W MF 01005 ROOM=CODEC CKPLUS_WAIVE=TERMSHORTED

C12500 0.1UF 10% 25V X5R 0201 ROOM=CODEC CKPLUS_WAIVE=TERMSHORTED
C12501 0.1UF 10% 25V X5R 0201 ROOM=CODEC CKPLUS_WAIVE=TERMSHORTED
C12503 0.1UF 10% 25V X5R 0201 ROOM=CODEC CKPLUS_WAIVE=TERMSHORTED

PP_VDD_BOOST — 33 36 52 97 101

C12510 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=codec
C12511 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=codec

Arc Amp

OMIT_TABLE
C12540 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=ARC CKPLUS_WAIVE=TERMSHORTED
OMIT_TABLE
C12541 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=ARC CKPLUS_WAIVE=TERMSHORTED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0306	2	CAP,CER,3900PF,10%,50V,X7R,0402	C12540,C12541	NC	?

Shields

CRITICAL
SH12500 SM 806-25301
SHLD-TTS-MLB-TALL-D53

CRITICAL
SH12501 SM 806-23166
SHLD-TTS-MLB-TOP-SM-D53

Interposer Spacers

RefDes called out below

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-03604	21	SPACER,INTERPOSER,SMALL,X891		CRITICAL	?

SP12500,SP12501,SP12502,SP12503,SP12504,SP12505,SP12506,SP12507,SP12508,SP12509,SP12510,SP12511,SP12512,SP12513,SP12514,SP12515,SP12516,SP12517,SP12518,SP12519,SP12520

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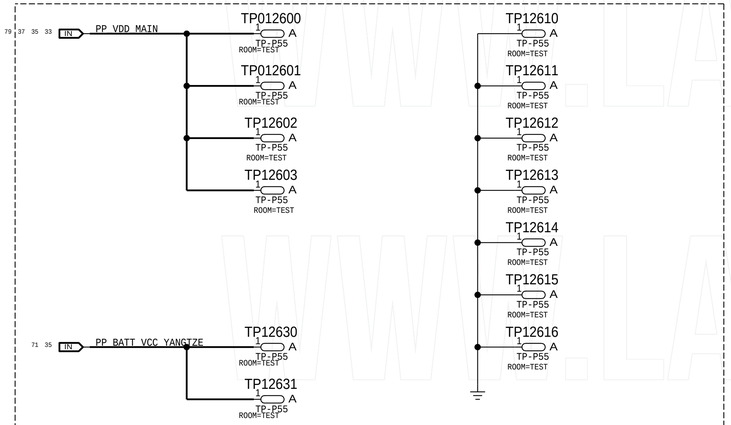
Test Points

Power + GND



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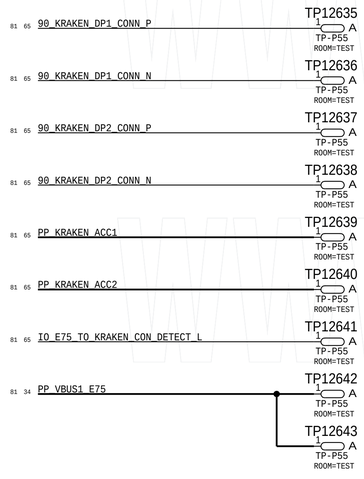
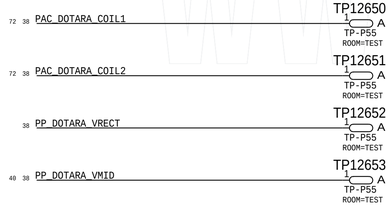
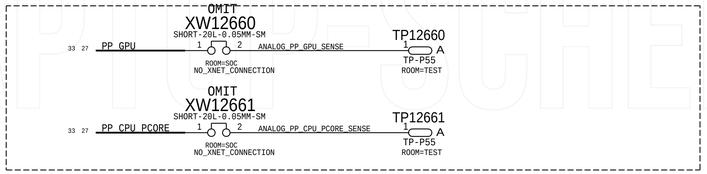


Dotara Power

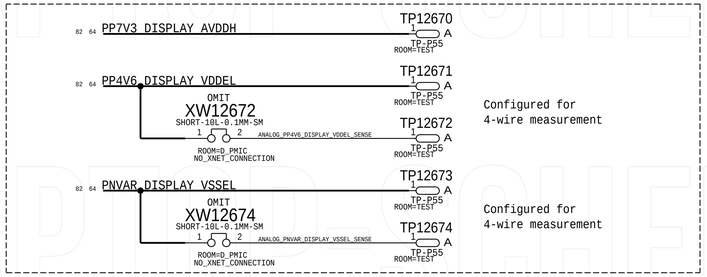


LVCC



REL Bias

Galena



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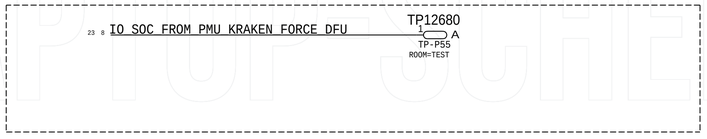
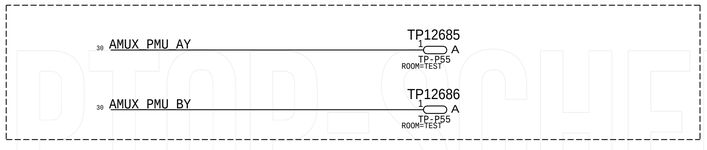
DFU



AMUX



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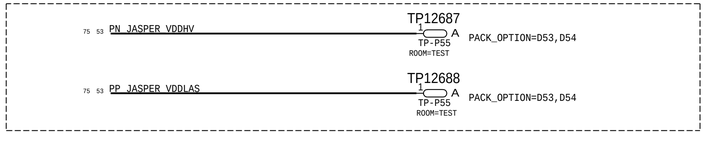

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Test Points

Touch

83 63 PP5V1_TOUCH_VDDH — TP12700 1 A — TP-P55 ROOM=TEST

83 63 IO_TOUCH_TO_VDDH_EN_1V8 — TP12701 1 A — TP-P55 ROOM=TEST

Discrete LDOs

OMIT
XW12710
SHORT-20L-0.05MM-SM
74 52 PP1V1_WIDE_DVDD — 1 — 2 — ANALOG_PP1V1_WIDE_DVDD_SENSE — TP12710 1 A — TP-P55 ROOM=TEST
ROOM=RCAM_LDO
NO_XNET_CONNECTION

XR12711
SHORT-01005-NOSMXWEB
74 52 PP2V85_WIDE_AVDD1 — 1 — 2 — ANALOG_PP2V85_WIDE_AVDD1_SENSE — TP12711 1 A — TP-P55 ROOM=TEST
998-19685
ROOM=RCAM_LDO
NO_XNET_CONNECTION

XR12712
SHORT-01005-NOSMXWEB
73 52 PP2V85_SINGLEFLEX_CAM_AVDD1 — 1 — 2 — ANALOG_PP2V85_SINGLEFLEX_CAM_AVDD1_SENSE — TP12712 1 A — TP-P55 ROOM=TEST
998-19685
ROOM=RCAM_LDO
NO_XNET_CONNECTION

OMIT
XW12713
SHORT-20L-0.05MM-SM
73 52 PP1V2_SINGLEFLEX_CAM_DVDD — 1 — 2 — ANALOG_PP1V2_SINGLEFLEX_CAM_DVDD_SENSE — TP12713 1 A — TP-P55 ROOM=TEST
ROOM=RCAM_LDO
NO_XNET_CONNECTION

XR12714
SHORT-01005-NOSMXWEB
74 52 PP2V85_SUPERFLEX_CAM2_AVDD1 — 1 — 2 — ANALOG_PP2V85_SUPERFLEX_CAM2_AVDD1_SENSE — TP12714 1 A — TP-P55 ROOM=TEST
998-19685
ROOM=RCAM_LDO
NO_XNET_CONNECTION

OMIT
XW12715
SHORT-20L-0.05MM-SM
79 PP1V8_ALS_S2 — 1 — 2 — ANALOG_PP1V8_ALS_S2_SENSE — TP12715 1 A — TP-P55 ROOM=TEST
ROOM=B2B_SENSOR
NO_XNET_CONNECTION

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Probe Points

PP	Net	Pin	Ref	Pin	Net	Type
PP12800	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	1	98 93 32 30			P2MM-NSM SM ROOM=TEST
PP12801	GPIO_SCM_AOP_FROM_JARVIS_INT	1	95 22			P2MM-NSM SM ROOM=TEST
PP12803	GPIO_AOP_TO_CODEC_RESET_L	1	58 22			P2MM-NSM SM ROOM=TEST
PP12804	GPIO_AP_BI_CCG2B_SWDIO	1	66 22			P2MM-NSM SM ROOM=TEST
PP12805	GPIO_AP_FROM_CODEC_INT_L	1	58 22			P2MM-NSM SM ROOM=TEST
PP12807	GPIO_AP_TO_AMUX_PMU_SYNC	1	30 24			P2MM-NSM SM ROOM=TEST
PP12808	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	1	55 48 30			P2MM-NSM SM ROOM=TEST
PP12809	GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	1	55 48			P2MM-NSM SM ROOM=TEST
PP12810	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	1	93 48			P2MM-NSM SM ROOM=TEST
PP12811	GPIO_NUB_FROM_CCG2B_INT_L	1	66 14			P2MM-NSM SM ROOM=TEST
PP12812	GPIO_NUB_FROM_GECKO_IRQ_L	1	67 14			P2MM-NSM SM ROOM=TEST
PP12813	GPIO_NUB_FROM_PARROT_INT_L	1	68 14			P2MM-NSM SM ROOM=TEST
PP12814	GPIO_NUB_TO_GECKO_RESET_L	1	67 14			P2MM-NSM SM ROOM=TEST
PP12815	GPIO_PMU_FROM_CODEC_WAKE_L	1	58 32			P2MM-NSM SM ROOM=TEST
PP12817	GPIO_PMU_TO_CCG2B_RESET_L	1	66 32			P2MM-NSM SM ROOM=TEST
PP12818	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	1	32 25			P2MM-NSM SM ROOM=TEST
PP12819	GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L	1	33 30			P2MM-NSM SM ROOM=TEST
PP12820	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	1	59 32			P2MM-NSM SM ROOM=TEST
PP12821	GPIO_SEQ_PMU_TO_BOOST_EN_1V8	1	36 32			P2MM-NSM SM ROOM=TEST
PP12822	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	1	64 32			P2MM-NSM SM ROOM=TEST
PP12823	I2S0_AOP_FROM_CODEC_ASP1_BCLK	1	58 14			P2MM-NSM SM ROOM=TEST
PP12824	I2S0_AOP_FROM_CODEC_ASP1_DIN	1	58 14			P2MM-NSM SM ROOM=TEST
PP12825	I2S0_AOP_FROM_CODEC_ASP1_LRCLK	1	58 14			P2MM-NSM SM ROOM=TEST
PP12826	I2S0_AOP_TO_CODEC_ASP1_DOUT	1	58 14			P2MM-NSM SM ROOM=TEST
PP12828	IO_KRAKEN_TO_CHARGER_VBUS1_VALID_L_1V8	1	65 34			P2MM-NSM SM ROOM=TEST
PP12829	IO_KRAKEN_TO_PARROT_PMU_USB_EN	1	68 65 30			P2MM-NSM SM ROOM=TEST
PP12830	IO_NUB_FROM_KRAKEN_DOCK_CONNECT	1	65 14			P2MM-NSM SM ROOM=TEST
PP12831	IO_PMU_FROM_KRAKEN_RESET	1	65 30			P2MM-NSM SM ROOM=TEST
PP12832	IO_SPKRAMP_TO_SPKRAMP_SYNC	1	61 60 59			P2MM-NSM SM ROOM=TEST
PP12833	PP_VAR_USB_RVP	1	66 65 34			P2MM-NSM SM ROOM=TEST
PP12834	SPI3_AP_FROM_CODEC_MISO	1	58 23			P2MM-NSM SM ROOM=TEST
PP12835	SPI3_AP_TO_CODEC_CS_L	1	58 23			P2MM-NSM SM ROOM=TEST
PP12836	SPI3_AP_TO_CODEC_MOSI	1	58 23			P2MM-NSM SM ROOM=TEST
PP12837	SWD_NUB_TO_PMU_TOUCH_SWCLK	1	23 14			P2MM-NSM SM ROOM=TEST
PP12838	UART2_AOP_TO_TOUCH_TXD	1	83 14			P2MM-NSM SM ROOM=TEST
PP12839	UART4_AP_FROM_KRAKEN_ACC_RXD	1	23 12			P2MM-NSM SM ROOM=TEST
PP12840	UART4_AP_TO_KRAKEN_ACC_TXD	1	23 12			P2MM-NSM SM ROOM=TEST

PP	Net	Pin	Ref	Pin	Net	Type
PP12841	90_EUSB_DBG_PARROT_BI_AP_N	1	68 23			P2MM-NSM SM ROOM=TEST
PP12842	90_EUSB_DBG_PARROT_BI_AP_P	1	68 23			P2MM-NSM SM ROOM=TEST
PP12843	90_EUSB_PARROT_BI_AP_N	1	68 8			P2MM-NSM SM ROOM=TEST
PP12844	90_EUSB_PARROT_BI_AP_P	1	68 8			P2MM-NSM SM ROOM=TEST
PP12845	90_USB1_KRAKEN_BI_PARROT_N	1	68 65			P2MM-NSM SM ROOM=TEST
PP12846	90_USB1_KRAKEN_BI_PARROT_P	1	68 65			P2MM-NSM SM ROOM=TEST
PP12848	I2S0_AP_FROM_CODEC_ASP3_BCLK	1	58 12			P2MM-NSM SM ROOM=TEST
PP12849	I2S0_AP_FROM_CODEC_ASP3_DIN	1	58 12			P2MM-NSM SM ROOM=TEST
PP12850	I2S0_AP_FROM_CODEC_ASP3_LRCLK	1	58 12			P2MM-NSM SM ROOM=TEST
PP12851	I2S0_AP_TO_CODEC_ASP3_DOUT	1	58 12			P2MM-NSM SM ROOM=TEST
PP12852	I2S1_AP_FROM_CODEC_ASP4_BCLK	1	58 12			P2MM-NSM SM ROOM=TEST
PP12853	I2S1_AP_FROM_CODEC_ASP4_DIN	1	58 12			P2MM-NSM SM ROOM=TEST
PP12854	I2S1_AP_FROM_CODEC_ASP4_LRCLK	1	58 12			P2MM-NSM SM ROOM=TEST
PP12855	I2S1_AP_TO_CODEC_ASP4_DOUT	1	58 12			P2MM-NSM SM ROOM=TEST
PP12856	IO_AP_TO_NAND_FW_STRAP	1	25 8			P2MM-NSM SM ROOM=TEST
PP12857	IO_NUB_FROM_KRAKEN_INT	1	65 14			P2MM-NSM SM ROOM=TEST
PP12858	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	1	33 32 30 34			P2MM-NSM SM ROOM=TEST
PP12859	PDM_OUT1_CODEC_TO_SPKRAMP_TOP_CLK	1	60 57			P2MM-NSM SM ROOM=TEST
PP12860	PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA	1	60 57			P2MM-NSM SM ROOM=TEST
PP12861	UART0_AP_FROM_KRAKEN_DEBUG_RXD	1	23 12			P2MM-NSM SM ROOM=TEST
PP12862	UART0_AP_TO_KRAKEN_DEBUG_TXD	1	23 12			P2MM-NSM SM ROOM=TEST
PP128A1	SWD_DOCK_TO_AP_SWCLK	1	65 14			P2MM-NSM SM ROOM=TEST
PP128A2	SWD_DOCK_BI_AP_SWDIO	1	65 14			P2MM-NSM SM ROOM=TEST

PCIe

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP12864	IN	90_PCIE_ST0_AP_TO_NAND_REFCLK_P	1	25 9			P2MM-NSM SM ROOM=TEST
PP12865	IN	90_PCIE_ST0_AP_TO_NAND_REFCLK_N	1	25 9			P2MM-NSM SM ROOM=TEST

NAND

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP12866	IN	SWD_AP_BI_NAND_SWDIO	1	25 8			P2MM-NSM SM ROOM=TEST
PP12867	IN	SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2	1	25 23 7			P2MM-NSM SM ROOM=TEST
PP12868	IN	IO_AP_TO_NAND_RESET_L	1	25 8			P2MM-NSM SM ROOM=TEST
PP12870	IN	ANALOG_NAND_ANI1_VREF	1	25			P2MM-NSM SM ROOM=TEST
PP12871	IN	ANALOG_NAND_ANI0_VREF	1	25			P2MM-NSM SM ROOM=TEST
PP12872	IN	IO_PMU_TO_NAND_SYSTEM_ALIVE	1	30 25			P2MM-NSM SM ROOM=TEST

PP	Net	Pin	Ref	Pin	Net	Type
PP12873	IO_SOC_DFU_STATUS	1	8		IO_SOC_DFU_STATUS	P2MM-NSM SM ROOM=TEST MAKE_BASE=TRUE
PP12874	TEST_PAD_MTR_ANALOG_P	1	8		TEST_PAD_MTR_ANALOG_P	P2MM-NSM SM ROOM=TEST MAKE_BASE=TRUE
PP12875	TEST_PAD_MTR_ANALOG_N	1	8		TEST_PAD_MTR_ANALOG_N	P2MM-NSM SM ROOM=TEST MAKE_BASE=TRUE

Miscellaneous

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP12876	IN	GPIO_AP_TO_CCG2B_SWCLK	1	66 22			P2MM-NSM SM ROOM=TEST

Parrot

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP12877	IN	GPIO0_PARROT	1	68			P2MM-NSM SM ROOM=TEST
PP12878	IN	GPIO1_PARROT	1	68			P2MM-NSM SM ROOM=TEST

Bump Sense

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP12879	IN	ANALOG_PCPU_SENSE_P	1	27 16			P2MM-NSM SM ROOM=TEST
PP12880	IN	ANALOG_PCPU_SENSE_N	1	19			P2MM-NSM SM ROOM=TEST
PP12881	IN	ANALOG_GPU_SENSE_P	1	16			P2MM-NSM SM ROOM=TEST
PP12882	IN	ANALOG_GPU_SENSE_N	1	19			P2MM-NSM SM ROOM=TEST
PP12883	IN	ANALOG_SOC_SENSE_P	1	16			P2MM-NSM SM ROOM=TEST
PP12884	IN	ANALOG_SOC_SENSE_N	1	19			P2MM-NSM SM ROOM=TEST
PP12885	IN	ANALOG_DCS_SENSE_SE	1	18			P2MM-NSM SM ROOM=TEST
PP12886	IN	ANALOG_DDR_SENSE_SE	1	19			P2MM-NSM SM ROOM=TEST
PP12887	IN	ANALOG_ECPU_SENSE_SE	1	16			P2MM-NSM SM ROOM=TEST
PP12888	IN	ANALOG_VDDQL_SENSE_SE	1	18			P2MM-NSM SM ROOM=TEST

SOC Debug

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP12889	IN	IO_AON_TO_AP_XTAL_CFSB	1	23 14			P2MM-NSM SM ROOM=TEST
PP12890	IN	CLK_AP_TO_PMU_TST_CLKOUT	1	23 8			P2MM-NSM SM ROOM=TEST
PP12891	IN	IO_AP_FROM_PMU_PRE_UVLO_L	1	23			P2MM-NSM SM ROOM=TEST
PP12892	IN	IO_AP_FROM_PMU_SW_SHDN_L	1	23			P2MM-NSM SM ROOM=TEST
PP128A10	IN	GPIO_BOARD_ID0	1	7			P2MM-NSM SM ROOM=TEST PLACE_SIDE=TOP

Dotara

PP	Net	Pin	Ref	Pin	Net	Type
PP12893	DOTARA_SUPER_GPIO_1V8	1	38 30			P2MM-NSM SM ROOM=DOTARA MAKE_BASE=TRUE CXPLUS_WAIVE=SYNONYM_CHECK
PP12894	PP_VBUS2_DOTARA	1	38 34			P2MM-NSM SM ROOM=DOTARA PLACE_SIDE=TOP
PP12895	I2C_SDA_DOTARA_1V8	1	38			P2MM-NSM SM ROOM=DOTARA CXPLUS_WAIVE=I2C_PULLUP
PP12896	I2C_SCL_DOTARA_1V8	1	38			P2MM-NSM SM ROOM=DOTARA CXPLUS_WAIVE=I2C_PULLUP
PP12897	IO_DOTARA_DFT1_1V8	1	38			P2MM-NSM SM ROOM=DOTARA
PP12898	IO_DOTARA_DFT2_1V8	1	38			P2MM-NSM SM ROOM=DOTARA
PP12899	IO_DOTARA_TO_DOMBRA_EN_1V8	1	40 38			P2MM-NSM SM ROOM=DOTARA
PP128A0	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	1	38 32			P2MM-NSM SM ROOM=DOTARA
PP128A3	CLK_BBPMU_TO_DOTARA_38M4	1	95 38			P2MM-NSM SM ROOM=DOTARA PLACE_SIDE=TOP
PP128A4	IO_DOTARA_MTP_WREN_1V8	1	38			P2MM-NSM SM ROOM=DOTARA
PP128A11	IO_DOTARA_TO_DOMBRA_FPWM_1V8	1	40 38			P2MM-NSM SM ROOM=TEST

PMU

PP	Dir	Net	Pin	Ref	Pin	Net	Type
PP128A5	IN	CLK_PMU_TO_AOP_32K	1	30 14			P2MM-NSM SM ROOM=TEST
PP128A6	IN	IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY	1	33 30			P2MM-NSM SM ROOM=TEST
PP128A7	IN	IO_SOC_TO_PMU_WDOG_RESET	1	30 14			P2MM-NSM SM ROOM=TEST
PP128A8	IN	IO_SOC_TO_PMU_SOCHOT_RESET_L	1	23 8			P2MM-NSM SM ROOM=TEST
PP128A9	IN	SWD_NUB_BI_PMU_SWDIO	1	33 14			P2MM-NSM SM ROOM=TEST

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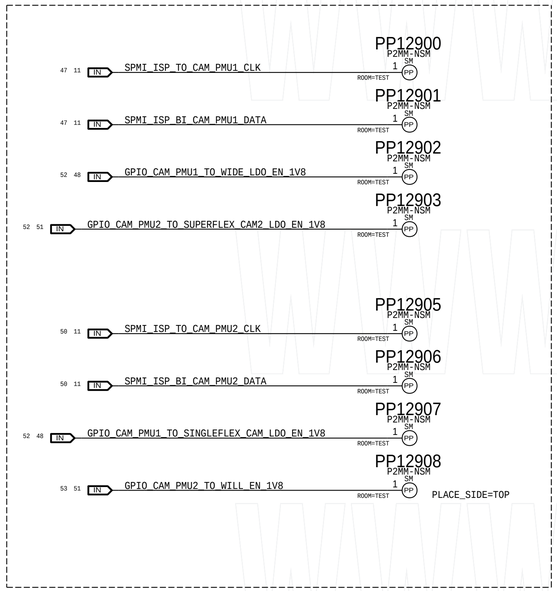
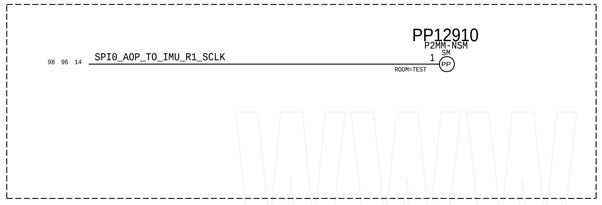
Probe Points

Adams



SPI0_AOP (IMU/R1)



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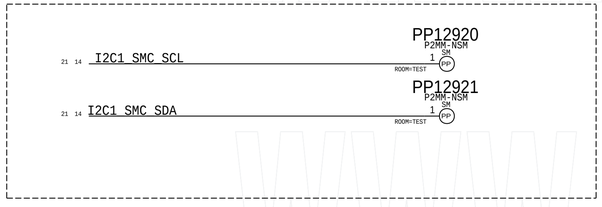

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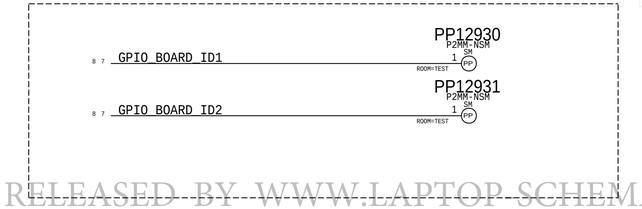

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93	GND	1	IO1	IO91	91	GND	93
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93	GND	3	IO3	IO93	93	GND	93
93	GND	4	IO4	IO94	94	PP_VDD_MAIN	93
93	GND	5	IO5	IO95	95	GND	93
93	GND	6	IO6	IO96	96	PP_VDD_MAIN	93
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93	GND	8	IO8	IO98	98	GPIO_AP_CANARY3	93
93	GND	9	IO9	IO99	99	GND	93
93	GPIO_AP_CANARY6_LEG1	10	IO10	IO100	100	GND	93
93	GND	11	IO11	IO101	101	GND	93
93	GND	12	IO12	IO102	102	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	93
93	GND	13	IO13	IO103	103	GND	93
93	GND	14	IO14	IO104	104	PP_VDD_BOOST	93
93	GPIO_AP_CANARY6_LEG1	15	IO15	IO105	105	GND	93
93	GPIO_AP_CANARY6	16	IO16	IO106	106	PP1V2_S4	93
93	GND	17	IO17	IO107	107	GND	93
93	PP1V8_S2	18	IO18	IO108	108	GPIO_AOP_TO_WLAN_CONTEXT_A	93
93	GND	19	IO19	IO109	109	GND	93
93	GND	20	IO20	IO110	110	PP1V8_S4	93
93	GND	21	IO21	IO111	111	GND	93
93	GND	22	IO22	IO112	112	RFFE_WLAN_TO_UAT_2G_FEM_RST_L	93
93	GND	23	IO23	IO113	113	GND	93
93	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	24	IO24	IO114	114	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	93
93	GND	25	IO25	IO115	115	GND	93
93	GND	26	IO26	IO116	116	GPIO_SE_TO_BT_PKT_RDY	93
93	GND	27	IO27	IO117	117	GND	93
93	IO_R1_TO_BB_LAA_SW_CTRL	28	IO28	IO118	118	GND	93
93	GND	29	IO29	IO119	119	GND	93
93	IO_BT_TO_R1_WAKE	30	IO30	IO120	120	I2C_BT_TO_NFC_SCL	93
93	GND	31	IO31	IO121	121	GND	93
93	GND	32	IO32	IO122	122	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	93
93	GND	33	IO33	IO123	123	GND	93
93	PPVAR_RCAM_PVDD	34	IO34	IO124	124	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	93
93	GND	35	IO35	IO125	125	GND	93
93	GND	36	IO36	IO126	126	GND	93
93	GND	37	IO37	IO127	127	GND	93
93	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	38	IO38	IO128	128	I2C_BT_TO_NFC_SDA	93
93	GND	39	IO39	IO129	129	GND	93
93	GPIO_BB_TO_R1_CH9_REQ	40	IO40	IO130	130	GPIO_AP_FROM_WLAN_TIME_SYNC	93
93	GND	41	IO41	IO131	131	GND	93
93	NTC_STROBE_MODULE	42	IO42	IO132	132	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	93
93	GND	43	IO43	IO133	133	GND	93
93	GND	44	IO44	IO134	134	GND	93
93	GPIO_AP_CANARY5	45	IO45	IO135	135	GND	93
93	GND	46	IO46	IO136	136	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	93
93	GPIO_AP_CANARY5_LEG1	47	IO47	IO137	137	GND	93
93	GND	48	IO48	IO138	138	GPIO_AP_TO_BB_PEAK_PWR_IND	93
93	GND	49	IO49	IO139	139	GND	93
93	GND	50	IO50	IO140	140	SWD_AP_BI_BB_SWDIO	93
93	GPIO_AP_CANARY5_LEG1	51	IO51	IO141	141	GND	93
93	GND	52	IO52	IO142	142	GND	93
93	GND	53	IO53	IO143	143	GND	93
93	GPIO_AP_CANARY5_LEG2	54	IO54	IO144	144	GPIO_AP_FROM_BB_RESET_DETECT_L	93
93	GND	55	IO55	IO145	145	GND	93
93	GND	56	IO56	IO146	146	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	93
93	GND	57	IO57	IO147	147	GND	93
93	GND	58	IO58	IO148	148	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	93
93	GND	59	IO59	IO149	149	GND	93
93	GND	60	IO60	IO150	150	GND	93
				IO151	151	GND	93
93	GND	62	IO62	IO152	152	GPIO_AP_FROM_BT_AUDIO_SYNC	93
93	GPIO_AP_CANARY5_LEG2	63	IO63	IO153	153	GND	93
93	GND	64	IO64	IO154	154	GPIO_AP_TO_BB_TIME_MARK	93
93	GND	65	IO65	IO155	155	GND	93
93	GND	66	IO66	IO156	156	NTC_RADIO_BB_P	93
93	GPIO_AP_CANARY5_LEG3	67	IO67	IO157	157	GND	93
93	GND	68	IO68	IO158	158	GND	93
93	GPIO_AP_CANARY5_LEG3	69	IO69	IO159	159	GND	93
93	GND	70	IO70	IO160	160	UART1_AOP_FROM_BB_RXD	93
93	GND	71	IO71	IO161	161	GND	93
93	GND	72	IO72	IO162	162	UART1_AOP_TO_BB_TXD	93
93	GND	73	IO73	IO163	163	GND	93
93	GND	74	IO74	IO164	164	GPIO_AOP_TO_BB_FORCE_PWM	93
93	GND	75	IO75	IO165	165	GND	93
93	GND	76	IO76	IO166	166	GND	93
93	GND	77	IO77	IO167	167	GND	93
93	GND	78	IO78	IO168	168	PP_VDD_RF_1V2	93
93	GND	79	IO79	IO169	169	GND	93
93	GND	80	IO80	IO170	170	GND	93
93	GND	81	IO81	IO171	171	GND	93
93	GND	82	IO82	IO172	172	GPIO_AOP_TO_WLAN_CONTEXT_B	93
93	GND	83	IO83	IO173	173	GND	93
93	GND	84	IO84	IO174	174	GND	93
93	GND	85	IO85	IO175	175	GND	93
93	GND	86	IO86	IO176	176	PP_VDD_BOOST	93
93	GND	87	IO87	IO177	177	GND	93
93	GND	88	IO88	IO178	178	GND	93
93	GND	89	IO89	IO179	179	GND	93
93	PP_VDD_MAIN	90	IO90	IO180	180	PP_VDD_MAIN	93

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94	GND	181	IO181	IO271	271	50_TRX_LB_PAD_ANT1	94
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94	GND	183	IO183	IO273	273	GND	94
94	PP_VDD_MAIN	184	IO184	IO274	274	GND	94
94	GND	185	IO185	IO275	275	GND	94
94	PP_VDD_MAIN	186	IO186	IO276	276	50_TRX_IN_LMB_PAD_2G_MB_OUT_M	94
94	GND	187	IO187	IO277	277	GND	94
94	GND	188	IO188	IO278	278	GND	94
94	GND	189	IO189	IO279	279	GND	94
94	PP3V0_S2	190	IO190	IO280	280	50_TRX_IN_LMB_PAD_LMB_ANT_M	94
94	GND	191	IO191	IO281	281	GND	94
94	GND	192	IO192	IO282	282	GND	94
94	GND	193	IO193	IO283	283	GND	94
94	GND	194	IO194	IO284	284	GND	94
94	GND	195	IO195	IO285	285	50_TRX_WLAN_G_BT_ANT3_NPLXR	94
94	GND	196	IO196	IO286	286	GND	94
94	GND	197	IO197	IO287	287	GND	94
94	GND	198	IO198	IO288	288	GND	94
94	GND	199	IO199				
94	GPIO_BT_TO_BOT_SPKR_TRIG	200	IO200	IO290	290	GND	94
94	GND	201	IO201	IO291	291	50_TX_IN_XCVR_TX0_MB2G	94
94	GND	202	IO202	IO292	292	GND	94
94	GND	203	IO203	IO293	293	GND	94
94	GND	204	IO204	IO294	294	GND	94
94	GND	205	IO205				
94	GND	206	IO206	IO296	296	GND	94
94	GND	207	IO207	IO297	297	50_TRX_ANT7_UHB_N79	94
94	GND	208	IO208	IO298	298	GND	94
94	GND	209	IO209	IO299	299	GND	94
94	RFFE_WLAN_TO_LAT_2G_FEM_RST_L	210	IO210	IO300	300	GND	94
94	GND	211	IO211	IO301	301	50_TX_IN_XCVR_TX0_LMB	94
94	GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	212	IO212	IO302	302	GPIO_AOP_CANARY7_LEG2	94
94	GND	213	IO213	IO303	303	GND	94
94	ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	214	IO214	IO304	304	GND	94
94	GND	215	IO215	IO305	305	GND	94
94	PP_LDO6_VIO_1V8_SOUTH	216	IO216	IO306	306	PP_VDD_MAIN_FEM_L	94
94	GND	217	IO217	IO307	307	PP_VDD_MAIN_FEM_L	94
94	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	218	IO218	IO308	308	GND	94
94	GND	219	IO219	IO309	309	GND	94
94	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	220	IO220	IO310	310	GPIO_AOP_CANARY7_LEG2	94
94	GND	221	IO221	IO311	311	GND	94
94	PP1V8_S2	222	IO222	IO312	312	GND	94
94	GND	223	IO223	IO313	313	GND	94
94	GND	224	IO224	IO314	314	GND	94
94	GND	225	IO225	IO315	315	GND	94
94	50_RX_LMB_PAD_LMB_PRX_OUT_M	226	IO226	IO316	316	GND	94
94	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	227	IO227	IO317	317	GND	94
94	GND	228	IO228	IO318	318	GND	94
94	GND	229	IO229	IO319	319	GND	94
94	GND	230	IO230	IO320	320	GND	94
94	GND	231	IO231	IO321	321	GPIO_AOP_CANARY7_LEG1	94
94	50_TX_IN_XCVR_TX0_LB	232	IO232	IO322	322	GND	94
94	GND	233	IO233	IO323	323	GND	94
94	GND	234	IO234	IO324	324	GND	94
94	GND	235	IO235	IO325	325	GND	94
94	50_UHB_L_CPLR_OUT	236	IO236	IO326	326	GPIO_AOP_CANARY7_LEG1	94
94	50_RX_XCVR_PRX6_LB_A_RX0	237	IO237	IO327	327	GND	94
94	GND	238	IO238	IO328	328	GPIO_AOP_CANARY7	94
94	GND	239	IO239	IO329	329	GND	94
94	GND	240	IO240	IO330	330	GND	94
94	GND	241	IO241	IO331	331	GND	94
94	PP_QET0_2G_PA	242	IO242	IO332	332	GND	94
94	GND	243	IO243	IO333	333	GND	94
94	PP_QET0_2G_PA	244	IO244	IO334	334	GND	94
94	GND	245	IO245	IO335	335	GND	94
94	PP_QET0_PA	246	IO246	IO336	336	50_TRX_PAUHBL_N79_ANT2_TO_ANT9	94
94	GND	247	IO247	IO337	337	GND	94
94	PP_QET0_PA	248	IO248	IO338	338	GND	94
94	GND	249	IO249	IO339	339	50_TRX_UHB_PAD_PORTB_TX_M	94
94	GND	250	IO250	IO340	340	GND	94
94	GND	251	IO251	IO341	341	GND	94
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94	GND	254	IO254	IO344	344	GND	94
94	GND	255	IO255	IO345	345	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	94
94	SHIELD_RFFE1_SCLK_SDR	256	IO256	IO346	346	GND	94
94	GND	257	IO257	IO347	347	GND	94
94	GND	258	IO258	IO348	348	50_TRX_LB_PORTB_RX1_M	94
94	GND	259	IO259	IO349	349	GND	94
94	SHIELD_RFFE1_SDATA_SDR	260	IO260	IO350	350	GND	94
94	GND	261	IO261				
94	GND	262	IO262	IO352	352	GND	94
94	GND	263	IO263				
94	GND	264	IO264	IO354	354	GND	94
94	GPIO_AOP_CANARY7_LEG3	265	IO265	IO355	355	50_TX_IN_XCVR_TX0_LB2G	94
94	GND	266	IO266	IO356	356	GND	94
94	GPIO_AOP_CANARY7_LEG3	267	IO267	IO357	357	50_RX_XCVR_PRX10_LB_PRX_OUT2	94
94	GND	268	IO268	IO358	358	50_TRX_LB_PORTB_TX_M	94
94	GND	269	IO269	IO359	359	GND	94
94	GND	270	IO270	IO360	360	GND	94

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95	GND	361	IO361	IO451	451	GND	95
95	PP_APT_L_PA	362	IO362	IO452	452	GND	95
95	PP_APT_L_PA	363	IO363	IO453	453	GND	95
95	GND	364	IO364	IO454	454	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	95
95	GND	365	IO365	IO455	455	GND	95
95	PP_QET1_PA	366	IO366	IO456	456	I2S2_AP_FROM_BB_BCLK	95
95	PP_QET1_PA	367	IO367	IO457	457	GND	95
95	GND	368	IO368	IO458	458	I2S2_AP_FROM_BB_LRCLK	95
95	GND	369	IO369	IO459	459	GND	95
95	GND	370	IO370	IO460	460	GND	95
95	50_RX_XCVR_PRX15_N79_RX_OUT2	371	IO371	IO461	461	GND	95
95	GND	372	IO372	IO462	462	I2S2_AP_FROM_BB_DIN	95
95	GND	373	IO373	IO463	463	GND	95
95	GND	374	IO374	IO464	464	I2S2_AP_TO_BB_DOUT	95
95	50_RX_XCVR_PRX17_UHB_RX_OUT2	375	IO375	IO465	465	GND	95
95	50_RX_XCVR_PRX14_N79_RX_OUT1	376	IO376	IO466	466	GND	95
95	GND	377	IO377	IO467	467	GND	95
95	GND	378	IO378				
95	GND	379	IO379	IO469	469	GND	95
95	GND	380	IO380	IO470	470	GND	95
95	50_RX_XCVR_PRX16_UHB_RX_OUT1	381	IO381	IO471	471	GND	95
95	SHIELD_RFFE2_SDATA_SDR	382	IO382	IO472	472	GND	95
95	GND	383	IO383	IO473	473	GND	95
95	SHIELD_RFFE2_SCLK_SDR	384	IO384	IO474	474	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	95
95	SHIELD_RFFE8_SDATA_SDR	385	IO385	IO475	475	GND	95
95	SHIELD_RFFE8_SCLK_SDR	386	IO386	IO476	476	GPIO_S4_PMU_TO_WLAN_REG_ON	95
95	PP_VDD_BOOST	387	IO387	IO477	477	GND	95
95	GND	388	IO388	IO478	478	GPIO_PMU_FROM_WLAN_HOST_WAKE	95
95	GND	389	IO389	IO479	479	GND	95
95	GND	390	IO390	IO480	480	GND	95
95	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	391	IO391	IO481	481	GND	95
95	GND	392	IO392	IO482	482	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	95
95	GND	393	IO393	IO483	483	GND	95
95	GND	394	IO394	IO484	484	PCIE_GP1_AP_TO_WLAN_PERST_L	95
95	50_TX_IN_XCVR_TX1_LB_JB	395	IO395	IO485	485	GND	95
95	SHIELD_RFFE3_SDATA_SDR	396	IO396	IO486	486	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	95
95	GND	397	IO397	IO487	487	GND	95
95	SHIELD_RFFE3_SCLK_SDR	398	IO398	IO488	488	GND	95
95	GND	399	IO399	IO489	489	GND	95
95	GND	400	IO400	IO490	490	PCIE_GP2_AP_TO_BB_PERST_L	95
95	GND	401	IO401	IO491	491	GND	95
95	PP_VDD_MAIN	402	IO402	IO492	492	PCIE_GP2_AP_BI_BB_CLKREQ_L	95
95	GND	403	IO403	IO493	493	GND	95
95	PP_VDD_MAIN	404	IO404	IO494	494	SWD_AP_TO_MANY_SWCLK	95
95	GND	405	IO405	IO495	495	GND	95
95	PP_VDD_MAIN	406	IO406	IO496	496	GPIO_AP_TO_BB_COREDUMP	95
95	GND	407	IO407	IO497	497	GND	95
95	PP_VDD_MAIN	408	IO408				
95	GND	409	IO409	IO499	499	GND	95
95	GND	410	IO410	IO500	500	GPIO_AP_CANARY4	95
95	GND	411	IO411	IO501	501	GND	95
95	GND	412	IO412	IO502	502	GND	95
95	GND	413	IO413	IO503	503	GND	95
95	PP1V2_S2	414	IO414	IO504	504	CLK_BBPMU_TO_NFC_38M4	95
95	GND	415	IO415	IO505	505	GND	95
95	GND	416	IO416	IO506	506	GND	95
95	GND	417	IO417	IO507	507	GND	95
95	GND	418	IO418	IO508	508	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	95
95	GND	419	IO419	IO509	509	GND	95
95	GPIO_SCM_AOP_FROM_JARVIS_INT	420	IO420	IO510	510	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	95
95	GND	421	IO421	IO511	511	GND	95
95	I2C1_AOP_SCL	422	IO422	IO512	512	GND	95
95	GND	423	IO423	IO513	513	GND	95
95	I2C1_AOP_SDA	424	IO424	IO514	514	90_PCIE_GP1_AP_FROM_WLAN_RX_N	95
95	GND	425	IO425	IO515	515	GND	95
95	GND	426	IO426	IO516	516	90_PCIE_GP1_AP_FROM_WLAN_RX_P	95
95	GND	427	IO427	IO517	517	GND	95
95	90_PCIE_GP2_AP_TO_BB_TX_N	428	IO428	IO518	518	GND	95
95	GND	429	IO429	IO519	519	GND	95
95	90_PCIE_GP2_AP_TO_BB_TX_P	430	IO430	IO520	520	90_PCIE_GP1_AP_TO_WLAN_TX_P	95
95	GND	431	IO431	IO521	521	GND	95
95	GND	432	IO432	IO522	522	90_PCIE_GP1_AP_TO_WLAN_TX_N	95
95	GND	433	IO433	IO523	523	GND	95
95	90_PCIE_GP2_AP_FROM_BB_RX_P	434	IO434	IO524	524	GND	95
95	GND	435	IO435	IO525	525	GND	95
95	90_PCIE_GP2_AP_FROM_BB_RX_N	436	IO436	IO526	526	CLK_BBPMU_TO_DOTARA_38M4	95
95	GND	437	IO437	IO527	527	GND	95
95	GND	438	IO438	IO528	528	GND	95
95	GND	439	IO439	IO529	529	GND	95
95	90_PCIE_GP2_AP_TO_BB_REFCLK_N	440	IO440	IO530	530	GPIO_SP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	95
95	GND	441	IO441	IO531	531	GND	95
95	90_PCIE_GP2_AP_TO_BB_REFCLK_P	442	IO442	IO532	532	GND	95
95	GND	443	IO443	IO533	533	GND	95
95	GND	444	IO444	IO534	534	GPIO_AP_CANARY2	95
95	GND	445	IO445	IO535	535	GND	95
95	PP_VDD_MAIN	446	IO446				
95	GND	447	IO447	IO537	537	GND	95
95	PP_VDD_MAIN	448	IO448	IO538	538	GND	95
95	GND	449	IO449	IO539	539	GND	95
95	PP_VDD_MAIN	450	IO450	IO540	540	GND	95

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96	GND	541	IO541	IO631	631	GND	96
96	GND	542	IO542	IO632	632	SHIELD_RFFE5_SDATA_SDR	96
96	50_WLAN_A_C0_TXRX_FEM_M	543	IO543	IO633	633	GND	96
96	GND	544	IO544	IO634	634	GND	96
96	GND	545	IO545	IO635	635	GND	96
96	50_WLAN_G_C0_TXRX_FEM_M	546	IO546	IO636	636	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	96
96	GND	547	IO547	IO637	637	GND	96
96	GND	548	IO548	IO638	638	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	96
96	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	549	IO549	IO639	639	GND	96
96	GND	550	IO550	IO640	640	GND	96
96	GND	551	IO551	IO641	641	GND	96
96	50_TRX_PAUHBU_N79_ANT1_TO_ANT4	552	IO552	IO642	642	UAT_SUBUS_B	96
96	GND	553	IO553	IO643	643	GND	96
96	GND	554	IO554	IO644	644	UAT_SUBUS_A	96
96	GND	555	IO555	IO645	645	GND	96
96	GND	556	IO556	IO646	646	GND	96
96	GND	557	IO557	IO647	647	GND	96
96	GND	558	IO558	IO648	648	NTC_RADIO_PA_P	96
96	GND	559	IO559	IO649	649	GND	96
96	IO_NFC_TO_BBPMU_CLKREQ	560	IO560	IO650	650	UAT_TUNER_TO_R1_STATE	96
96	GND	561	IO561	IO651	651	GND	96
96	GND	562	IO562	IO652	652	GPIO_R1_TO_BB_CH9_COEX	96
96	GND	563	IO563	IO653	653	GND	96
96	GND	564	IO564	IO654	654	GND	96
96	GND	565	IO565	IO655	655	GND	96
96	GND	566	IO566	IO656	656	GPIO_R1_TO_WLAN_COEX	96
96	GND	567	IO567	IO657	657	GND	96
96	GND	568	IO568	IO658	658	PP1V2_S2	96
96	GND	569	IO569	IO659	659	GND	96
96	GND	570	IO570	IO660	660	GND	96
96	GND	571	IO571	IO661	661	GND	96
96	GND	572	IO572	IO662	662	GPIO_CAM_PMU1_TO_PVDD_RESET_L	96
96	GND	573	IO573	IO663	663	GND	96
96	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	574	IO574	IO664	664	I2C4_CAM_PMU1_SCL_1V8	96
96	GND	575	IO575	IO665	665	GND	96
96	GND	576	IO576	IO666	666	GND	96
96	GND	577	IO577	IO667	667	GND	96
96	GND	578	IO578	IO668	668	I2C4_CAM_PMU1_SDA_1V8	96
96	GND	579	IO579	IO669	669	GND	96
96	GND	580	IO580	IO670	670	GND	96
96	GND	581	IO581	IO671	671	GND	96
96	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	582	IO582	IO672	672	GND	96
96	GND	583	IO583	IO673	673	GND	96
96	50_TRX_ANT8_UHB_N79	584	IO584	IO674	674	GND	96
96	GND	585	IO585	IO675	675	GPIO_SCM_AOP_FROM_IMU_DATARDY	96
96	GND	586	IO586	IO676	676	GPIO_AP_CANARY1_LEG2	96
96	GND	587	IO587	IO677	677	GPIO_AP_CANARY1_LEG3	96
96	GND	588	IO588	IO678	678	SPI0_AOP_FROM_IMU_R1_MISO	96
96	GND	589	IO589	IO679	679	PP_STROBE_DRIVER_COOL_LED	96
96	GND	590	IO590	IO680	680	GND	96
96	GPIO_AP_CANARY1	591	IO591	IO681	681	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	96
96	GND	592	IO592	IO682	682	PP_STROBE_DRIVER_COOL_LED	96
96	GND	593	IO593	IO683	683	GPIO_AP_CANARY1_LEG3	96
96	GPIO_AP_CANARY1_LEG1	594	IO594	IO684	684	GND	96
96	GND	595	IO595	IO685	685	GND	96
96	GND	596	IO596	IO686	686	GND	96
96	GND	597	IO597	IO687	687	SPI0_AOP_TO_IMU_R1_MOSI	96
96	GND	598	IO598	IO688	688	PP_STROBE_DRIVER_WARM_LED	96
96	GND	599	IO599	IO689	689	GPIO_AP_CANARY1_LEG4	96
96	GND	600	IO600	IO690	690	SPI0_AOP_TO_IMU_R1_SCLK	96
96	GND	601	IO601	IO691	691	PP_STROBE_DRIVER_WARM_LED	96
96	GND	602	IO602	IO692	692	GND	96
96	GND	603	IO603	IO693	693	GND	96
96	GND	604	IO604	IO694	694	GND	96
96	GPIO_AP_CANARY1_LEG1	605	IO605	IO695	695	GPIO_AP_CANARY1_LEG4	96
96	GND	606	IO606	IO696	696	GND	96
96	GND	607	IO607	IO697	697	GND	96
96	GND	608	IO608	IO698	698	GND	96
96	GND	609	IO609	IO699	699	GND	96
96	GND	610	IO610	IO700	700	GND	96
96	GND	611	IO611	IO701	701	GND	96
96	GND	612	IO612	IO702	702	GND	96
96	GPIO_AP_CANARY1_LEG2	613	IO613	IO703	703	GND	96
96	PP_LDO6_VIO_1V8_NORTH	614	IO614	IO704	704	GND	96
96	GND	615	IO615	IO705	705	GND	96
96	GPIO_BB_TO_R1_COEX	616	IO616	IO706	706	GND	96
96	GND	617	IO617	IO707	707	GND	96
96	IO_BT_TO_R1_TIME_SYNC	618	IO618	IO708	708	GPIO_AP_CANARY6_LEG4	96
96	GND	619	IO619	IO709	709	GND	96
96	GPIO_WLAN_TO_R1_COEX	620	IO620	IO710	710	GND	96
96	GND	621	IO621	IO711	711	GND	96
96	GND	622	IO622	IO712	712	GND	96
96	GND	623	IO623	IO713	713	GPIO_AP_CANARY6_LEG4	96
96	GND	624	IO624	IO714	714	GND	96
96	50_TRX_ANT2_LB_LMB_MB_HB_L1	625	IO625	IO715	715	GND	96
96	GND	626	IO626	IO716	716	GND	96
96	50_LAA_RX_XCVR_DRX10	627	IO627	IO717	717	GPIO_AP_CANARY6_LEG3	96
96	GND	628	IO628	IO718	718	GND	96
96	GND	629	IO629	IO719	719	GND	96
96	SHIELD_RFFE5_SCLK_SDR	630	IO630	IO720	720	GPIO_AP_CANARY6_LEG2	96
				IO721	721	GPIO_AP_CANARY6_LEG3	96
				IO722	722	GND	96
				IO723	723	GND	96
				IO724	724	GND	96
				IO725	725	GND	96
				IO726	726	GND	96
				IO727	727	GND	96

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GND	
GND	
GND	
GND	
GND	
GND	
GPIO_AP_CANARY6_LEG2	GPIO_AP_CANARY6_LEG2 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GPIO_AP_CANARY6_LEG1	GPIO_AP_CANARY6_LEG1 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GND	
GND	
GPIO_AP_CANARY6_LEG1	GPIO_AP_CANARY6_LEG1 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GPIO_AP_CANARY6	GPIO_AP_CANARY6 24 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
PP1V8_S2	PP1V8_S2 29 33 37 64 72 79 83 94 99 100
	MAKE_BASE=TRUE
GND	
GND	
GND	
GND	
GND	
GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8 70 73 74
	MAKE_BASE=TRUE
GND	
GND	
GND	
IO_R1_TO_BB_LAA_SW_CTRL	IO_R1_TO_BB_LAA_SW_CTRL 98 100
	MAKE_BASE=TRUE
GND	
IO_BT_TO_R1_WAKE	IO_BT_TO_R1_WAKE 98
	MAKE_BASE=TRUE
GND	
GND	
GND	
PPVAR_RCAM_PVDD	PPVAR_RCAM_PVDD 73 74 97
	MAKE_BASE=TRUE
GND	
GND	
GND	
GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8 48 89
	MAKE_BASE=TRUE
GND	
GPIO_BB_TO_R1_CH9_REQ	GPIO_BB_TO_R1_CH9_REQ 98
	MAKE_BASE=TRUE
GND	
NTC_STROBE_MODULE	NTC_STROBE_MODULE 80
	MAKE_BASE=TRUE
GND	
GND	
GPIO_AP_CANARY5	GPIO_AP_CANARY5 24 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GPIO_AP_CANARY5_LEG1	GPIO_AP_CANARY5_LEG1 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GND	
GPIO_AP_CANARY5_LEG1	GPIO_AP_CANARY5_LEG1 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GPIO_AP_CANARY5_LEG2	GPIO_AP_CANARY5_LEG2 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GPIO_AP_CANARY5_LEG2	GPIO_AP_CANARY5_LEG2 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GND	
GPIO_AP_CANARY5_LEG3	GPIO_AP_CANARY5_LEG3 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GPIO_AP_CANARY5_LEG3	GPIO_AP_CANARY5_LEG3 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GND	
GND	
GND	
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GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	GND 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
PP_VDD_MAIN	PP_VDD_MAIN 93 97
	CKPLUS_WAIVE=SYNONYM_CHECK
	MAKE_BASE=TRUE

GND	
PP_VDD_MAIN	PP_VDD_MAIN 93 97
	CKPLUS_WAIVE=SYNONYM_CHECK
GND	
PP_VDD_MAIN	PP_VDD_MAIN 93 97
	CKPLUS_WAIVE=SYNONYM_CHECK
GND	
PP_VDD_MAIN	PP_VDD_MAIN 93 97
	CKPLUS_WAIVE=SYNONYM_CHECK
GND	
GPIO_AP_CANARY3	GPIO_AP_CANARY3 24 97
	CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET
GND	
GND	
GND	
CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K 30 32 89 98
	MAKE_BASE=TRUE
GND	
PP_VDD_BOOST	PP_VDD_BOOST 97
	CKPLUS_WAIVE=SYNONYM_CHECK
GND	
PP1V2_S4	PP1V2_S4 27 33 98 99
	MAKE_BASE=TRUE
GND	
GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A 23
	MAKE_BASE=TRUE
GND	
PP1V8_S4	PP1V8_S4 27 33 37 98 99 100
	MAKE_BASE=TRUE
GND	
RFFE_WLAN_TO_UAT_2G_FEM_RST_L	RFFE_WLAN_TO_UAT_2G_FEM_RST_L 100
	MAKE_BASE=TRUE
GND	
RFFE_WLAN_TO_UAT_5G_FEM_RST_L	RFFE_WLAN_TO_UAT_5G_FEM_RST_L 100
	MAKE_BASE=TRUE
GND	
GPIO_SE_TO_BT_PKT_RDY	GPIO_SE_TO_BT_PKT_RDY 99
	MAKE_BASE=TRUE
GND	
GND	
GND	
I2C_BT_TO_NFC_SCL	I2C_BT_TO_NFC_SCL 99
	MAKE_BASE=TRUE
GND	
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS 100
	MAKE_BASE=TRUE
GND	
GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8 79
	MAKE_BASE=TRUE
GND	
GND	
GND	
I2C_BT_TO_NFC_SDA	I2C_BT_TO_NFC_SDA 99
	MAKE_BASE=TRUE
GND	
GPIO_AP_FROM_WLAN_TIME_SYNC	GPIO_AP_FROM_WLAN_TIME_SYNC 22
	MAKE_BASE=TRUE
GND	
GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN 100
	MAKE_BASE=TRUE
GND	
GND	
GND	
GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN 100
	MAKE_BASE=TRUE
GND	
GPIO_AP_TO_BB_PEAK_PWR_IND	GPIO_AP_TO_BB_PEAK_PWR_IND 22
	MAKE_BASE=TRUE
GND	
SWD_AP_BI_BB_SWDIO	SWD_AP_BI_BB_SWDIO 8
	MAKE_BASE=TRUE
GND	
GND	
GND	
GPIO_AP_FROM_BB_RESET_DETECT_L	GPIO_AP_FROM_BB_RESET_DETECT_L 22
	MAKE_BASE=TRUE
GND	
SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA 14 99
	MAKE_BASE=TRUE
GND	
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK 14 99
	MAKE_BASE=TRUE
GND	
GND	
GND	
GPIO_AP_FROM_BT_AUDIO_SYNC	GPIO_AP_FROM_BT_AUDIO_SYNC 22
	MAKE_BASE=TRUE
GND	
GPIO_AP_TO_BB_TIME_MARK	GPIO_AP_TO_BB_TIME_MARK 22
	MAKE_BASE=TRUE
GND	
NTC_RADIO_BB_P	NTC_RADIO_BB_P 30 44
	MAKE_BASE=TRUE
GND	
GND	
GND	
UART1_AOP_FROM_BB_RXD	UART1_AOP_FROM_BB_RXD 14
	MAKE_BASE=TRUE
GND	
UART1_AOP_TO_BB_TXD	UART1_AOP_TO_BB_TXD 14
	MAKE_BASE=TRUE
GND	
GPIO_AOP_TO_BB_FORCE_PWM	GPIO_AOP_TO_BB_FORCE_PWM 22
	MAKE_BASE=TRUE
GND	
GND	
GND	
PP_VDD_RF_1V2	PP_VDD_RF_1V2 101
	MAKE_BASE=TRUE
GND	
GND	
GND	
GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B 23
	MAKE_BASE=TRUE
GND	
GND	
GND	
PP_VDD_BOOST	PP_VDD_BOOST 97
	CKPLUS_WAIVE=SYNONYM_CHECK
GND	
GND	
GND	
PP_VDD_MAIN	PP_VDD_MAIN 94 95 97
	CKPLUS_WAIVE=SYNONYM_CHECK
	MAKE_BASE=TRUE

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91 GND		
91 PP_VDD_MAIN	PP_VDD_MAIN	93 94 95 97
91 GND		
91 PP_VDD_MAIN	PP_VDD_MAIN	93 94 95 97
91 GND		
91 PP_VDD_MAIN	PP_VDD_MAIN	93 94 95 97
91 GND		
91 GND		
91 GND		
91 PP3V0_S2	PP3V0_S2	29 33
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GPIO_BT_TO_BOT_SPKR_TRIG	GPIO_BT_TO_BOT_SPKR_TRIG	59
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 RFFE_WLAN_TO_LAT_2G_FEM_RST_L	RFFE_WLAN_TO_LAT_2G_FEM_RST_L	100
91 GND		
91 GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	100
91 GND		
91 ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	100
91 GND		
91 PP_LDO6_VIO_1V8_SOUTH	PP_LDO6_VIO_1V8_SOUTH	97 101
91 GND		
91 SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	100
91 GND		
91 SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	100
91 GND		
91 PP1V8_S2	PP1V8_S2	29 33 37 64 72 79 83 93 99 100
91 GND		
91 GND		
91 GND		
91 50_RX_LMB_PAD_LMB_PRX_OUT_M	50_RX_LMB_PAD_LMB_PRX_OUT_M	101
91 50_TX_IN_TX2_UHB_PAD_TX_N79_IN	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	101
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TX_IN_XCVR_TX0_LB	50_TX_IN_XCVR_TX0_LB	101
91 GND		
91 GND		
91 GND		
91 50_UHB_L_CPLR_OUT	50_UHB_L_CPLR_OUT	101
91 50_RX_XCVR_PRX6_LB_A_RX0	50_RX_XCVR_PRX6_LB_A_RX0	101
91 GND		
91 GND		
91 GND		
91 GND		
91 PP_QET0_2G_PA	PP_QET0_2G_PA	94 101
91 GND		
91 PP_QET0_2G_PA	PP_QET0_2G_PA	94 101
91 GND		
91 PP_QET0_PA	PP_QET0_PA	94 101
91 GND		
91 PP_QET0_PA	PP_QET0_PA	94 101
91 GND		
91 GND		
91 GND		
91 50_WLAN_G_C1_TXRX_FEM_M	50_WLAN_G_C1_TXRX_FEM_M	100
91 GND		
91 GND		
91 GND		
91 SHIELD_RFFE1_SCLK_SDR	SHIELD_RFFE1_SCLK_SDR	101
91 GND		
91 GND		
91 GND		
91 SHIELD_RFFE1_SDATA_SDR	SHIELD_RFFE1_SDATA_SDR	101
91 GND		
91 GND		
91 GND	GND	97
91 GND		
91 GPIO_AOP_CANARY7_LEG3	GPIO_AOP_CANARY7_LEG3	97
91 GND		
91 GPIO_AOP_CANARY7_LEG3	GPIO_AOP_CANARY7_LEG3	97
91 GND		
91 GND		
91 GND		

MAKE_BASE=TRUE

91 50_TRX_LB_PAD_ANT1	50_TRX_LB_PAD_ANT1	101
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TRX_IN_LMB_PAD_2G_MB_OUT_M	50_TRX_IN_LMB_PAD_2G_MB_OUT_M	101
91 GND		
91 GND		
91 GND		
91 50_TRX_IN_LMB_PAD_LMB_ANT_M	50_TRX_IN_LMB_PAD_LMB_ANT_M	101
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TRX_WLAN_G_BT_ANT3_NPLXR	50_TRX_WLAN_G_BT_ANT3_NPLXR	100
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TX_IN_XCVR_TX0_MB2G	50_TX_IN_XCVR_TX0_MB2G	101
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TRX_ANT7_UHB_N79	50_TRX_ANT7_UHB_N79	101
91 GND		
91 GND		
91 GND		
91 50_TX_IN_XCVR_TX0_LMB	50_TX_IN_XCVR_TX0_LMB	101
91 GPIO_AOP_CANARY7_LEG2	GPIO_AOP_CANARY7_LEG2	97
91 GND		
91 GND		
91 GND		
91 PP_VDD_MAIN_FEM_L	PP_VDD_MAIN_FEM_L	94 97
91 PP_VDD_MAIN_FEM_L	PP_VDD_MAIN_FEM_L	94 97
91 GND		
91 GND		
91 GPIO_AOP_CANARY7_LEG2	GPIO_AOP_CANARY7_LEG2	97
91 GND		
91 GND		
91 GND		
91 GND		
91 GPIO_AOP_CANARY7_LEG1	GPIO_AOP_CANARY7_LEG1	97
91 GND		
91 GND		
91 GND		
91 GND		
91 GPIO_AOP_CANARY7_LEG1	GPIO_AOP_CANARY7_LEG1	97
91 GND		
91 GPIO_AOP_CANARY7	GPIO_AOP_CANARY7	24 97
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TRX_PAUHBL_N79_ANT2_TO_ANT9	50_TRX_PAUHBL_N79_ANT2_TO_ANT9	101
91 GND		
91 GND		
91 50_TRX_UHB_PAD_PORTB_TX_M	50_TRX_UHB_PAD_PORTB_TX_M	101
91 GND		
91 GND		
91 50_TRX_UHB_PAD_N79_PORTB_TX_M	50_TRX_UHB_PAD_N79_PORTB_TX_M	101
91 GND		
91 GND		
91 50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	101
91 GND		
91 GND		
91 50_TRX_LB_PORTB_RX1_M	50_TRX_LB_PORTB_RX1_M	101
91 GND		
91 GND		
91 GND		
91 GND		
91 50_TX_IN_XCVR_TX0_LB2G	50_TX_IN_XCVR_TX0_LB2G	101
91 GND		
91 50_RX_XCVR_PRX10_LB_PRX_OUT2	50_RX_XCVR_PRX10_LB_PRX_OUT2	101
91 50_TRX_LB_PORTB_TX_M	50_TRX_LB_PORTB_TX_M	101
91 GND		
91 GND		

MAKE_BASE=TRUE

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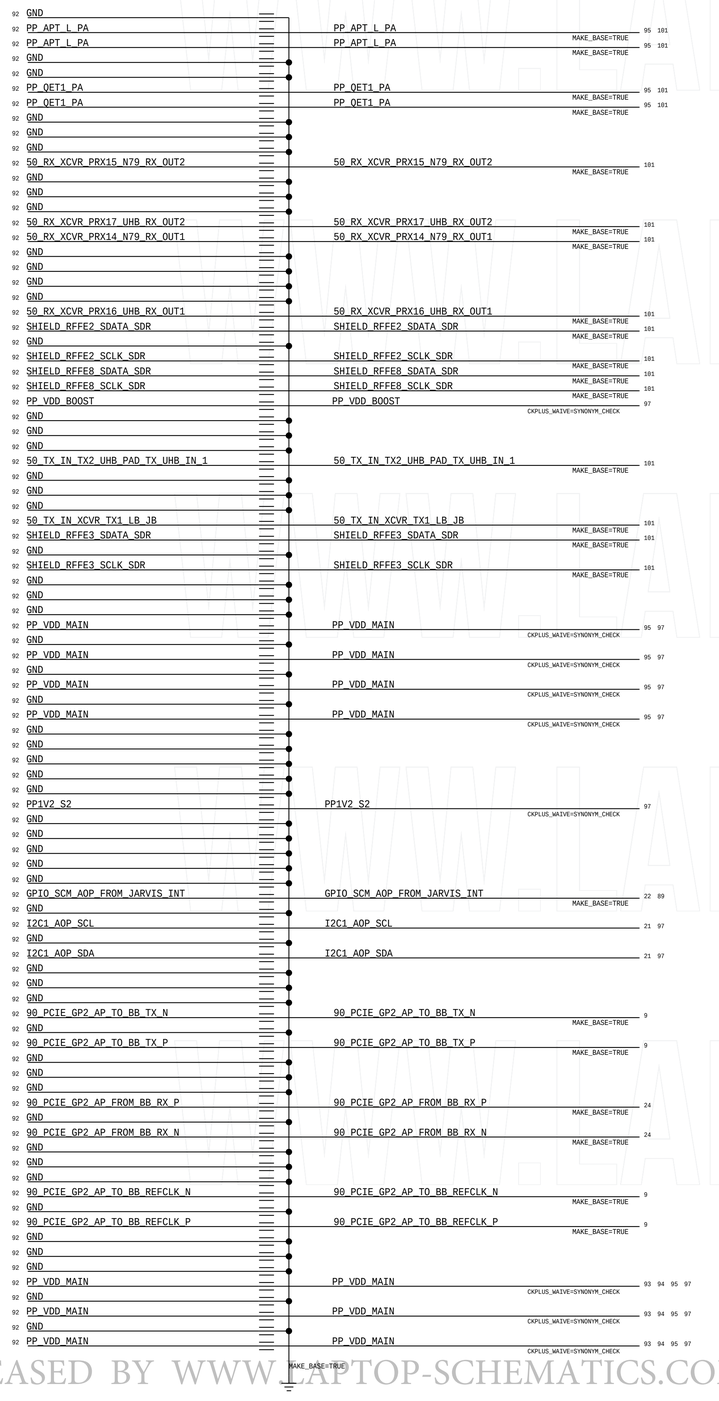

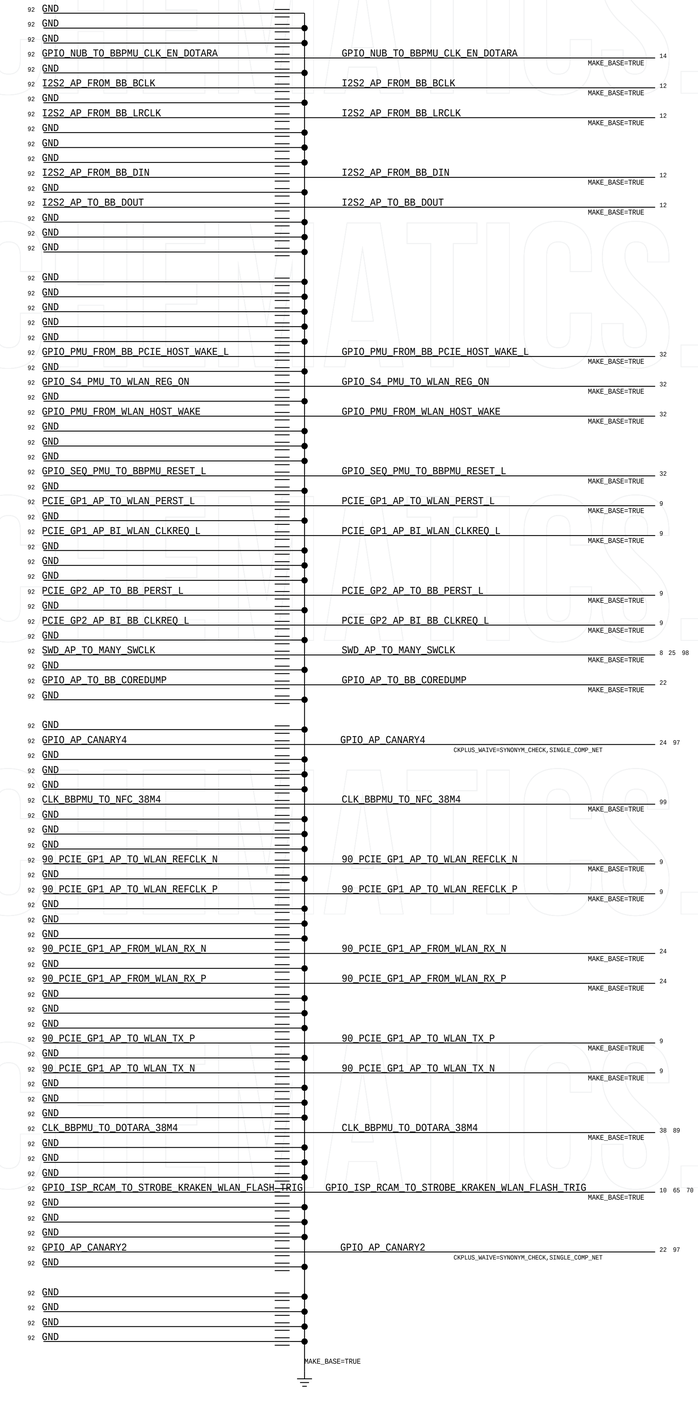

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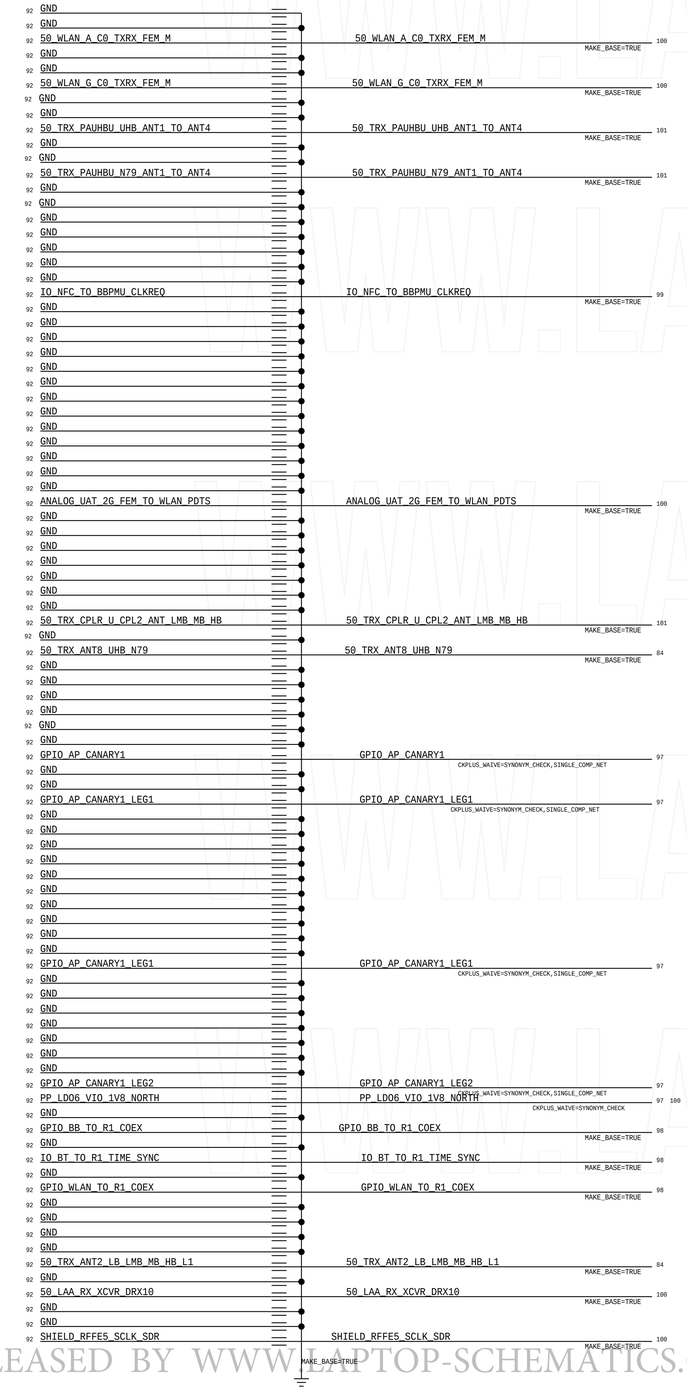

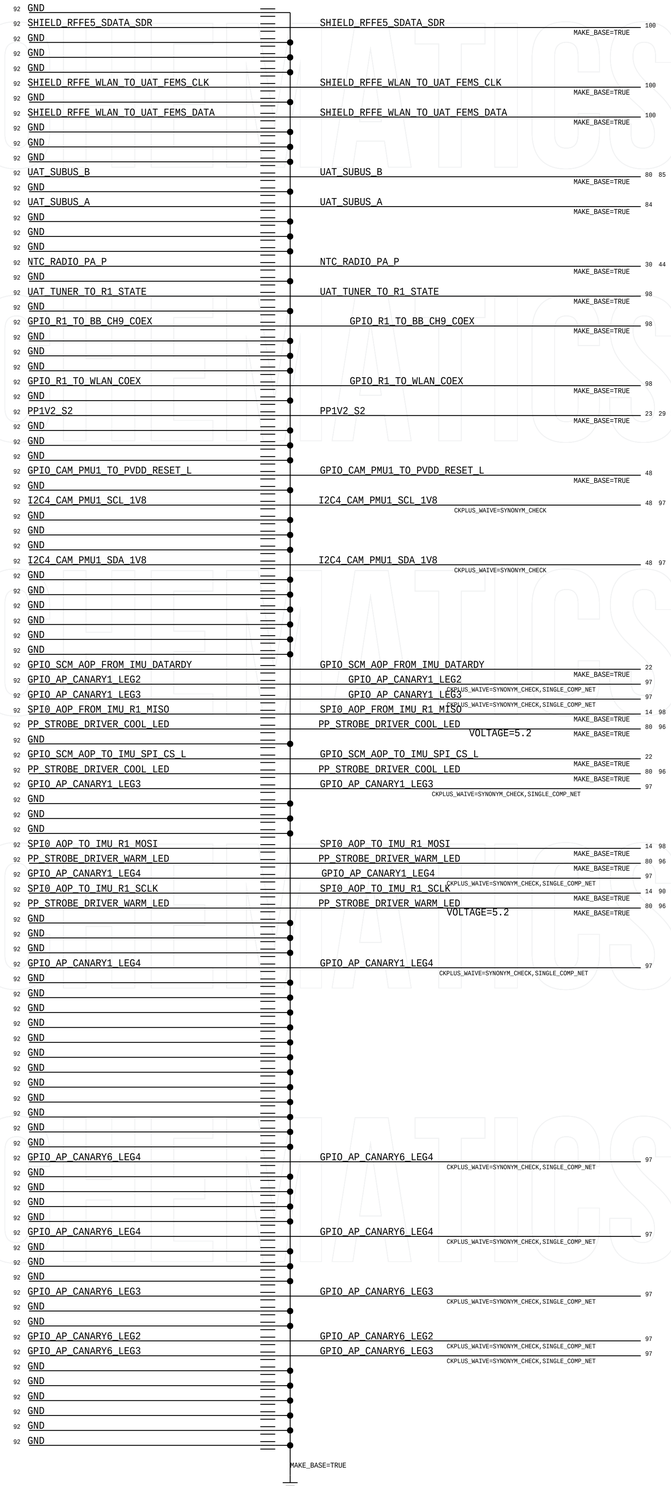

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Lex Output

OMIT
XW13900
SHORT-20L-0.05MM-SM
1 — 2
ROOM=INTERPOSER
NO_XNET_CONNECTION

93 74 79 PPVAR_RCAM_PVDD — AMUX_RCAM_PVDD 30

Power Rail Splits (Bottom Board)

37 36 33 93 / 97 87 79 PP_VDD_MAIN (MAKE_BASE=TRUE) — PP_VDD_MAIN 93
PP_VDD_MAIN 93 94 95
PP_VDD_MAIN 95

100 37 PP_VDD_MAIN_FEM_L (MAKE_BASE=TRUE) — PP_VDD_MAIN_FEM_L 94

52 36 33 101 86 PP_VDD_BOOST (MAKE_BASE=TRUE) — PP_VDD_BOOST 93
PP_VDD_BOOST 95
PP_VDD_BOOST 93

Power Rail Splits (Top Board)

101 97 94 PP_LDO6_VIO_1V8_SOUTH (MAKE_BASE=TRUE) — PP_LDO6_VIO_1V8_SOUTH 94 97 101

100 97 96 PP_LDO6_VIO_1V8_NORTH (MAKE_BASE=TRUE) — PP_LDO6_VIO_1V8_NORTH 96 97 100

Lex/Yeti I2C

96 48 I2C4_CAM_PMU1_SCL_1V8 — I2C4_CAM_PMU1_SCL_1V8 48 (CKPLUS_WAIVE=SYNONYM_CHECK)

96 48 I2C4_CAM_PMU1_SDA_1V8 — I2C4_CAM_PMU1_SDA_1V8 48 (CKPLUS_WAIVE=SYNONYM_CHECK)

Jarvis

97 95 21 I2C1_AOP_SCL — I2C1_AOP_SCL 21 95 97 (CKPLUS_WAIVE=SYNONYM_CHECK)

97 95 21 I2C1_AOP_SDA — I2C1_AOP_SDA 21 95 97 (CKPLUS_WAIVE=SYNONYM_CHECK)

95 PP1V2_S2 — PP1V2_S2 23 29 33 67 77 78 82 83 96 99 (MAKE_BASE=TRUE)

SCAN_ACTIVE (NC'd)

70 NC_IO_TOUCH_TO_MANY_SCAN_ACTIVE — NC_IO_TOUCH_TO_MANY_SCAN_ACTIVE (MAKE_BASE=TRUE)

Canary (single-pin)

97 95 22 GPIO_AP_CANARY2 — GPIO_AP_CANARY2 22 95 97 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)

97 93 24 GPIO_AP_CANARY3 — GPIO_AP_CANARY3 24 93 97 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)

97 95 24 GPIO_AP_CANARY4 — GPIO_AP_CANARY4 24 95 97 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)

Canary (daisy-chain)

22 GPIO_AP_CANARY1 — GPIO_AP_CANARY1 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY1_LEG1 — GPIO_AP_CANARY1_LEG1 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY1_LEG1 — GPIO_AP_CANARY1_LEG1 96 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY1_LEG2 — GPIO_AP_CANARY1_LEG2 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY1_LEG2 — GPIO_AP_CANARY1_LEG2 96 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY1_LEG3 — GPIO_AP_CANARY1_LEG3 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY1_LEG3 — GPIO_AP_CANARY1_LEG3 96 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY1_LEG4 — GPIO_AP_CANARY1_LEG4 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY1_LEG4 — GPIO_AP_CANARY1_LEG4 96 (MAKE_BASE=TRUE)

97 93 24 GPIO_AP_CANARY6 — GPIO_AP_CANARY6 24 93 97 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY6_LEG1 — GPIO_AP_CANARY6_LEG1 93 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY6_LEG1 — GPIO_AP_CANARY6_LEG1 93 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY6_LEG2 — GPIO_AP_CANARY6_LEG2 93 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY6_LEG2 — GPIO_AP_CANARY6_LEG2 96 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY6_LEG3 — GPIO_AP_CANARY6_LEG3 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY6_LEG3 — GPIO_AP_CANARY6_LEG3 96 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY6_LEG4 — GPIO_AP_CANARY6_LEG4 96 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY6_LEG4 — GPIO_AP_CANARY6_LEG4 96 (MAKE_BASE=TRUE)

97 93 24 GPIO_AP_CANARY5 — GPIO_AP_CANARY5 24 93 97 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY5_LEG1 — GPIO_AP_CANARY5_LEG1 93 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY5_LEG1 — GPIO_AP_CANARY5_LEG1 93 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY5_LEG2 — GPIO_AP_CANARY5_LEG2 93 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY5_LEG2 — GPIO_AP_CANARY5_LEG2 93 (MAKE_BASE=TRUE)
97 GPIO_AP_CANARY5_LEG3 — GPIO_AP_CANARY5_LEG3 93 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AP_CANARY5_LEG3 — GPIO_AP_CANARY5_LEG3 93 (MAKE_BASE=TRUE)
GND 93 (MAKE_BASE=TRUE)

97 94 24 GPIO_AOP_CANARY7 — GPIO_AOP_CANARY7 24 94 97 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AOP_CANARY7_LEG1 — GPIO_AOP_CANARY7_LEG1 94 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AOP_CANARY7_LEG1 — GPIO_AOP_CANARY7_LEG1 94 (MAKE_BASE=TRUE)
97 GPIO_AOP_CANARY7_LEG2 — GPIO_AOP_CANARY7_LEG2 94 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AOP_CANARY7_LEG2 — GPIO_AOP_CANARY7_LEG2 94 (MAKE_BASE=TRUE)
97 GPIO_AOP_CANARY7_LEG3 — GPIO_AOP_CANARY7_LEG3 94 (MAKE_BASE=TRUE, CKPLUS_WAIVE=SYNONYM_CHECK,SINGLE_COMP_NET)
97 GPIO_AOP_CANARY7_LEG3 — GPIO_AOP_CANARY7_LEG3 94 (MAKE_BASE=TRUE)
GND 94 (MAKE_BASE=TRUE)

33 PP_VDD_MAIN — PP_VDD_MAIN 33 35 37 79 87 97 99 (MAKE_BASE=TRUE)

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Arrow Hierarchy

103	99	93	33	27	PP1V2_S4	PP1V2_S4
103	100	99	93	37	33	27	PP1V8_S4	PP1V8_S4
103	29	PP1V0_R1_ANA_S4	PP1V0_R1_ANA
103	29	PP1V0_S4	PP1V0_R1_SOC
103	32	GPIO_S4_PMU_TO_R1_RESET_L	APPMU_TO_R1_RESET_L
103	93	89	32	30	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	APPMU_TO_WLAN_32K_CLK
103	22	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	AOP_TO_R1_COREDUMP_TRIG
103	22	GPIO_SCM_AOP_TO_R1_SPI_CS_L	SPI_AOP_TO_R1_CS_L
103	96	90	14	SPI0_AOP_TO_IMU_R1_SCLK	SPI_AOP_TO_R1_SCLK
103	96	14	SPI0_AOP_TO_IMU_R1_MOSI	SPI_AOP_TO_R1_MOSI
103	96	14	SPI0_AOP_FROM_IMU_R1_MISO	SPI_R1_TO_AOP_MISO
103	22	GPIO_SCM_AOP_FROM_R1_INT	R1_TO_AOP_INT
103	99	I2C_R1_TO_NFC_SCL	I2C_R1_TO_SE_SCL
103	99	I2C_R1_TO_NFC_SDA	I2C_R1_TO_SE_SDA
103	93	GPIO_BB_TO_R1_CH9_REQ	BB_TO_R1_CH9_REQ
103	96	GPIO_WLAN_TO_R1_COEX	WLAN_TO_R1_COEX
103	96	GPIO_R1_TO_BB_CH9_COEX	R1_TO_BB_GRANT
103	96	GPIO_R1_TO_WLAN_COEX	R1_TO_WLAN_COEX
103	96	GPIO_BB_TO_R1_COEX	BB_TO_R1_LAA_REQ
103	22	GPIO_AOP_TO_R1_TIME_SYNC_L	AOP_TO_R1_TIME_SYNC
103	96	IO_BT_TO_R1_TIME_SYNC	BT_TO_R1_TIME_SYNC
103	93	IO_BT_TO_R1_WAKE	BT_TO_R1_WAKE
103	0	SWD_AP_BI_R1_SWDIO	SWD_AOP_BI_R1_SWDIO
103	95	25	0	SWD_AP_TO_MANY_SWCLK	SWD_AOP_TO_MANY_SWCLK
104	84	50_TRX_R1_AOA1	50_R1_ANT0
104	84	50_TRX_R1_AOA2	50_R1_ANT1
104	84	50_TRX_R1_AOA3	50_R1_ANT3
104	100	50_TRX_R1_ANT2_CH9	50_R1_ANT_CH9
104	100	50_TRX_R1_ANT2_CH5	50_LAA_TO_R1
103	96	UAT_TUNER_TO_R1_STATE	TUNER_TO_R1_STATE
103	100	93	IO_R1_TO_BB_LAA_SW_CTRL	R1_TO_BB_LAA_SW_CTRL

hier_arrow

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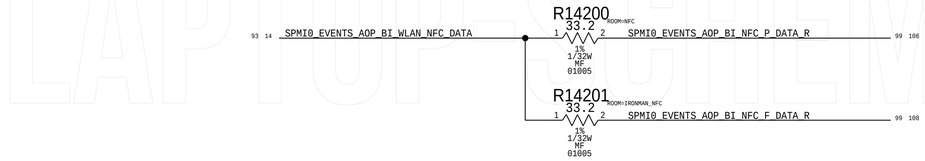
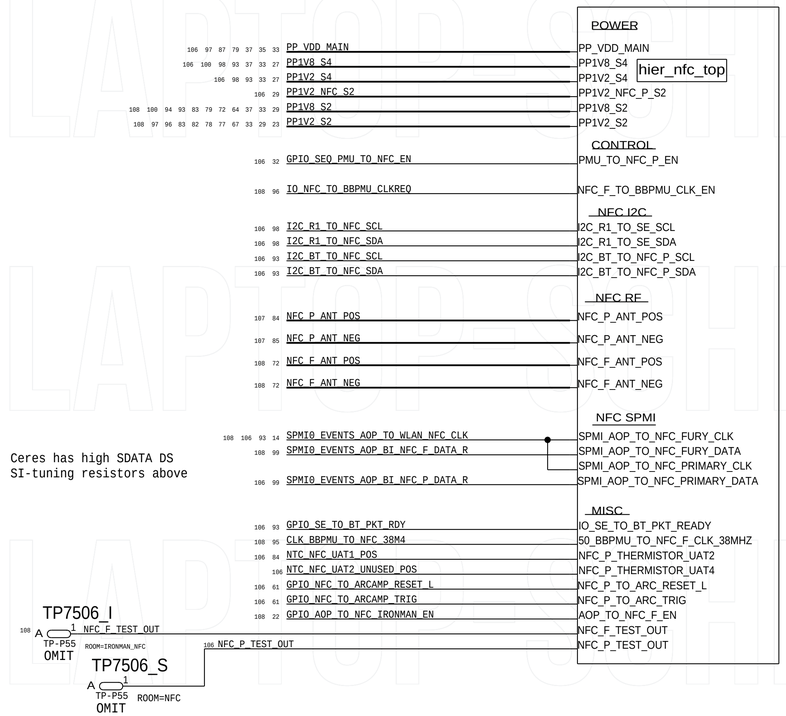
NFC Hierarchy





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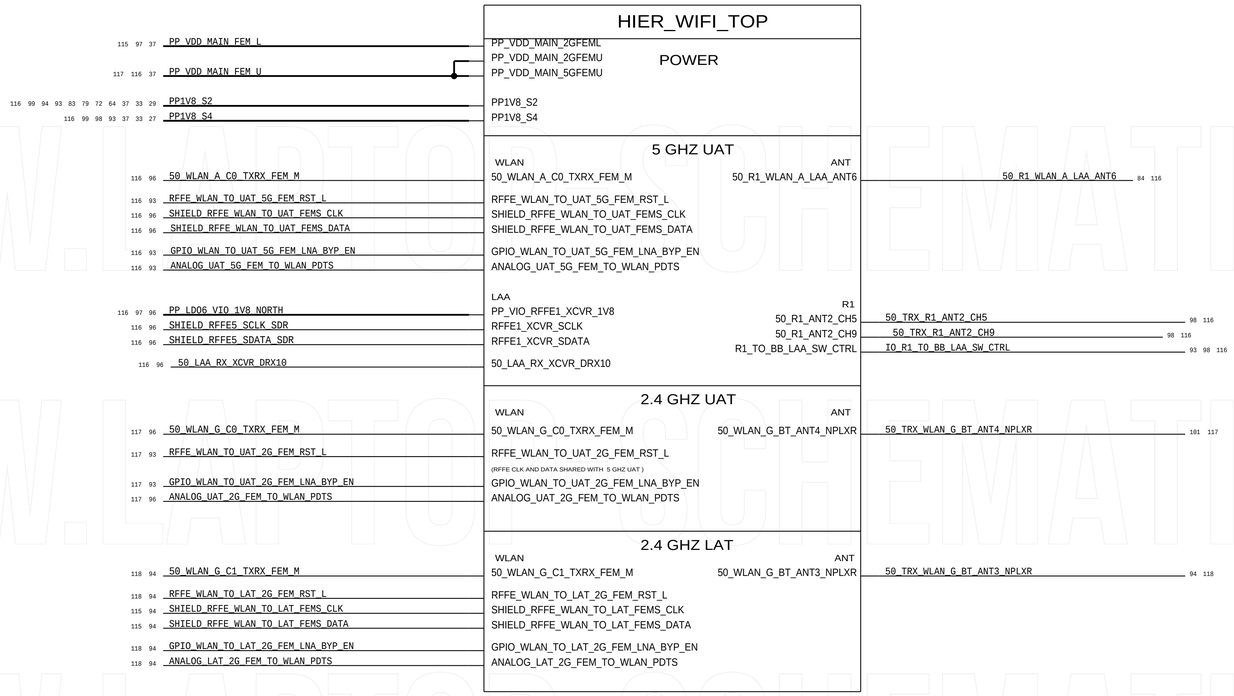
WiFi Hierarchy



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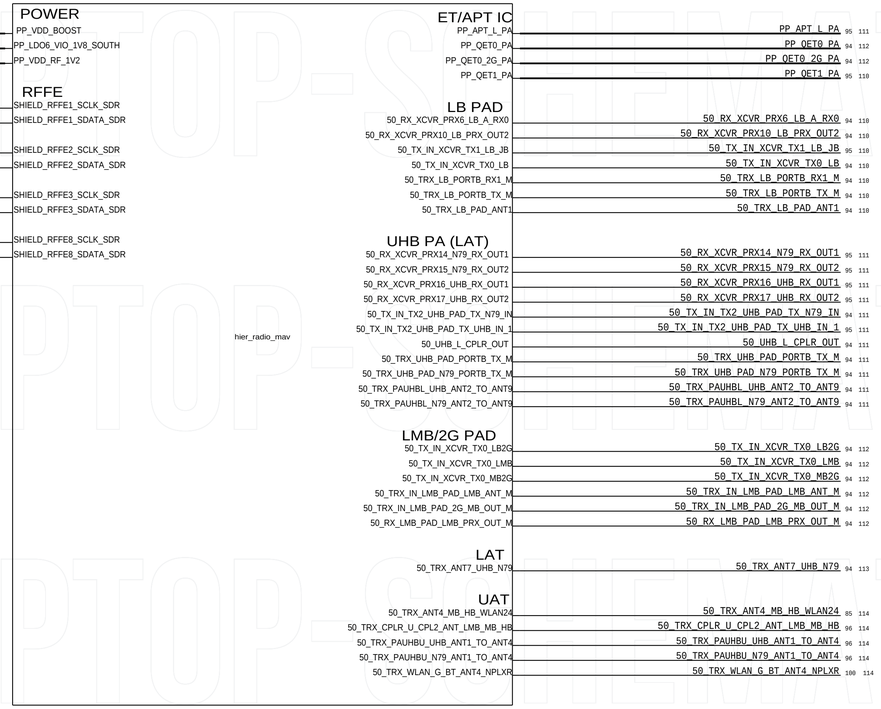
Radio Hierarchy



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103	2	MODULE		
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POWER
- 103 98 IO PP1V2_S4
- 103 98 IO PP1V8_S4
- 103 98 IO PP1V0_R1_ANA_S4
- 103 98 IO PP1V0_S4

HOST IPC
- 103 98 IO SPI0_AOP_TO_IMU_R1_SCLK
- 103 98 IO GPIO_SCM_AOP_TO_R1_SPI_CS_L
- 103 98 IO SPI0_AOP_FROM_IMU_R1_MISO
- 103 98 IO SPI0_AOP_TO_IMU_R1_MOSI
- 103 98 IO GPIO_AOP_TO_R1_COREDUMP_TRIGGER
- 103 98 IO GPIO_SCM_AOP_FROM_R1_INT

RESET/CLOCK
- 103 98 IO GPIO_S4_PMU_TO_R1_RESET_L
- 103 98 IO CLK_GPIO_S4_PMU_TO_WLAN_R1_32K
- 103 98 IO GPIO_AOP_TO_R1_TIME_SYNC_L

DEBUG
- 103 98 IO SWD_AP_TO_MANY_SWCLK
- 103 98 IO SWD_AP_BI_R1_SWDIO

SPMI/COEX GPIOS
- 103 98 IO GPIO_WLAN_TO_R1_COEX
- 103 98 IO GPIO_R1_TO_BB_CH9_COEX
- 103 98 IO GPIO_R1_TO_WLAN_COEX
- 103 98 IO GPIO_BB_TO_R1_COEX
- 103 98 IO GPIO_BB_TO_R1_CH9_REQ

SE IPC
- 103 98 IO I2C_R1_TO_NFC_SCL
- 103 98 IO I2C_R1_TO_NFC_SDA

BT TIME SYNC / WAKE
- 103 98 IO IO_BT_TO_R1_TIME_SYNC
- 103 98 IO IO_BT_TO_R1_WAKE

ANTENNA SWITCH CTRL
- 103 98 IO UAT_TUNER_TO_R1_STATE
- 103 98 IO IO_R1_TO_BB_LAA_SW_CTRL

ANTENNA
- 104 98 IO 50_TRX_R1_AOA1
- 104 98 IO 50_TRX_R1_AOA2
- 104 98 IO 50_TRX_R1_AOA3
- 104 98 IO 50_TRX_R1_ANT2_CH9
- 104 98 IO 50_TRX_R1_ANT2_CH5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00775	339S00774	?	U_ROSE_R	USI STRIDER2 MODULE

SCH #: 951-09582
PCB #: 920-05369
BOM #: 939-05686

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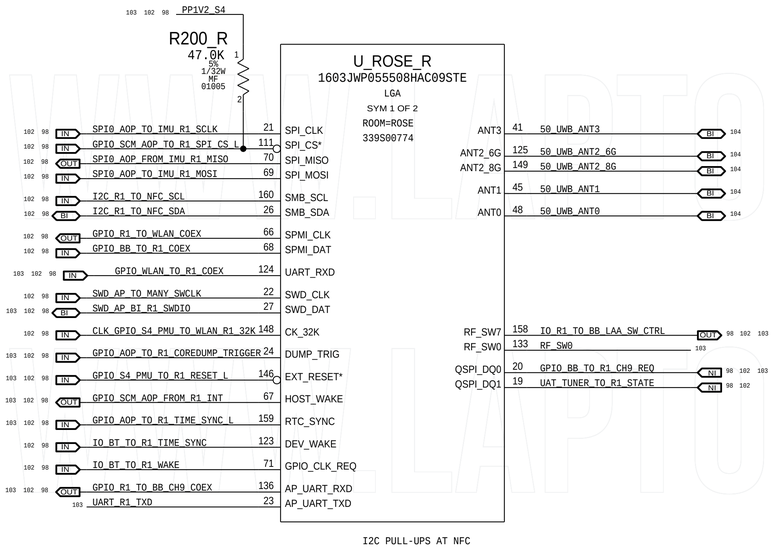
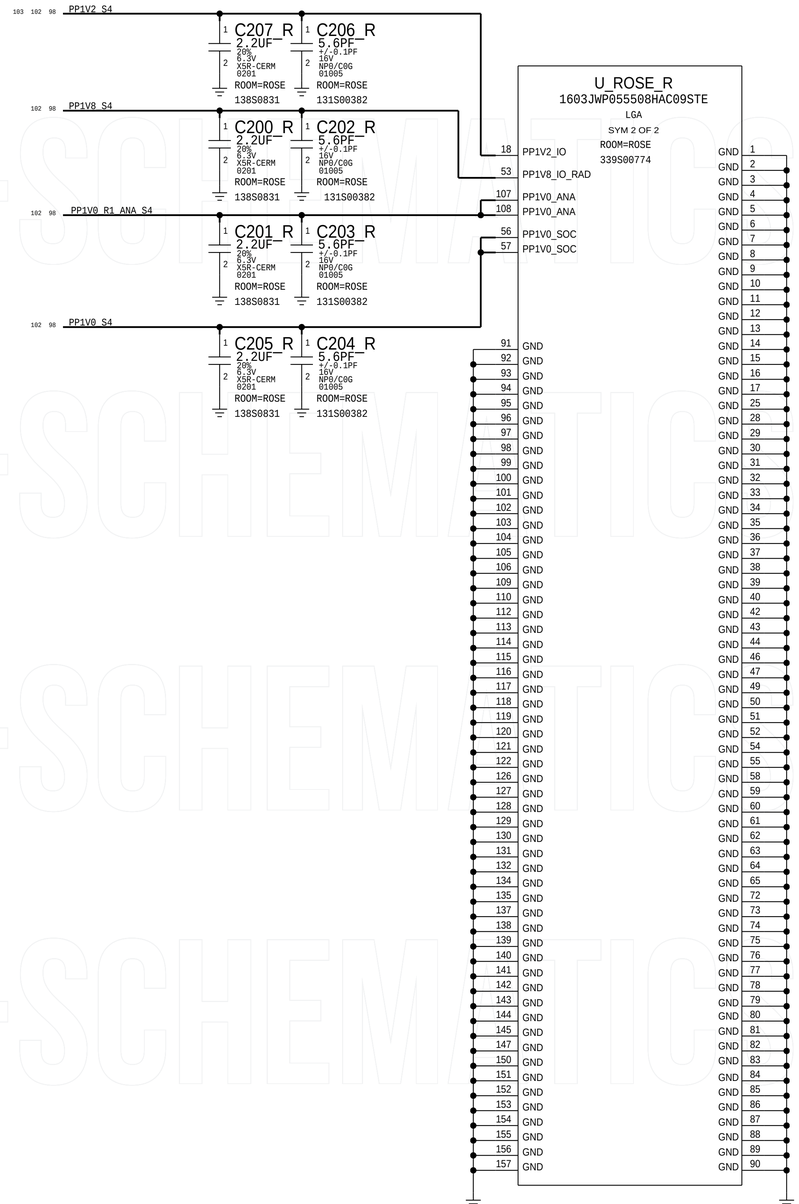
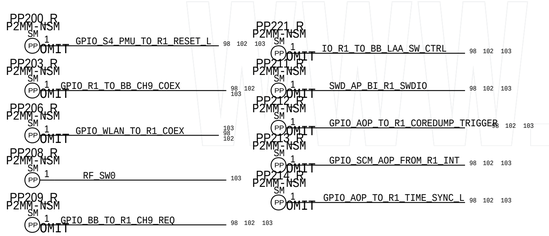
MODULE

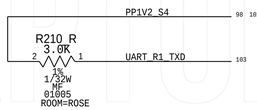


I2C PULL-UPS AT NFC





UNSECURE BOOT BOOTSTRAP PULLUP



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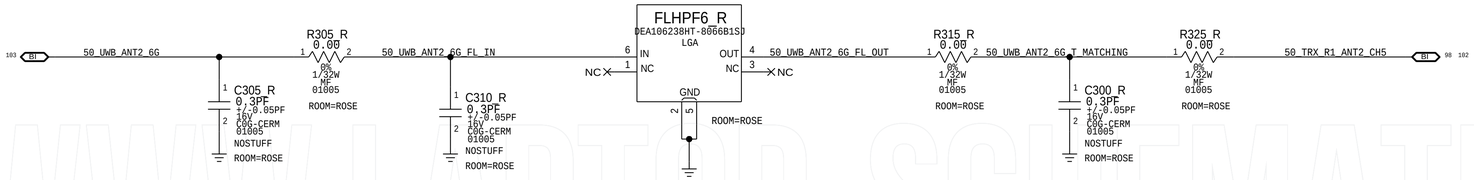

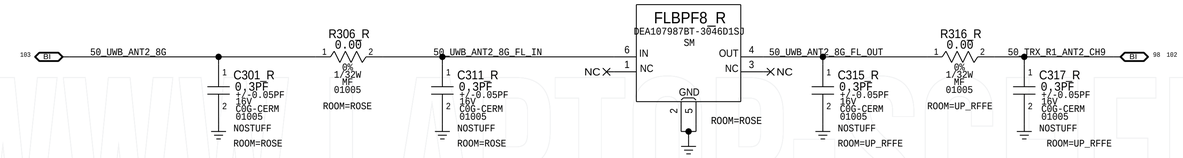

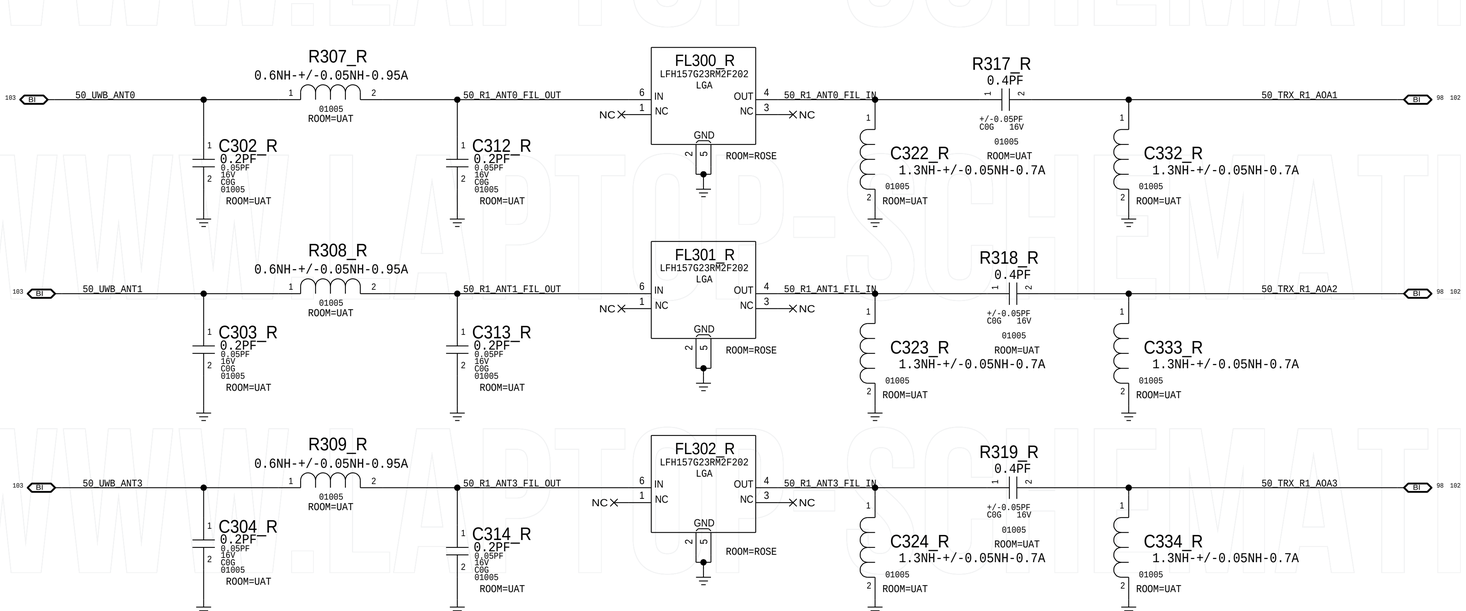

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HIER_NFC

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FURY CHIP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00611	1	IC,SN211V,A0,FURY,NO SE	NFC_F	?
998-19915	1	IC,SN210V,B1,CERES,DEVKEY,V7	NFC_F	NOSTUFF

D53 PRIMARY MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00025	2	CAP,CER,C0G,1000PF,2%25V,0201	C7510_S,C7513_S	?
131S00016	2	CAP,CER,C0G,470PF,2%25V,0201	C7550_S,C7551_S	?
152S01116	2	IND,82NH,2.5%,0.55A,0402	L7500_S,L7501_S	?
131S0882	2	CAP,CER,C0G,390PF,2%,25V,0201	C7514_S,C7542_S	?
131S0583	2	CAP,CER,C0G,4.7PF,2%,25V,0201	C7512_S,C7541_S	NOSTUFF
131S0883	1	CAP,CER,C0G,220PF,2%,50V,0201	C7546_S	?
131S0883	1	CAP,CER,C0G,220PF,2%,50V,0201	C7547_S	?
131S00017	1	CAP,CER,C0G,47PF,2%,50V,0201	C7548_S	?
131S0583	1	CAP,CER,C0G,4.7PF,2%,25V,0201	C7558_S	NOSTUFF

D53 FURY MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00025	2	CAP,CER,C0G,1000PF,2%25V,0201	C7510_I,C7513_I	NOSTUFF
131S00016	2	CAP,CER,C0G,470PF,2%25V,0201	C7550_I,C7551_I	?
152S01117	2	IND,91NH,2.5%,0.55A,0402	L7500_I,L7501_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7514_I,C7542_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7515_I,C7543_I	NOSTUFF
131S0583	2	CAP,CER,C0G,4.7PF,2%,25V,0201	C7512_I,C7541_I	NOSTUFF
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7545_I,C7565_I	NOSTUFF
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7546_I,C7566_I	?
131S00026	2	CAP,CER,C0G,820PF,2%,25V,0201	C7547_I,C7567_I	?
131S00017	2	CAP,CER,C0G,47PF,2%,50V,0201	C7548_I,C7568_I	?

XTAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00077	197S00206	?	Y7500_S	XTAL,27P12 MHZ
197S00076	197S00206	?	Y7500_S	XTAL,27P12 MHZ

BALUN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S00040	157S00035	?	T7500_S	ATB16106HD-15011-T10

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108 106 99 IN PP_VDD_MAIN VOLTAGE=3.8
106 99 IN PP1V2_NFC_S2 VOLTAGE=1.2
106 99 IN PP1V8_S4 VOLTAGE=1.8
106 99 IN PP1V2_S4 VOLTAGE=1.2
108 99 IN PP1V8_S2 VOLTAGE=1.8

106 99 IO I2C_R1_TO_NFC_SCL
106 99 IO I2C_R1_TO_NFC_SDA
106 99 IO I2C_BT_TO_NFC_SCL
106 99 IO I2C_BT_TO_NFC_SDA

106 99 IN SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
106 99 IN SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R
108 99 IN SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
108 99 IN SPMI0_EVENTS_AOP_BI_NFC_F_DATA_R

106 99 IN GPIO_SEQ_PMU_TO_NFC_EN

106 99 IN NTC_NFC_UAT2_UNUSED_POS
106 99 IN NTC_NFC_UAT1_POS

106 99 OUT GPIO_SE_TO_BT_PKT_RDY
106 99 OUT GPIO_NFC_TO_ARCAMP_RESET_L
106 99 OUT GPIO_NFC_TO_ARCAMP_TRIG
107 99 IO NFC_P_ANT_POS
107 99 IO NFC_P_ANT_NEG
106 99 IO NFC_P_TEST_OUT

108 99 IO NFC_F_ANT_POS
108 99 IO NFC_F_ANT_NEG
108 99 IN PP1V2_S2 VOLTAGE=1.2
108 99 IN GPIO_AOP_TO_NFC_IRONMAN_EN
108 99 IN CLK_BBPMU_TO_NFC_38M4
108 99 OUT IO_NFC_TO_BBPMU_CLKREQ
108 99 IO NFC_F_TEST_OUT

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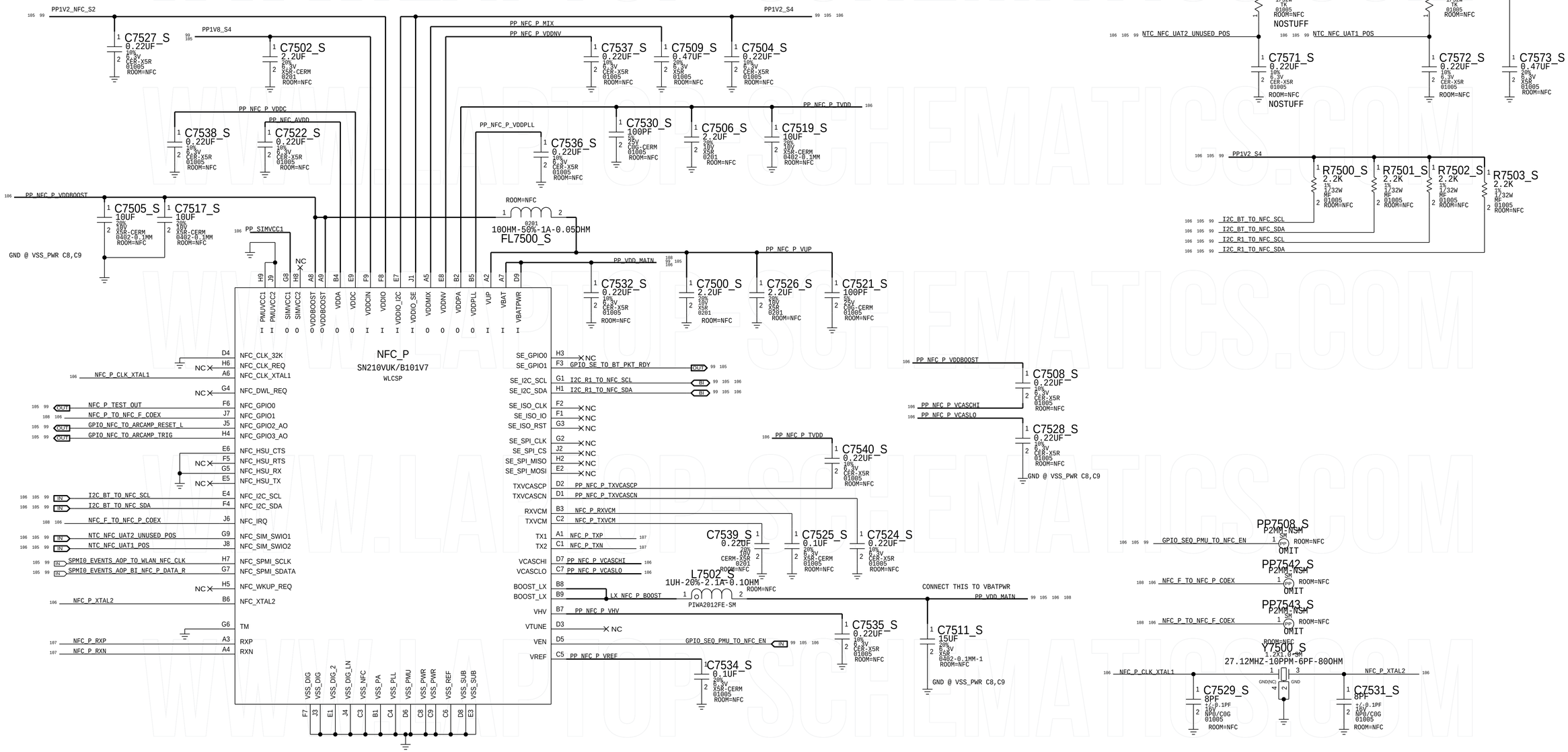
STOCKHOLM

PRIMARY NFC CONTROLLER



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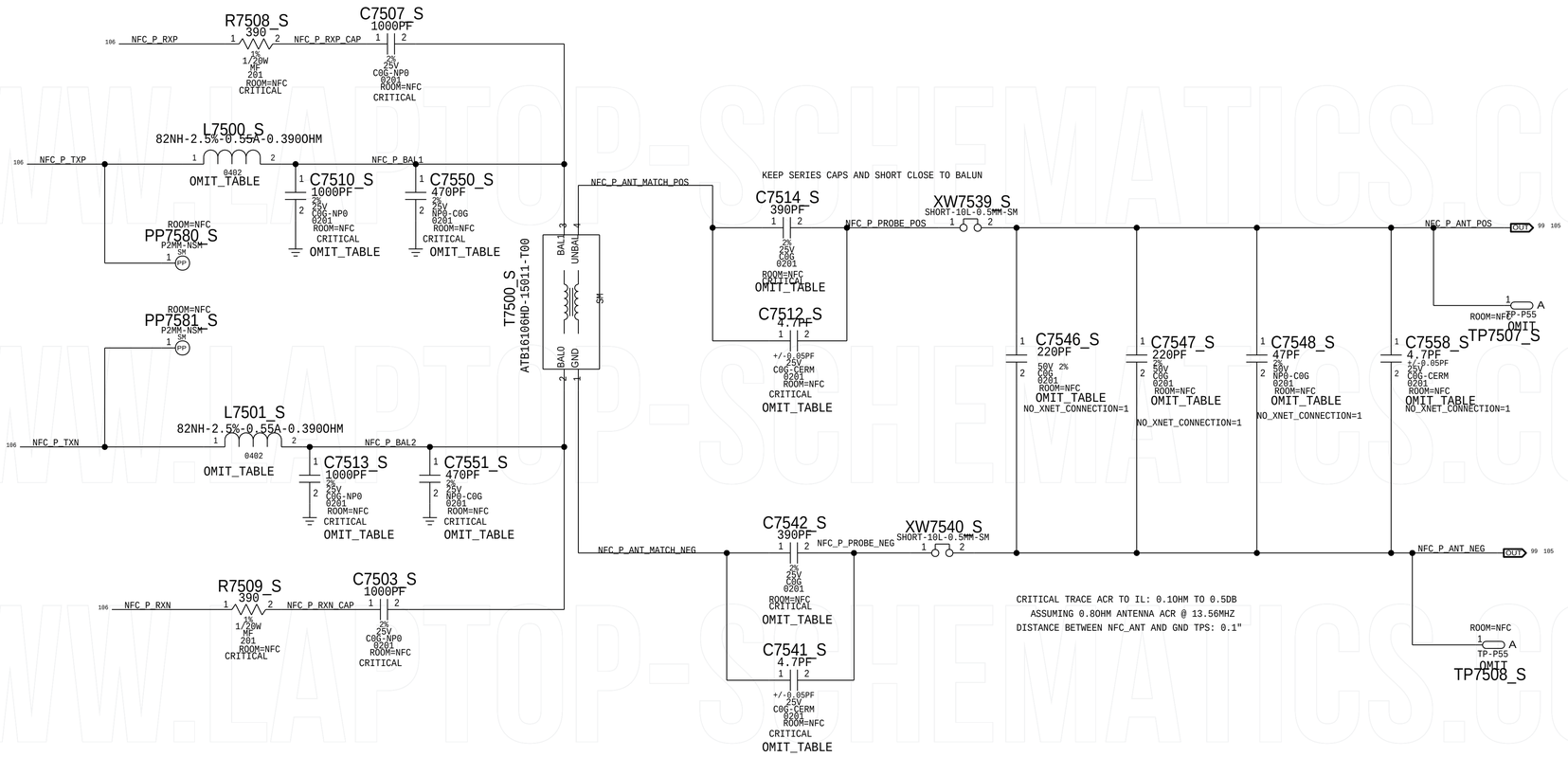
PRIMARY NFC FRONT END



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STOCKHOLM

FURY NFC CONTROLLER

FURY NFC FRONT END

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PP1V2_S2
PP1V8_S2
C7527_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7502_I 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=IRONMAN_NFC
PP_NFC_F_VDDC
PP_NFC_F_AVDD
C7538_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7522_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
PP_NFC_F_VDDBOOST
C7505_I 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=IRONMAN_NFC
C7517_I 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=IRONMAN_NFC
GROUND @ VSS_PWR AT C8,C9
PP_NFC_F_MIX
PP_NFC_F_VDDNV
C7537_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7509_I 0.47UF 20% 6.3V X5R 01005 ROOM=IRONMAN_NFC
PP_NFC_F_VDDPLL
PP_NFC_F_TVDD
C7536_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7530_I 100PF 5% 25V C0G-CERM 01005 ROOM=IRONMAN_NFC
C7506_I 2.2UF 20% 10V X5R 0201 ROOM=IRONMAN_NFC
C7519_I 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=IRONMAN_NFC
FL7500_I 0201 100HM-50%-1A-0.05OHM ROOM=IRONMAN_NFC
PP_VDD_MAIN
PP_NFC_F_VUP
C7532_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7500_I 2.2UF 20% 10V X5R 0201 ROOM=IRONMAN_NFC
C7526_I 2.2UF 20% 10V X5R 0201 ROOM=IRONMAN_NFC
C7521_I 100PF 5% 25V C0G-CERM 01005 ROOM=IRONMAN_NFC

NFC_F
SN210VUK/B101V7
WLCSP
OMIT_TABLE

H9	PMUVCC1	I	
J9	PMUVCC2	I	
G8	SIMVCC1	I	
H8	SIMVCC2	I	
A8	VDDBOOST	O	
A9	VDDBOOST	O	
B4	VDDA	O	
E9	VDDC	O	
F9	VDDCIN	I	
F8	VDDIO	I	
E7	VDDIO_I2C	I	
J1	VDDIO_SE	I	
A5	VDDMIX	O	
E8	VDDNV	O	
B2	VDDPA	O	
B5	VDDPLL	O	
A2	VLIP	I	
A7	VBAT	I	
D9	VBATPWR	I	

D4	NFC_CLK_32K	
H6	NFC_CLK_REQ	IO_NFC_TO_BBPMU_CLKREQ
A6	NFC_CLK_XTAL1	NFC_F_CLK_XTAL1
G4	NFC_DWL_REQ	NC
F6	NFC_GPIO0	NFC_F_TEST_OUT
J7	NFC_GPIO1	NFC_F_TO_NFC_P_COEX
J5	NFC_GPIO2_AO	NC
H4	NFC_GPIO3_AO	NC
E6	NFC_HSU_CTS	
F5	NFC_HSU_RTS	NC
G5	NFC_HSU_RX	
E5	NFC_HSU_TX	NC
E4	NFC_I2C_SCL	NC
F4	NFC_I2C_SDA	NC
J6	NFC_IRQ	NFC_P_TO_NFC_F_COEX
G9	NFC_SIM_SWIO1	NC
J8	NFC_SIM_SWIO2	NC
H7	NFC_SPMI_SCLK	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
G7	NFC_SPMI_SDATA	SPMI0_EVENTS_AOP_BI_NFC_F_DATA_R
H5	NFC_WKUP_REQ	NC
B6	NFC_XTAL2	NC
G6	TM	
A3	RXP	NFC_F_RXP
A4	RXN	NFC_F_RXN

H3	SE_GPIO0	NC
F3	SE_GPIO1	NC
G1	SE_I2C_SCL	NC
H1	SE_I2C_SDA	NC
F2	SE_ISO_CLK	NC
F1	SE_ISO_IO	NC
G3	SE_ISO_RST	NC
G2	SE_SPI_CLK	NC
J2	SE_SPI_CS	NC
H2	SE_SPI_MISO	NC
E2	SE_SPI_MOSI	NC
D2	TXVCASCP	PP_NFC_F_TXVCASCP
D1	TXVCASCN	PP_NFC_F_TXVCASCN
B3	RXVCM	NFC_F_RXVCM
C2	TXVCM	NFC_F_TXVCM
A1	TX1	NFC_F_TXP
C1	TX2	NFC_F_TXN
D7	VCASCHI	PP_NFC_F_VCASCHI
C7	VCASCLO	PP_NFC_F_VCASLO
B8	BOOST_LX	
B9	BOOST_LX	LX_NFC_F_BOOST
B7	VHV	PP_NFC_F_VHV
D3	VTUNE	NC
D5	VEN	GPIO_AOP_TO_NFC_IRONMAN_EN
C5	VREF	PP_NFC_F_VREF

F7	VSS_DIG	
J3	VSS_DIG	
E1	VSS_DIG_2	
J4	VSS_DIG_LN	
C3	VSS_NFC	
B1	VSS_PA	
C4	VSS_PLL	
D6	VSS_PMU	
C8	VSS_PWR	
C9	VSS_PWR	
C6	VSS_REF	
D8	VSS_SUB	
E3	VSS_SUB	

C7540_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7539_I 0.22UF 20% 10V CERM-X5R 0201 ROOM=IRONMAN_NFC
C7525_I 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=IRONMAN_NFC
C7524_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
L7502_I 1UH-20%-2.1A-0.1OHM PIWA2012FE-SM ROOM=IRONMAN_NFC
C7534_I 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=IRONMAN_NFC
R7569_I 100K 5% 1/32W MF 01005 ROOM=IRONMAN_NFC
C7535_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7511_I 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=IRONMAN_NFC
GROUND @ VSS_PWR AT C8,C9
PP7540_I P2MM-NSM SM ROOM=IRONMAN_NFC OMIT
R7510_I 0.00 0% 1/32W MF 01005 ROOM=IRONMAN_NFC
CLK_BBPMU_TO_NFC_38M4
NFC_F_CLK_XTAL1
C7508_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
C7528_I 0.22UF 10% 6.3V CER-X5R 01005 ROOM=IRONMAN_NFC
GROUND @ VSS_PWR AT C8,C9

R7508_I 390 1% 1/20W MF 201 ROOM=IRONMAN_NFC CRITICAL
C7507_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL
L7500_I 91NH-2.5%-0.55A-0.351OHM 0402 ROOM=IRONMAN_NFC OMIT_TABLE
C7510_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7550_I 470PF 5% 25V NP0-C0G 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
PP7580_I P2MM-NSM SM ROOM=IRONMAN_NFC
L7501_I 91NH-2.5%-0.55A-0.351OHM 0402 ROOM=IRONMAN_NFC OMIT_TABLE
C7513_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7551_I 470PF 5% 25V NP0-C0G 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
PP7581_I P2MM-NSM SM ROOM=IRONMAN_NFC
R7509_I 390 1% 1/20W MF 201 ROOM=IRONMAN_NFC CRITICAL
C7503_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL
C7515_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7514_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7512_I 4.7PF +/-0.05PF 25V C0G-CERM 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7542_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7541_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7543_I 4.7PF +/-0.05PF 25V C0G-CERM 0201 ROOM=IRONMAN_NFC CRITICAL OMIT_TABLE
C7545_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7546_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7547_I 820PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7548_I 47PF 5% 50V NP0-C0G 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7565_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7566_I 1000PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7567_I 820PF 2% 25V C0G-NP0 0201 ROOM=IRONMAN_NFC OMIT_TABLE
C7568_I 47PF 5% 50V NP0-C0G 0201 ROOM=IRONMAN_NFC OMIT_TABLE
TP7507_I OMIT TP-P55 ROOM=IRONMAN_NFC
TP7508_I OMIT TP-P55 ROOM=IRONMAN_NFC

NFC_F_RXP
NFC_F_RXP_CAP
NFC_F_TXP
NFC_F_TXN
NFC_F_RXN
NFC_F_RXN_CAP
NFC_F_ANT_MATCH_POS
NFC_F_ANT_POS
NFC_F_ANT_NEG
NFC_F_ANT_MATCH_NEG
DISTANCE BETWEEN NFC_ANT AND GND TPS: 0.1"

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
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MAV20 HIER_RADIO_MAV_TOP

LAST_MODIFICATION=Fri Apr 3 17:41:41 2020

X1803

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113	36	LOWER ANTENNA FEEDS_ANT7		07/30/2019
114	39	UPPER ANTENNA FEEDS_ANT4		07/30/2019

POWER

PP_LDO6_VIO_1V8_SOUTH	VOLTAGE=1.8	IN	101 110 111 112
PP_VDD_RF_1V2	VOLTAGE=1.2	IN	101 110 111 112
PP_VDD_BOOST	VOLTAGE=4.5	IN	101 110 111 112

ET/APT IC

PP_APT_L_PA	VOLTAGE=4.5	OUT	101 111
PP_QET0_PA	VOLTAGE=5.8V	OUT	101 112
PP_QET0_2G_PA	VOLTAGE=5.8V	OUT	101 112
PP_QET1_PA	VOLTAGE=5.8V	OUT	101 110

RF RFFE

SHIELD_RFFE1_SCLK_SDR	IN	101 112
SHIELD_RFFE1_SDATA_SDR	IO	101 112
SHIELD_RFFE2_SCLK_SDR	IN	101 111
SHIELD_RFFE2_SDATA_SDR	IO	101 111
SHIELD_RFFE3_SCLK_SDR	IN	101 110 111 112
SHIELD_RFFE3_SDATA_SDR	IO	101 110 111 112
SHIELD_RFFE8_SCLK_SDR	IN	101 110
SHIELD_RFFE8_SDATA_SDR	IO	101 110

LB PAD

50_RX_XCVR_PRX6_LB_A_RX0	OUT	101 110
50_RX_XCVR_PRX10_LB_PRX_OUT2	OUT	101 110
50_TX_IN_XCVR_TX1_LB_JB	IN	101 110
50_TX_IN_XCVR_TX0_LB	IN	101 110
50_TRX_LB_PORTB_RX1_M	OUT	101 110
50_TRX_LB_PORTB_TX_M	IO	101 110
50_TRX_LB_PAD_ANT1	OUT	101 110

UHB PA (LAT)

50_RX_XCVR_PRX14_N79_RX_OUT1	OUT	101 111
50_RX_XCVR_PRX15_N79_RX_OUT2	OUT	101 111
50_RX_XCVR_PRX16_UHB_RX_OUT1	OUT	101 111
50_RX_XCVR_PRX17_UHB_RX_OUT2	OUT	101 111
50_TX_IN_TX2_UHB_PAD_TX_N79_IN	IN	101 111
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	IN	101 111
50_UHB_L_CPLR_OUT	OUT	101 111
50_TRX_UHB_PAD_PORTB_TX_M	IO	101 111
50_TRX_UHB_PAD_N79_PORTB_TX_M	IO	101 111
50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	IO	101 111
50_TRX_PAUHBL_N79_ANT2_TO_ANT9	IO	101 111

LMB/2G PAD

50_TX_IN_XCVR_TX0_LB2G	IN	101 112
50_TX_IN_XCVR_TX0_LMB	IN	101 112
50_TX_IN_XCVR_TX0_MB2G	IN	101 112
50_TRX_IN_LMB_PAD_LMB_ANT_M	IN	101 112
50_TRX_IN_LMB_PAD_2G_MB_OUT_M	IN	101 112
50_RX_LMB_PAD_LMB_PRX_OUT_M	IO	101 112

LAT

50_TRX_ANT7_UHB_N79	IO	101 113

UAT

50_TRX_ANT4_MB_HB_WLAN24	IO	101 114
50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	IO	101 114
50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	IO	101 114
50_TRX_PAUHBU_N79_ANT1_TO_ANT4	IO	101 114
50_TRX_WLAN_G_BT_ANT4_NPLXR	IO	101 114

SCH #: 951-10915

FRONT PAGE

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LB PAD

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S02386	1	IC,LB PAD,SKY58240,WW,DSMBGA84	PA_LB_E	RF_SKU:WWBRF_SKU:WW+ROLKATA
353S02387	1	IC,LB PAD,SKY58241,ROW,DSMBGA84	PA_LB_E	RF_SKU:ROW

109 101 PP_QET1_PA
112 111 109 101 PP_VDD_BOOST

C2004_E 0.1UF 20% 6.3V X5R-CERM 01005 LBPAD
C2009_E 47PF 5% 16V NP0-C0G 01005 LBPAD
C2001_E 24PF 5% 16V C0G 01005 LBPAD

112 111 110 109 101 PP_LDO6_VIO_1V8_SOUTH
109 101 SHIELD_RFFE8_SCLK_SDR
109 101 SHIELD_RFFE8_SDATA_SDR

C2007_E 47PF 5% 16V NP0-C0G 01005 LBPAD NOSTUFF
C2006_E 47PF 5% 16V NP0-C0G 01005 LBPAD NOSTUFF
C2005_E 47PF 5% 16V NP0-C0G 01005 LBPAD

112 111 110 109 101 PP_LDO6_VIO_1V8_SOUTH
112 111 109 101 SHIELD_RFFE3_SCLK_SDR
112 111 109 101 SHIELD_RFFE3_SDATA_SDR

C2008_E 47PF 5% 16V NP0-C0G 01005 LBPAD NOSTUFF
C2003_E 47PF 5% 16V NP0-C0G 01005 LBPAD NOSTUFF

PA_LB_E
SKY58240
DSBGA
SYM 1 OF 2

K10 SDATA_RX
K9 SCLK_RX
K11 VIO_RX
K7 SDATA_TX
K6 SCLK_TX
K8 VIO_TX
K4 VBIAS
G3 VCC1
G2 VCC2
K13 VDD_LNA

VDD_LNA_LB_PAD
C2010_E 47PF 5% 16V NP0-C0G 01005 LBPAD
XR2006_E SHORT-01005-NOSMXWEB 998-19685 LBPAD
PP_VDD_RF_1V2 101 109 111 112

109 101 50_TX_IN_XCVR_TX0_LB
FROM XCVR
R2003_E 0.00 0% 1/32W MF 01005 LBPAD
50_TX_IN_TX0_LB_PAD_TX_LB_IN
K2 TX_LB_IN

PART_NUMBER=353S02386
SHIELD=YES
BOMOPTION=OMIT_TABLE
ROOM=LBPAD

USID RX=0X01
USID TX=0X01

112 50_TRX_IN_LMB_PAD_2G_LB_OUT_M
FROM 2G PA
152S00504
R2004_E 3.0NH-+/-0.1NH-0.45A-0.20HM 01005 LBPAD
50_TRX_LB_PAD_TX_2G_IN
B7 TX_2G_IN

109 101 50_RX_XCVR_PRX6_LB_A_RX0
TO XCVR
R2005_E 0.00 0% 1/32W MF 01005 LBPAD
50_RX_LB_PAD_PRX_OUT
H13 PRX_OUT1

109 101 50_RX_XCVR_PRX10_LB_PRX_OUT2
FROM XCVR
R2002_E 0.00 0% 1/32W MF 01005 LBPAD
50_RX_XCVR_PRX10_LB_PRX_OUT2_M
G13 PRX_OUT2

109 101 50_TX_IN_XCVR_TX1_LB_JB
FROM XCVR
R2009_E 0.00 0% 1/32W MF 01005 LBPAD
50_TX_IN_XCVR_TX1_LB_JB_M
L2 TX_LB_IN2

DRX_OUT F13 50_TRX_LB_PORTB_RX1
152S00422
R2007_E 1.5NH-+/-0.1NH-0.70A 01005 LBPAD
50_TRX_LB_PORTB_RX1_M 101 109
TO LB DSM
L2001_E 10NH-+/-3%-0.25A 01005 NOSTUFF LBPAD

ANT1 B13 50_TRX_LB_PAD_ANT1 101 109
LB LMB/MB/HB DPLX -> CPLR_L -> ANT1

ANT2 D13 50_TRX_LB_PORTB_TX_ANT2
R2008_E 1.5NH-+/-0.1NH-0.70A 01005 LBPAD 152S00422
50_TRX_LB_PORTB_TX_M 101 109
TO LB DSM TXIN
L2002_E 10NH-+/-3%-0.25A 01005 NOSTUFF LBPAD

PART_NUMBER=353S02386
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LBPAD

PA_LB_E
SKY58240
DSBGA
SYM 2 OF 2

A1	GND	GND	H6
A2	GND	GND	H7
A3	GND	GND	H14
A4	GND	GND	J1
A5	GND	GND	J2
A6	GND	GND	J3
A7	GND	GND	J4
A8	GND	GND	J5
A9	GND	GND	J6
A10	GND	GND	J7
A11	GND	GND	J13
A12	GND	GND	J14
A13	GND	GND	K1
A14	GND	GND	K3
B1	GND	GND	K5
B2	GND	GND	K12
B14	GND	GND	K14
C1	GND	GND	L1
C13	GND	GND	L3
C14	GND	GND	L4
D1	GND	GND	L5
D14	GND	GND	L6
E1	GND	GND	L7
E13	GND	GND	L8
E14	GND	GND	L9
F1	GND	GND	L10
F14	GND	GND	L11
G1	GND	GND	L12
G4	GND	GND	L13
G5	GND	GND	L14
G14	GND		
H1	GND		
H2	GND		
H3	GND		
H4	GND		
H5	GND		

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UHB LAT PAD

PP_LDO6_VIO_1V8_SOUTH
SHIELD_RFFE2_SCLK_SDR
SHIELD_RFFE2_SDATA_SDR
PP_LDO6_VIO_1V8_SOUTH
SHIELD_RFFE3_SCLK_SDR
SHIELD_RFFE3_SDATA_SDR

PP_VDD_BOOST
PP_APT_L_PA
PP_VDD_RF_1V2

SDATA_RX D4
SCLK_RX E4
VIO_RX C4
SDATA_TX D9
SCLK_TX E9
VIO_TX C9
VBIAS C6
VCC1 F7
VCC2 G7
VDD_LNA C7

PART_NUMBER=353S02389
SHIELD=YES
ROOM=UHB_LAT

PAUHBL_E
SKY58245-17
DSBGA
SYM 1 OF 2

USID RX=0X06
USID TX=0X06

VDD_LNA_UHB_PAD

138S0706 C2211_E 1.0UF 20% 10V X5R-CERM 0201-1
131S00353 C2212_E 10PF 5% 16V NP0/C0G 01005
C2208_E 1.0UF 20% 10V X5R-CERM 0201-1
C2207_E 1000PF 10% 6.3V X5R-CERM 01005
UHB_LAT

XR2207_E
SHORT 01005-NOSTUFFWEB
998-19685
UHB_LAT

B1 TX_UHB_IN1
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1
FROM XCVR
TO UHBPAD

B12 TX_N79_IN1
50_TX_IN_TX2_UHB_PAD_TX_N79_IN
FROM XCVR
TO UHBPAD

UHB_ANT1 M2 50_TRX_PAUHBL_UHB_ANT1_TO_ANT7
TO UHB/N79 DPLX -> ANT7

UHB_ANT2 M3 50_TRX_PAUHBL_UHB_ANT2_TO_ANT9

C2205_E 10PF 5% 25V C0G 01005
C2203_E 18PF 5% 16V NP0/C0G 01005
C2201_E 18PF 5% 16V NP0/C0G 01005
C2206_E 10PF 5% 25V C0G 01005
C2204_E 18PF 5% 16V NP0/C0G 01005
C2202_E 18PF 5% 16V NP0/C0G 01005
UHB_LAT NOSTUFF

R2204_E 0.0OHM 0% 1/32W MF 01005 UHB_LAT
A3 RX_OUT1
50_RX_XCVR_PRX16_UHB_RX_OUT1
50_RX_UHB_PAD_UHB_RX_OUT_1
TO XCVR

R2205_E 0.0OHM 0% 1/32W MF 01005 UHB_LAT
A4 RX_OUT2
50_RX_XCVR_PRX14_N79_RX_OUT1
50_RX_UHB_PAD_N79_RX_OUT_1
TO XCVR

R2203_E 0.0OHM 0% 1/32W MF 01005 UHB_LAT
A8 RX_OUT3
50_RX_XCVR_PRX17_UHB_RX_OUT2
50_RX_UHB_PAD_UHB_RX_OUT_2
TO XCVR

R2206_E 0.0OHM 0% 1/32W MF 01005 UHB_LAT
A9 RX_OUT4
50_RX_XCVR_PRX15_N79_RX_OUT2
50_RX_UHB_PAD_N79_RX_OUT_2
TO XCVR

E12 FBRX1
50_UHB_L_CPLR_OUT
TO XCVR

EXT_CPL1 J12
EXT_CPL2 J11
NCNC

152S00496
R2209_E
0.6NH-+/-0.1NH-0.95A-0.05OHM
01005 UHB_LAT

UHB_ANT4 M5 50_TRX_UHB_PAD_PORTB_TX
50_TRX_UHB_PAD_PORTB_TX_M
TO UHB UAT PAD UHB ANT 4

C2210_E 0.5PF +/-0.05PF 16V C0G 01005 UHB_LAT NOSTUFF

N79_ANT1 M7 50_TRX_PAUHBL_N79_ANT1_TO_ANT7
TO UHB/N79 DPLX -> ANT7

N79_ANT2 M8 50_TRX_PAUHBL_N79_ANT2_TO_ANT9

152S00496
R2208_E
0.6NH-+/-0.1NH-0.95A-0.05OHM
01005 UHB_LAT

N79_ANT4 M10 50_TRX_UHB_PAD_N79_PORTB_TX
50_TRX_UHB_PAD_N79_PORTB_TX_M
TO UHB UAT PAD N79 ANT4

C2209_E 0.5PF +/-0.05PF 16V C0G 01005 UHB_LAT NOSTUFF

PAUHBL_E
SKY58245-17
DSBGA
SYM 2 OF 2
PART_NUMBER=353S02389
SHIELD=YES
ROOM=UHB_LAT

A1 GND	A2 GND	A5 GND	A6 GND
A7 GND	A11 GND	A10 GND	A12 GND
B2 GND	B3 GND	B4 GND	B5 GND
B6 GND	B7 GND	B8 GND	B9 GND
B10 GND	B11 GND	C1 GND	C2 GND
C3 GND	C5 GND	C8 GND	C10 GND
C11 GND	C12 GND	D1 GND	D2 GND
D3 GND	D5 GND	D6 GND	D7 GND
D8 GND	D10 GND	D11 GND	D12 GND
E1 GND	E2 GND	E3 GND	E5 GND
GND E6	GND E7	GND E8	GND E10
GND E11	GND F1	GND F2	GND F3
GND F4	GND F5	GND F6	GND F8
GND F9	GND F10	GND F11	GND F12
GND G1	GND G2	GND G3	GND G4
GND G5	GND G6	GND G8	GND G9
GND G10	GND G11	GND G12	GND H1
GND H12	GND J1	GND K1	GND K12
GND L1	GND M1	GND M4	GND M6
GND M9	GND M11	GND M12	

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PAGE TITLE: UHB LAT PAD

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LMB_2G_PAD

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S02393	1	IC,2G-LMB PAD,SKY58232,DSBGA79	PA_LMB_E	RF_SKU:WWRF_SKU:WW+KOLKATA
353S02401	1	IC,2G-LMB PAD,ROW,SKY58242,DSBGA79	PA_LMB_E	RF_SKU:ROW

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109 101 PP_QET0_2G_PA

131S00303 C2305_E 100PF 5% 16V NP0-C0G 01005-1 LMB_2GPAD

C2304_E 2.2UF 20% 10V X5R 0201 LMB_2GPAD

PP_VDD_BOOST 101 109 110 111

130S00071 C2306_E 4UF 20% 6.3V CER-X5R 0201 LMB_2GPAD

112 111 110 109 101 PP_LDO6_VIO_1V8_SOUTH

109 101 SHIELD_RFFE1_SCLK_SDR

109 101 SHIELD_RFFE1_SDATA_SDR

C2311_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD

C2313_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD NOSTUFF

C2302_E 10PF 2% 25V C0G 01005 LMB_2GPAD NOSTUFF

112 111 110 109 101 PP_LDO6_VIO_1V8_SOUTH

111 110 109 101 SHIELD_RFFE3_SCLK_SDR

111 110 109 101 SHIELD_RFFE3_SDATA_SDR

C2312_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD

C2301_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD NOSTUFF

C2303_E 10PF 2% 25V C0G 01005 LMB_2GPAD NOSTUFF

PP_QET0_PA 101 109

131S00382 C2314_E 5.6PF +/-0.1PF 16V NP0/C0G 01005 LMB_2GPAD

VFE_LO_1V14_LMB_PAD

XR2304_E SHORT-01005-NOSMXWEB 998-19685 LMB_2GPAD

C2315_E 1000PF 10% 6.3V X5R-CERM 01005 LMB_2GPAD

PP_VDD_RF_1V2 101 109 110 111

A7 SDATA_RX
A6 CLK_RX
A5 VIO_RX
J4 SDATA_TX
J3 SCLK_TX
J2 VIO_TX
F6 VIO_VAPT_1
F7 VIO_VAPT_2
H1 VBIAS
J6 VCC1
J7 VCC2
A9 VDD_LNA

PART_NUMBER=353S02393
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LMB_2GPAD

PA_LMB_E
SKY58232
DSBGA
SYM 1 OF 2

USID RX=0X05
USID TX=0X05

109 101 50_TX_IN_XCVR_TX0_LB2G — R2301_E 0.00 1/32W MF 01005 LMB_2GPAD — 50_TX_IN_XCVR_TX0_LB2_2G_LB_IN — C1 2G_LB_IN

FROM XCVR

109 101 50_TX_IN_XCVR_TX0_MB2G — R2302_E 0.00 1/32W MF 01005 LMB_2GPAD — 50_TX_IN_XCVR_TX0_MB2G_2G_MB_IN — D1 2G_MB_IN

FROM XCVR

NC E1 NC

109 101 50_TX_IN_XCVR_TX0_LMB — F1 TX_LMB_IN

FROM XCVR

2G_LB_OUT B11 — 50_TRX_IN_LMB_PAD_2G_LB_OUT — R2305_E 0.00 1/32W MF 01005 LMB_2GPAD — 50_TRX_IN_LMB_PAD_2G_LB_OUT_M 110 — TO LB PAD

C2307_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

2G_MB_OUT D11 — 50_TRX_IN_LMB_PAD_2G_MB_OUT — 152S00494 R2306_E 0.8NH-+/-0.1NH-0.9A-0.05OHM 01005 LMB_2GPAD — 50_TRX_IN_LMB_PAD_2G_MB_OUT_M 101 109 — TO HB PAD

C2308_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

LMB_ANT G11 — 50_TRX_IN_LMB_PAD_LMB_ANT — 152S00498 R2307_E 0.4NH-+/-0.1NH-1.0A-0.03OHM 01005 LMB_2GPAD — 50_TRX_IN_LMB_PAD_LMB_ANT_M 101 109 — TO HB PAD

C2309_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

LMB_PRX_OUT C4 — 50_RX_LMB_PAD_LMB_PRX_OUT — R2308_E 0.00 1/32W MF 01005 LMB_2GPAD — 50_RX_LMB_PAD_LMB_PRX_OUT_M 101 109 — TO HB PAD

C2310_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

PA_LMB_E
SKY58232
DSBGA
SYM 2 OF 2

PART_NUMBER=353S02393
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LMB_2GPAD

A1 A2 B3 B4 B9 B10 B12 C2 C3 C9 C10 C11 A3 C12 D2 D3 D4 D12 E2 E3 E4 E11 E12 A4 F2 F3 F4 F5 F11 GND F12 G1 G2 G3 G4 A8 G5 G6 G7 G12 H2 H3 H4 H5 H6 H7 A10 H11 H12 J1 J5 J8 J9 J10 J11 J12 A11 A12 B1 B2

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LOWER ANTENNA FEEDS: ANT7

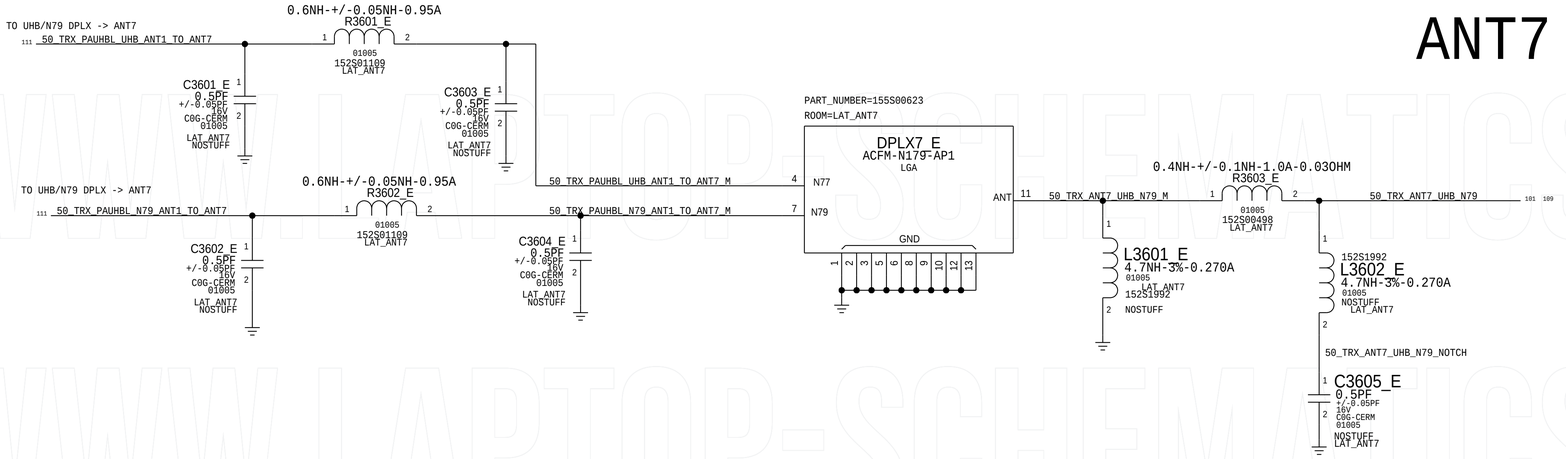
UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			

ANT7



5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

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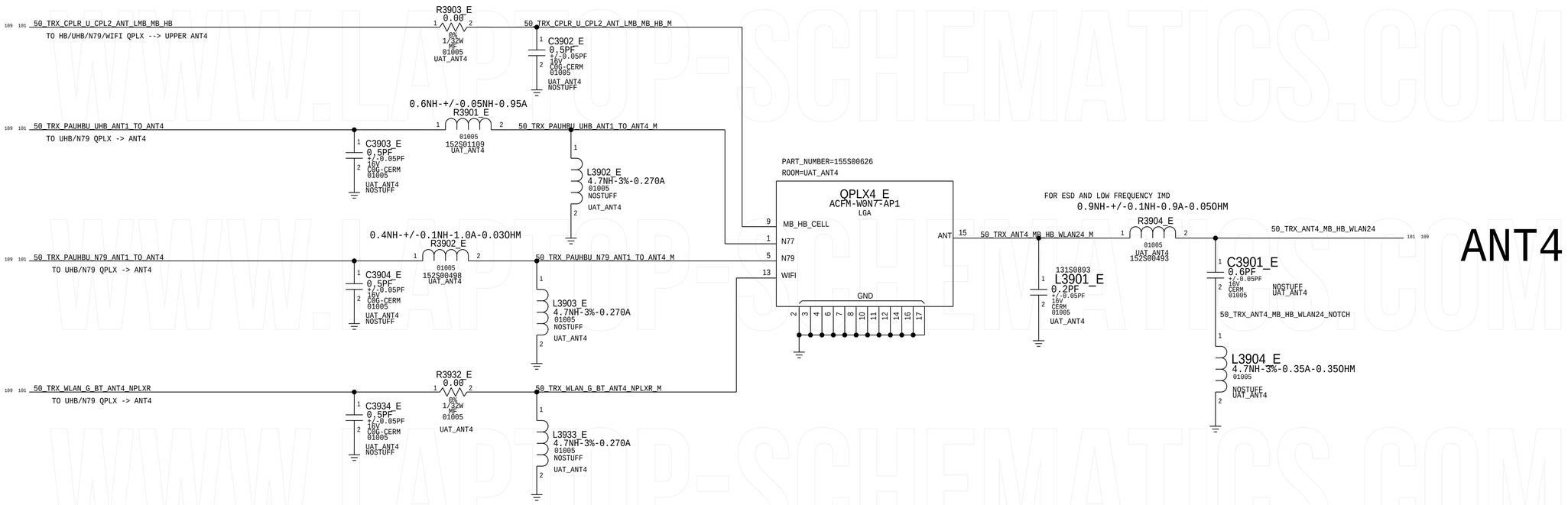
UPPER ANTENNA FEEDS



ANT4

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2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4			2020-04-03

D53 HIER_WIFI_TOP EVT

LAST_MODIFICATION=Fri Apr 3 17:53:23 2020

PAGE	CSA	CONTENTS	SYNC	DATE
115	1	Table of Contents		
116	4	5G rFEM (UAT)	D52_WIFI_MASTER_0.19.0	
117	7	2G4 rFEM (UAT)	D52_WIFI_MASTER_0.19.0	
118	8	2G4 rFEM (LAT)	D52_WIFI_MASTER_0.19.0	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00540	1	FLTR,DIPLEXER,5GHZ,BANDPAS,BRUBECK,LGA16	DPLXR_U_W	CRITICAL	

POWER

116 100 IO PP_VDD_MAIN_FEM_U VOLTAGE=3.8
117 100 IO PP_VDD_MAIN_FEM_U VOLTAGE=3.8
118 115 100 IO PP_VDD_MAIN_FEM_L VOLTAGE=3.8
117 116 100 IO PP1V8_S4 VOLTAGE=1.8
118 116 100 IO PP1V8_S2 VOLTAGE=1.8

5G RFEM (UAT)

116 100 IO 50_WLAN_A_C0_TXRX_FEM_M
116 100 IO 50_LAA_RX_XCVR_DRX10
116 100 IO 50_TRX_R1_ANT2_CH5
116 100 IO RFFE_WLAN_TO_UAT_5G_FEM_RST_L

WLAN RFFE
117 116 100 IO SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
117 116 100 IO SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
116 100 IO GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN

LAA RFFE
116 100 IO PP_LDO6_VIO_1V8_NORTH
116 100 IO SHIELD_RFFE5_SCLK_SDR
116 100 IO SHIELD_RFFE5_SDATA_SDR

116 100 IO IO_R1_TO_BB_LAA_SW_CTRL
116 100 IO ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
116 100 IO 50_TRX_R1_ANT2_CH9
116 100 IO 50_R1_WLAN_A_LAA_ANT6

2.4G RFEM (UAT)

117 100 IO 50_WLAN_G_C0_TXRX_FEM_M
117 100 IO RFFE_WLAN_TO_UAT_2G_FEM_RST_L

WLAN RFFE — WLAN RFFE CLK AND DATA SHARED WITH 5G UAT FEM

117 100 IO GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN
117 100 IO ANALOG_UAT_2G_FEM_TO_WLAN_PDTS
117 100 IO 50_TRX_WLAN_G_BT_ANT4_NPLXR

D53 SPECIFIC IMPLEMENTATION

PLACE_SIDE=TOP
OMIT SM PP230_W P2MM-NSM ROOM=LAT_FEM
PP 1 SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK 100 115 118

PLACE_SIDE=TOP
OMIT SM PP231_W P2MM-NSM ROOM=LAT_FEM
PP 1 SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA 100 115 118

118 115 100 PP_VDD_MAIN_FEM_L
C413_W 220PF 6.3V X5S 01005 ROOM=LAT_FEM

2.4G RFEM (LAT)

118 100 IO 50_WLAN_G_C1_TXRX_FEM_M
118 115 100 IO SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK

WLAN RFFE
118 115 100 IO SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA
118 100 IO RFFE_WLAN_TO_LAT_2G_FEM_RST_L

118 100 IO GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN
118 100 IO ANALOG_LAT_2G_FEM_TO_WLAN_PDTS
118 100 IO 50_TRX_WLAN_G_BT_ANT3_NPLXR

DRAWING TITLE: SCH,MLB,TOP,D53

DRAWING NUMBER: 051-05215 SIZE: D
REVISION: 4.6.0
BRANCH:
PAGE: 179 OF 191
SHEET:

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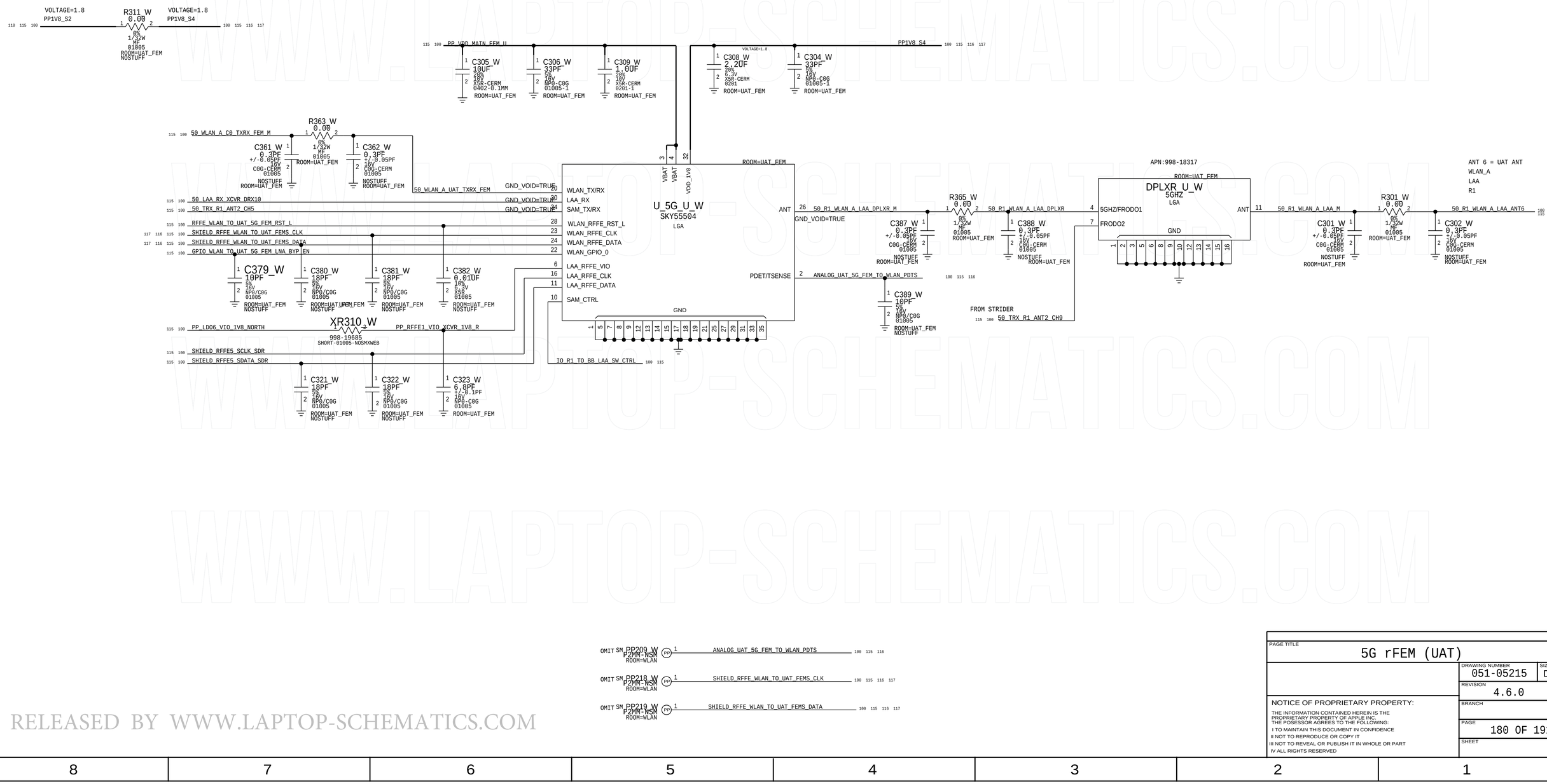
UAT 5GHZ RFEM



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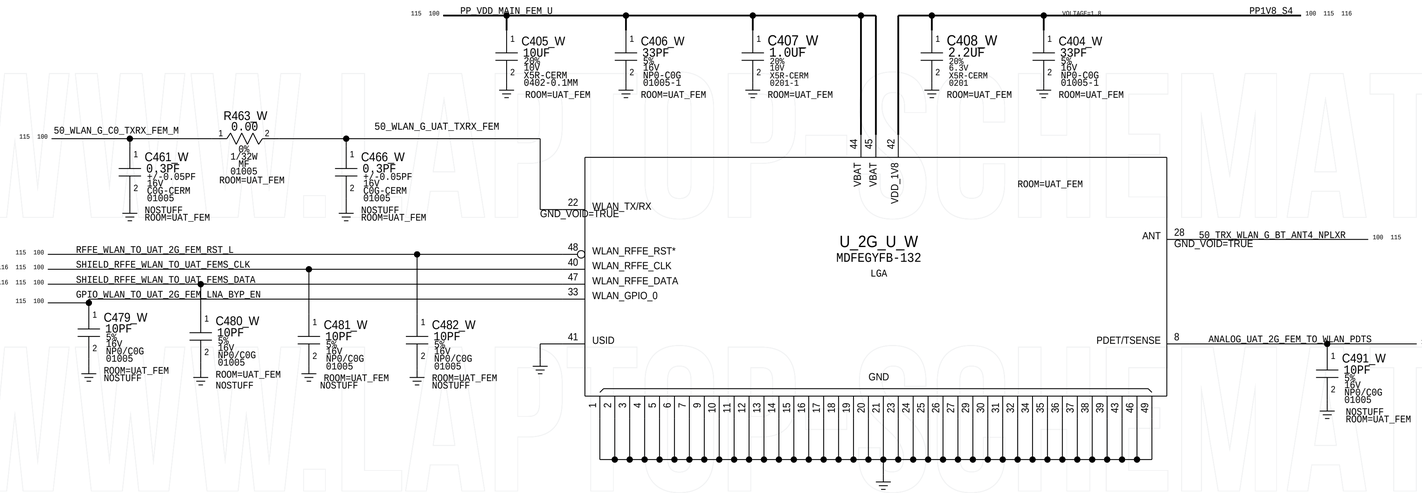
UAT 2.4 GHZ RFEM



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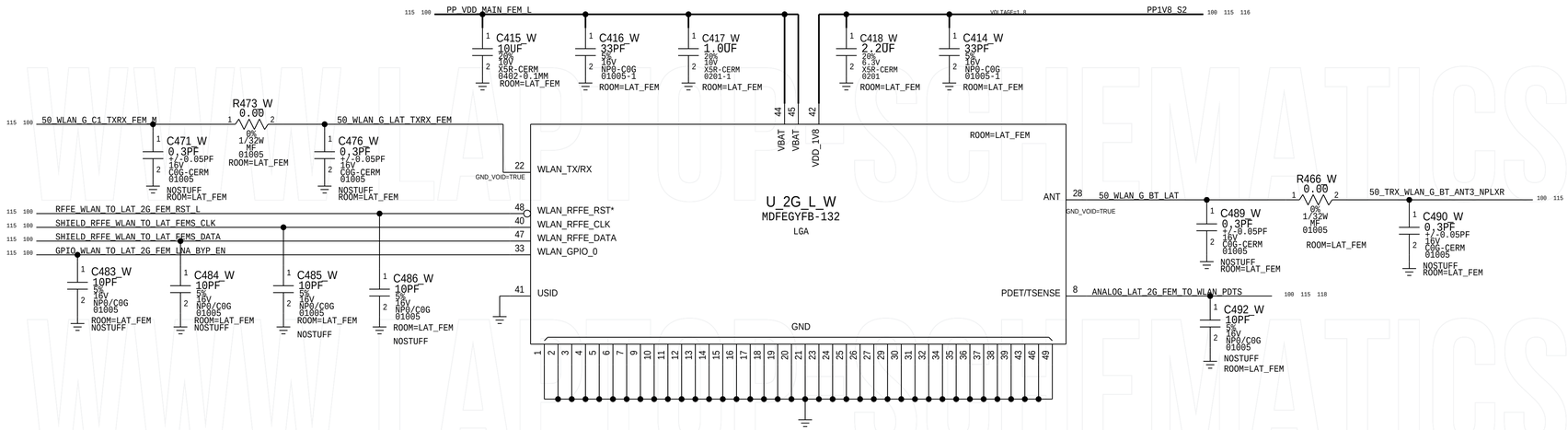
LAT 2.4 GHZ RFEM



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2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0022702675	ENGINEERING RELEASED	2020-03-26

D53 INTERPOSER

EVT

LAST_MODIFICATION=Fri Mar 13 16:11:10 2020

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	Table of Contents		
2	2	Top Side: Symbol (1/2)		08/08/2019
3	3	Top Side: Symbol (2/2)		08/08/2019
4	4	Bottom Side: Symbol (1/2)		08/08/2019
5	5	Bottom Side: Symbol (2/2)		08/08/2019
6	6	INTERPOSER: Aliases (1/4)		08/08/2019
7	7	INTERPOSER: Aliases (2/4)		08/08/2019
8	8	INTERPOSER: Aliases (3/4)		08/08/2019
9	9	INTERPOSER: Aliases (4/4)		08/08/2019

APNs

BOM: 639-08623

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05226	1	SCH,MLB,INT,D53	SCH	CRITICAL	?
820-01957	1	PCBA,MLB,INT,D53	PCB	CRITICAL	?

EEEE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR PCBA,MLB,INT,D53	MT1D	CRITICAL	?

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TOP SIDE SYMBOL (1/2)

J INT TOP
INTERPOSER-TOP-D53
SM
SYM 1 OF 4

998-20170

6 4	GND_OUTER_NORTHEAST_PENINSULA	1	IO1	IO91	91	GND_OUTER_ARMPIT 4 6
6 4	GND_INNER_NORTHEAST	2	IO2	IO92	92	PP_VDD_MAIN_2 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	3	IO3	IO93	93	GND_OUTER_ARMPIT 4 6
6 4	GND_INNER_NORTHEAST	4	IO4	IO94	94	PP_VDD_MAIN_3 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	5	IO5	IO95	95	GND_OUTER_ARMPIT 4 6
6 4	GND_INNER_NORTHEAST	6	IO6	IO96	96	PP_VDD_MAIN_4 4 6
6 4	GPIO_AP_CANARY6_PIN_7	7	IO7	IO97	97	GND_OUTER_ARMPIT 4 6
6 4	GND_INNER_NORTHEAST	8	IO8	IO98	98	GPIO_AP_CANARY3 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	9	IO9	IO99	99	GND_OUTER_ARMPIT 4 6
6 4	GPIO_AP_CANARY6_PIN_10	10	IO10	IO100	100	GND_INNER_ARMPIT 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	11	IO11	IO101	101	GND_OUTER_TAB_2 4 6
6 4	GND_INNER_NORTHEAST	12	IO12	IO102	102	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	13	IO13	IO103	103	GND_OUTER_TAB_2 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	14	IO14	IO104	104	PP_VDD_BOOST_NORTH_PA 4 6
6 4	GPIO_AP_CANARY6_PIN_15	15	IO15	IO105	105	GND_OUTER_TAB_2 4 6
6 4	GPIO_AP_CANARY6	16	IO16	IO106	106	PP1V2_S4 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	17	IO17	IO107	107	GND_OUTER_TAB_2 4 6
6 4	PP1V8_S2_1	18	IO18	IO108	108	GPIO_AOP_TO_WLAN_CONTEXT_A 4 6
6 4	GND_OUTER_NORTHEAST_PENINSULA	19	IO19	IO109	109	GND_OUTER_TAB_2 4 6
6 4	GND_INNER_NORTHEAST	20	IO20	IO110	110	PP1V8_S4 4 6
6 4	GND_OUTER_TAB_1	21	IO21	IO111	111	GND_OUTER_TAB_2 4 6
6 4	GND_INNER_NORTHEAST	22	IO22	IO112	112	RFFE_WLAN_TO_UAT_2G_FEM_RST_L 4 6
6 4	GND_OUTER_TAB_1	23	IO23	IO113	113	GND_OUTER_TAB_2 4 6
6 4	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	24	IO24	IO114	114	RFFE_WLAN_TO_UAT_5G_FEM_RST_L 4 6
6 4	GND_OUTER_TAB_1	25	IO25	IO115	115	GND_OUTER_TAB_2 4 6
6 4	GND_INNER_NORTHEAST	26	IO26	IO116	116	GPIO_SE_TO_BT_PKT_RDY 4 6
6 4	GND_OUTER_TAB_1	27	IO27	IO117	117	GND_OUTER_EAST 4 6
6 4	IO_R1_TO_BB_LAA_SW_CTRL	28	IO28	IO118	118	GND_INNER_ARMPIT 4 6
6 4	GND_OUTER_TAB_1	29	IO29	IO119	119	GND_OUTER_EAST 4 6
6 4	IO_BT_TO_R1_WAKE	30	IO30	IO120	120	I2C_BT_TO_NFC_SCL 4 6
6 4	GND_OUTER_TAB_1	31	IO31	IO121	121	GND_OUTER_EAST 4 6
6 4	GND_INNER_NORTHEAST	32	IO32	IO122	122	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS 4 6
6 4	GND_OUTER_TAB_1	33	IO33	IO123	123	GND_OUTER_EAST 4 6
6 4	PPVAR_RCAM_PVDD	34	IO34	IO124	124	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8 4 6
6 4	GND_OUTER_TAB_1	35	IO35	IO125	125	GND_OUTER_EAST 4 6
6 4	GND_INNER_NORTHEAST	36	IO36	IO126	126	GND_INNER_ARMPIT 4 6
6 4	GND_OUTER_ARMPIT	37	IO37	IO127	127	GND_OUTER_EAST 4 6
6 4	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	38	IO38	IO128	128	I2C_BT_TO_NFC_SDA 4 6
6 4	GND_OUTER_ARMPIT	39	IO39	IO129	129	GND_OUTER_EAST 4 6
6 4	GPIO_BB_TO_R1_CH9_REQ	40	IO40	IO130	130	GPIO_AP_FROM_WLAN_TIME_SYNC 4 6
6 4	GND_OUTER_ARMPIT	41	IO41	IO131	131	GND_OUTER_EAST 4 6
6 4	NTC_STROBE_MODULE	42	IO42	IO132	132	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN 4 6
6 4	GND_OUTER_ARMPIT	43	IO43	IO133	133	GND_OUTER_EAST 4 6
6 4	GND_OUTER_ARMPIT	44	IO44	IO134	134	GND_OUTER_EAST 4 6
6 4	GPIO_AP_CANARY5	45	IO45	IO135	135	GND_OUTER_EAST 4 6
6 4	GND_OUTER_ARMPIT	46	IO46	IO136	136	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN 4 6
6 4	GPIO_AP_CANARY5_PIN_47	47	IO47	IO137	137	GND_OUTER_EAST 4 6
6 4	GND_OUTER_ARMPIT	48	IO48	IO138	138	GPIO_AP_TO_BB_PEAK_PWR_IND 4 6
6 4	GND_OUTER_ARMPIT	49	IO49	IO139	139	GND_OUTER_EAST 4 6
6 4	GND_OUTER_ARMPIT	50	IO50	IO140	140	SWD_AP_BI_BB_SWDIO 4 6
6 4	GPIO_AP_CANARY5_PIN_51	51	IO51	IO141	141	GND_OUTER_EAST 4 6
6 4	GND_OUTER_ARMPIT	52	IO52	IO142	142	GND_INNER_EAST 4 6
6 4	GND_OUTER_ARMPIT	53	IO53	IO143	143	GND_OUTER_EAST 4 6
6 4	GPIO_AP_CANARY5_PIN_54	54	IO54	IO144	144	GPIO_AP_FROM_BB_RESET_DETECT_L 4 6
6 4	GND_OUTER_ARMPIT	55	IO55	IO145	145	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	56	IO56	IO146	146	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA 4 6
6 4	GND_OUTER_ARMPIT	57	IO57	IO147	147	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	58	IO58	IO148	148	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK 4 6
6 4	GND_OUTER_ARMPIT	59	IO59	IO149	149	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	60	IO60	IO150	150	GND_INNER_EAST 4 6
				IO151	151	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	62	IO62	IO152	152	GPIO_AP_FROM_BT_AUDIO_SYNC 4 6
6 4	GPIO_AP_CANARY5_PIN_63	63	IO63	IO153	153	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	64	IO64	IO154	154	GPIO_AP_TO_BB_TIME_MARK 4 6
6 4	GND_INNER_ARMPIT	65	IO65	IO155	155	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	66	IO66	IO156	156	NTC_RADIO_BB_P 4 6
6 4	GPIO_AP_CANARY5_PIN_67	67	IO67	IO157	157	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	68	IO68	IO158	158	GND_INNER_EAST 4 6
6 4	GPIO_AP_CANARY5_PIN_69	69	IO69	IO159	159	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	70	IO70	IO160	160	UART1_AOP_FROM_BB_RXD 4 6
6 4	GND_INNER_ARMPIT	71	IO71	IO161	161	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	72	IO72	IO162	162	UART1_AOP_TO_BB_TXD 4 6
6 4	GND_OUTER_ARMPIT	73	IO73	IO163	163	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	74	IO74	IO164	164	GPIO_AOP_TO_BB_FORCE_PWM 4 6
6 4	GND_OUTER_ARMPIT	75	IO75	IO165	165	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	76	IO76	IO166	166	GND_INNER_EAST 4 6
6 4	GND_OUTER_ARMPIT	77	IO77	IO167	167	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	78	IO78	IO168	168	PP_VDD_RF_1V2 4 6
6 4	GND_OUTER_ARMPIT	79	IO79	IO169	169	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	80	IO80	IO170	170	GND_INNER_EAST 4 6
6 4	GND_OUTER_ARMPIT	81	IO81	IO171	171	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	82	IO82	IO172	172	GPIO_AOP_TO_WLAN_CONTEXT_B 4 6
6 4	GND_OUTER_ARMPIT	83	IO83	IO173	173	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	84	IO84	IO174	174	GND_INNER_EAST 4 6
6 4	GND_OUTER_ARMPIT	85	IO85	IO175	175	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	86	IO86	IO176	176	PP_VDD_BOOST_BBPMU 4 6
6 4	GPIO_AP_CANARY5_PIN_87	87	IO87	IO177	177	GND_OUTER_EAST 4 6
6 4	GND_INNER_ARMPIT	88	IO88	IO178	178	GND_INNER_EAST 4 6
6 4	GND_OUTER_ARMPIT	89	IO89	IO179	179	GND_OUTER_EAST 4 6
6 4	PP_VDD_MAIN_1	90	IO90	IO180	180	PP_VDD_MAIN_5 4 6

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7 4	GND_OUTER_EAST	181	IO181	IO271	271	50_TRX_LB_PAD_ANT1 4 7
7 4	PP_VDD_MAIN_6	182	IO182	IO272	272	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	183	IO183	IO273	273	GND_PA_CAVITY 4 7
7 4	PP_VDD_MAIN_7	184	IO184	IO274	274	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	185	IO185	IO275	275	GND_OUTER_SOUTH 4 7
7 4	PP_VDD_MAIN_8	186	IO186	IO276	276	50_TRX_IN_LMB_PAD_2G_MB_OUT_M 4 7
7 4	GND_OUTER_EAST	187	IO187	IO277	277	GND_PA_CAVITY 4 7
7 4	GND_INNER_EAST	188	IO188	IO278	278	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	189	IO189	IO279	279	GND_PA_CAVITY 4 7
7 4	PP3V0_S2	190	IO190	IO280	280	50_TRX_IN_LMB_PAD_LMB_ANT_M 4 7
7 4	GND_OUTER_EAST	191	IO191	IO281	281	GND_OUTER_SOUTH 4 7
7 4	GND_INNER_EAST	192	IO192	IO282	282	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	193	IO193	IO283	283	GND_PA_CAVITY 4 7
7 4	GND_INNER_EAST	194	IO194	IO284	284	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	195	IO195	IO285	285	50_TRX_WLAN_G_BT_ANT3_NPLXR 4 7
7 4	GND_INNER_EAST	196	IO196	IO286	286	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	197	IO197	IO287	287	GND_OUTER_SOUTH 4 7
7 4	GND_INNER_EAST	198	IO198	IO288	288	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	199	IO199			
7 4	GPIO_BT_TO_BOT_SPKR_TRIG	200	IO200	IO290	290	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	201	IO201	IO291	291	50_TX_IN_XCVR_TX0_MB2G 4 7
7 4	GND_INNER_EAST	202	IO202	IO292	292	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	203	IO203	IO293	293	GND_OUTER_SOUTH 4 7
7 4	GND_INNER_EAST	204	IO204	IO294	294	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	205	IO205			
7 4	GND_INNER_EAST	206	IO206	IO296	296	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	207	IO207	IO297	297	50_TRX_ANT7_UHB_N79 4 7
7 4	GND_INNER_EAST	208	IO208	IO298	298	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	209	IO209	IO299	299	GND_OUTER_SOUTH 4 7
7 4	RFFE_WLAN_TO_LAT_2G_FEM_RST_L	210	IO210	IO300	300	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	211	IO211	IO301	301	50_TX_IN_XCVR_TX0_LMB 4 7
7 4	GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	212	IO212	IO302	302	GPIO_AOP_CANARY7_PIN_302 4 7
7 4	GND_OUTER_EAST	213	IO213	IO303	303	GND_PA_CAVITY 4 7
7 4	ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	214	IO214	IO304	304	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	215	IO215	IO305	305	GND_OUTER_SOUTH 4 7
7 4	PP_LDO6_VIO_1V8_SOUTH	216	IO216	IO306	306	PP_VDD_MAIN_9 4 7
7 4	GND_OUTER_EAST	217	IO217	IO307	307	PP_VDD_MAIN_10 4 7
7 4	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	218	IO218	IO308	308	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	219	IO219	IO309	309	GND_OUTER_SOUTH 4 7
7 4	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	220	IO220	IO310	310	GPIO_AOP_CANARY7_PIN_310 4 7
7 4	GND_OUTER_EAST	221	IO221	IO311	311	GND_SOUTHWEST 4 7
7 4	PP1V8_S2_2	222	IO222	IO312	312	GND_OUTER_SOUTH 4 7
7 4	GND_OUTER_EAST	223	IO223	IO313	313	
7 4	GND_OUTER_EAST	224	IO224	IO314	314	GND_SOUTHWEST 4 7
7 4	GND_OUTER_EAST	225	IO225	IO315	315	GND_SOUTHWEST 4 7
7 4	50_RX_LMB_PAD_LMB_PRX_OUT_M	226	IO226	IO316	316	GND_PA_CAVITY 4 7
7 4	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	227	IO227	IO317	317	GND_SOUTHWEST 4 7
7 4	GND_PA_CAVITY	228	IO228	IO318	318	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	229	IO229	IO319	319	GND_SOUTHWEST 4 7
7 4	GND_PA_CAVITY	230	IO230	IO320	320	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	231	IO231	IO321	321	GPIO_AOP_CANARY7_PIN_321 4 7
7 4	50_TX_IN_XCVR_TX0_LB	232	IO232	IO322	322	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	233	IO233	IO323	323	GND_SOUTHWEST 4 7
7 4	GND_PA_CAVITY	234	IO234	IO324	324	GND_SOUTHWEST 4 7
7 4	GND_OUTER_EAST	235	IO235	IO325	325	GND_SOUTHWEST 4 7
7 4	50_UHB_L_CPLR_OUT	236	IO236	IO326	326	GPIO_AOP_CANARY7_PIN_326 4 7
7 4	50_RX_XCVR_PRX6_LB_A_RX0	237	IO237	IO327	327	GND_SOUTHWEST 4 7
7 4	GND_PA_CAVITY	238	IO238	IO328	328	GPIO_AOP_CANARY7 4 7
7 4	GND_OUTER_EAST	239	IO239	IO329	329	GND_OUTER_WEST 4 7
7 4	GND_PA_CAVITY	240	IO240	IO330	330	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	241	IO241	IO331	331	GND_OUTER_WEST 4 7
7 4	PP_QET0_2G_PA_1	242	IO242	IO332	332	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	243	IO243	IO333	333	GND_OUTER_WEST 4 7
7 4	PP_QET0_2G_PA_2	244	IO244	IO334	334	GND_PA_CAVITY 4 7
7 4	GND_OUTER_EAST	245	IO245	IO335	335	GND_OUTER_WEST 4 7
7 4	PP_QET0_PA_1	246	IO246	IO336	336	50_TRX_PAUHBL_N79_ANT2_TO_ANT9 4 7
7 4	GND_OUTER_TAB_3	247	IO247	IO337	337	GND_OUTER_WEST 4 7
7 4	PP_QET0_PA_2	248	IO248	IO338	338	GND_PA_CAVITY 4 7
7 4	GND_OUTER_TAB_3	249	IO249	IO339	339	50_TRX_UHB_PAD_PORTB_TX_M 4 7
7 4	GND_PA_CAVITY	250	IO250	IO340	340	GND_PA_CAVITY 4 7
7 4	GND_OUTER_TAB_3	251	IO251	IO341	341	GND_OUTER_WEST 4 7
7 4	50_WLAN_G_C1_TXRX_FEM_M	252	IO252	IO342	342	50_TRX_UHB_PAD_N79_PORTB_TX_M 4 7
7 4	GND_OUTER_TAB_3	253	IO253	IO343	343	GND_OUTER_WEST 4 7
7 4	GND_PA_CAVITY	254	IO254	IO344	344	GND_PA_CAVITY 4 7
7 4	GND_OUTER_TAB_3	255	IO255	IO345	345	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9 4 7
7 4	SHIELD_RFFE1_SCLK_SDR	256	IO256	IO346	346	GND_PA_CAVITY 4 7
7 4	GND_OUTER_TAB_3	257	IO257	IO347	347	GND_OUTER_WEST 4 7
7 4	GND_OUTER_TAB_3	258	IO258	IO348	348	50_TRX_LB_PORTB_RX1_M 4 7
7 4	GND_OUTER_SOUTH	259	IO259	IO349	349	GND_OUTER_WEST 4 7
7 4	SHIELD_RFFE1_SDATA_SDR	260	IO260	IO350	350	GND_SOUTHWEST 4 7
7 4	GND_OUTER_SOUTH	261	IO261			
7 4	GND_PA_CAVITY	262	IO262	IO352	352	GND_PA_CAVITY 4 7
7 4	GPIO_AOP_CANARY7_PIN_263	263	IO263			
7 4	GND_PA_CAVITY	264	IO264	IO354	354	GND_INNER_WEST 4 7
7 4	GPIO_AOP_CANARY7_PIN_265	265	IO265	IO355	355	50_TX_IN_XCVR_TX0_LB2G 4 7
7 4	GND_PA_CAVITY	266	IO266	IO356	356	GND_INNER_WEST 4 7
7 4	GPIO_AOP_CANARY7_PIN_267	267	IO267	IO357	357	50_RX_XCVR_PRX10_LB_PRX_OUT2 4 7
7 4	GND_PA_CAVITY	268	IO268	IO358	358	50_TRX_LB_PORTB_TX_M 4 7
7 4	GND_OUTER_SOUTH	269	IO269	IO359	359	GND_PA_CAVITY 4 7
7 4	GND_PA_CAVITY	270	IO270	IO360	360	GND_INNER_WEST 4 7

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GND_PA_CAVITY	361	IO361	IO451	451	GND_OUTER_WEST	
PP_APT_L_PA_1	362	IO362	IO452	452	GND_INNER_WEST	
PP_APT_L_PA_2	363	IO363	IO453	453	GND_OUTER_WEST	
GND_INNER_WEST	364	IO364	IO454	454	GPIO_NUB_TO_BBPMU_CLK_EN_DQTARA	
GND_PA_CAVITY	365	IO365	IO455	455	GND_OUTER_WEST	
PP_QET1_PA_1	366	IO366	IO456	456	I2S2_AP_FROM_BB_BCLK	
PP_QET1_PA_2	367	IO367	IO457	457	GND_OUTER_WEST	
GND_INNER_WEST	368	IO368	IO458	458	I2S2_AP_FROM_BB_LRCLK	
GND_PA_CAVITY	369	IO369	IO459	459	GND_OUTER_WEST	
GND_INNER_WEST	370	IO370	IO460	460	GND_INNER_WEST	
50_RX_XCVR_PRX15_N79_RX_OUT2	371	IO371	IO461	461	GND_OUTER_WEST	
GND_INNER_WEST	372	IO372	IO462	462	I2S2_AP_FROM_BB_DIN	
GND_PA_CAVITY	373	IO373	IO463	463	GND_OUTER_WEST	
GND_INNER_WEST	374	IO374	IO464	464	I2S2_AP_TO_BB_DOUT	
50_RX_XCVR_PRX17_UHB_RX_OUT2	375	IO375	IO465	465	GND_OUTER_WEST	
50_RX_XCVR_PRX14_N79_RX_OUT1	376	IO376	IO466	466	GND_INNER_WEST	
GND_PA_CAVITY	377	IO377	IO467	467	GND_OUTER_WEST	
GND_INNER_WEST	378	IO378				
GND_PA_CAVITY	379	IO379	IO469	469	GND_OUTER_WEST	
GND_INNER_WEST	380	IO380	IO470	470	GND_INNER_WEST	
50_RX_XCVR_PRX16_UHB_RX_OUT1	381	IO381	IO471	471	GND_OUTER_WEST	
SHIELD_RFFE2_SDATA_SDR	382	IO382	IO472	472	GND_INNER_WEST	
GND_PA_CAVITY	383	IO383	IO473	473	GND_OUTER_WEST	
SHIELD_RFFE2_SCLK_SDR	384	IO384	IO474	474	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	
SHIELD_RFFE8_SDATA_SDR	385	IO385	IO475	475	GND_OUTER_WEST	
SHIELD_RFFE8_SCLK_SDR	386	IO386	IO476	476	GPIO_S4_PMU_TO_WLAN_REG_ON	
PP_VDD_BOOST_SOUTH_PA	387	IO387	IO477	477	GND_OUTER_WEST	
GND_INNER_EAST	388	IO388	IO478	478	GPIO_PMU_FROM_WLAN_HOST_WAKE	
GND_PA_CAVITY	389	IO389	IO479	479	GND_OUTER_WEST	
GND_INNER_EAST	390	IO390	IO480	480	GND_INNER_WEST	
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	391	IO391	IO481	481	GND_OUTER_WEST	
GND_INNER_EAST	392	IO392	IO482	482	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	
GND_PA_CAVITY	393	IO393	IO483	483	GND_OUTER_WEST	
GND_INNER_EAST	394	IO394	IO484	484	PCIE_GP1_AP_TO_WLAN_PERST_L	
50_TX_IN_XCVR_TX1_LB_JB	395	IO395	IO485	485	GND_OUTER_WEST	
SHIELD_RFFE3_SDATA_SDR	396	IO396	IO486	486	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	
GND_PA_CAVITY	397	IO397	IO487	487	GND_OUTER_WEST	
SHIELD_RFFE3_SCLK_SDR	398	IO398	IO488	488	GND_OUTER_WEST	
GND_PA_CAVITY	399	IO399	IO489	489	GND_OUTER_WEST	
GND_INNER_WEST	400	IO400	IO490	490	PCIE_GP2_AP_TO_BB_PERST_L	
GND_OUTER_WEST	401	IO401	IO491	491	GND_OUTER_WEST	
PP_VDD_MAIN_11	402	IO402	IO492	492	PCIE_GP2_AP_BI_BB_CLKREQ_L	
GND_OUTER_WEST	403	IO403	IO493	493	GND_OUTER_WEST	
PP_VDD_MAIN_12	404	IO404	IO494	494	SWD_AP_TO_MANY_SWCLK	
GND_OUTER_WEST	405	IO405	IO495	495	GND_OUTER_WEST	
PP_VDD_MAIN_13	406	IO406	IO496	496	GPIO_AP_TO_BB_COREDUMP	
GND_OUTER_WEST	407	IO407	IO497	497	GND_OUTER_WEST	
PP_VDD_MAIN_14	408	IO408				
GND_OUTER_WEST	409	IO409	IO499	499	GND_OUTER_WEST	
GND_INNER_WEST	410	IO410	IO500	500	GPIO_AP_CANARY4	
GND_OUTER_WEST	411	IO411	IO501	501	GND_OUTER_TAB_5	
GND_INNER_WEST	412	IO412	IO502	502	GND_INNER_NORTHWEST	
GND_OUTER_WEST	413	IO413	IO503	503	GND_OUTER_TAB_5	
PP1V2_S2_1	414	IO414	IO504	504	CLK_BBPMU_TO_NFC_38M4	
GND_OUTER_WEST	415	IO415	IO505	505	GND_OUTER_TAB_5	
GND_INNER_WEST	416	IO416	IO506	506	GND_INNER_NORTHWEST	
GND_OUTER_WEST	417	IO417	IO507	507	GND_OUTER_TAB_5	
GND_INNER_WEST	418	IO418	IO508	508	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	
GND_OUTER_WEST	419	IO419	IO509	509	GND_OUTER_TAB_5	
GPIO_SCM_AOP_FROM_JARVIS_INT	420	IO420	IO510	510	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	
GND_OUTER_WEST	421	IO421	IO511	511	GND_OUTER_TAB_5	
I2C1_AOP_SCL	422	IO422	IO512	512	GND_INNER_NORTHWEST	
GND_OUTER_WEST	423	IO423	IO513	513	GND_OUTER_TAB_5	
I2C1_AOP_SDA	424	IO424	IO514	514	90_PCIE_GP1_AP_FROM_WLAN_RX_N	
GND_OUTER_WEST	425	IO425	IO515	515	GND_OUTER_TAB_5	
GND_INNER_WEST	426	IO426	IO516	516	90_PCIE_GP1_AP_FROM_WLAN_RX_P	
GND_OUTER_WEST	427	IO427	IO517	517	GND_OUTER_NORTHWEST	
90_PCIE_GP2_AP_TO_BB_TX_N	428	IO428	IO518	518	GND_INNER_NORTHWEST	
GND_OUTER_WEST	429	IO429	IO519	519	GND_OUTER_NORTHWEST	
90_PCIE_GP2_AP_TO_BB_TX_P	430	IO430	IO520	520	90_PCIE_GP1_AP_TO_WLAN_TX_P	
GND_OUTER_WEST	431	IO431	IO521	521	GND_OUTER_NORTHWEST	
GND_INNER_WEST	432	IO432	IO522	522	90_PCIE_GP1_AP_TO_WLAN_TX_N	
GND_OUTER_WEST	433	IO433	IO523	523	GND_OUTER_NORTHWEST	
90_PCIE_GP2_AP_FROM_BB_RX_P	434	IO434	IO524	524	GND_INNER_NORTHWEST	
GND_OUTER_WEST	435	IO435	IO525	525	GND_OUTER_NORTHWEST	
90_PCIE_GP2_AP_FROM_BB_RX_N	436	IO436	IO526	526	CLK_BBPMU_TO_DOTARA_38M4	
GND_OUTER_WEST	437	IO437	IO527	527	GND_OUTER_NORTHWEST	
GND_INNER_WEST	438	IO438	IO528	528	GND_INNER_NORTHWEST	
GND_OUTER_WEST	439	IO439	IO529	529	GND_OUTER_NORTHWEST	
90_PCIE_GP2_AP_TO_BB_REFCLK_N	440	IO440	IO530	530	GPIO_SP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	
GND_OUTER_WEST	441	IO441	IO531	531	GND_OUTER_NORTHWEST	
90_PCIE_GP2_AP_TO_BB_REFCLK_P	442	IO442	IO532	532	GND_INNER_NORTHWEST	
GND_OUTER_WEST	443	IO443	IO533	533	GND_OUTER_NORTHWEST	
GND_INNER_WEST	444	IO444	IO534	534	GPIO_AP_CANARY2	
GND_OUTER_WEST	445	IO445	IO535	535	GND_OUTER_NORTHWEST	
PP_VDD_MAIN_15	446	IO446				
GND_OUTER_WEST	447	IO447	IO537	537	GND_OUTER_NORTHWEST	
PP_VDD_MAIN_16	448	IO448	IO538	538	GND_INNER_NORTHWEST	
GND_OUTER_WEST	449	IO449	IO539	539	GND_OUTER_NORTHWEST	
PP_VDD_MAIN_17	450	IO450	IO540	540	GND_INNER_NORTHWEST	

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GND_OUTER_NORTHWEST	541	IO541	IO631	631	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	542	IO542	IO632	632	SHIELD_RFFE5_SDATA_SDR	
50_WLAN_A_C0_TXRX_FEM_M	543	IO543	IO633	633	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	544	IO544	IO634	634	GND_INNER_NORTHEAST	
GND_OUTER_NORTHWEST	545	IO545	IO635	635	GND_OUTER_NORTH	
50_WLAN_G_C0_TXRX_FEM_M	546	IO546	IO636	636	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	
GND_OUTER_NORTHWEST	547	IO547	IO637	637	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	548	IO548	IO638	638	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	
50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	549	IO549	IO639	639	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	550	IO550	IO640	640	GND_INNER_NORTHEAST	
GND_OUTER_NORTHWEST	551	IO551	IO641	641	GND_OUTER_NORTH	
50_TRX_PAUHBU_N79_ANT1_TO_ANT4	552	IO552	IO642	642	UAT_SUBUS_B	
GND_OUTER_NORTHWEST	553	IO553	IO643	643	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	554	IO554	IO644	644	UAT_SUBUS_A	
GND_OUTER_NORTHWEST	555	IO555	IO645	645	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	556	IO556	IO646	646	GND_INNER_NORTHEAST	
GND_OUTER_NORTHWEST	557	IO557	IO647	647	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	558	IO558	IO648	648	NTC_RADIO_PA_P	
GND_OUTER_NORTHWEST	559	IO559	IO649	649	GND_OUTER_NORTH	
IO_NFC_TO_BBPMU_CLKREQ	560	IO560	IO650	650	UAT_TUNER_TO_R1_STATE	
GND_OUTER_NORTHWEST	561	IO561	IO651	651	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	562	IO562	IO652	652	GPIO_R1_TO_BB_CH9_COEX	
GND_OUTER_NORTHWEST	563	IO563	IO653	653	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	564	IO564	IO654	654	GND_INNER_NORTHEAST	
GND_OUTER_TAB_6	565	IO565	IO655	655	GND_OUTER_NORTH	
GND_OUTER_TAB_6	566	IO566	IO656	656	GPIO_R1_TO_WLAN_COEX	
GND_OUTER_TAB_6	567	IO567	IO657	657	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	568	IO568	IO658	658	PP1V2_S2_2	
GND_OUTER_TAB_6	569	IO569	IO659	659	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	570	IO570	IO660	660	GND_INNER_NORTHEAST	
GND_OUTER_TAB_6	571	IO571	IO661	661	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	572	IO572	IO662	662	GPIO_CAM_PMU1_TO_PVDD_RESET_L	
GND_OUTER_TAB_6	573	IO573	IO663	663	GND_OUTER_NORTH	
ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	574	IO574	IO664	664	I2C4_CAM_PMU1_SCL_1V8	
GND_OUTER_TAB_6	575	IO575	IO665	665	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	576	IO576	IO666	666	GND_INNER_NORTHEAST	
GND_OUTER_TAB_6	577	IO577	IO667	667	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	578	IO578	IO668	668	I2C4_CAM_PMU1_SDA_1V8	
GND_OUTER_NORTH	579	IO579	IO669	669	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	580	IO580	IO670	670	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	581	IO581	IO671	671	GND_OUTER_NORTH	
50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	582	IO582	IO672	672	GND_OUTER_NORTH	
GND_OUTER_NORTH	583	IO583	IO673	673	GND_OUTER_NORTH	
50_TRX_ANT8_UHB_N79	584	IO584	IO674	674	GND_OUTER_NORTH	
GND_OUTER_NORTH	585	IO585	IO675	675	GPIO_SCM_AOP_FROM_IMU_DATARDY	
GND_OUTER_NORTH	586	IO586	IO676	676	GPIO_AP_CANARY1_PIN_676	
GND_OUTER_NORTH	587	IO587	IO677	677	GPIO_AP_CANARY1_PIN_677	
GND_INNER_NORTHWEST	588	IO588	IO678	678	SPI0_AOP_FROM_IMU_R1_MISO	
GND_OUTER_NORTH	589	IO589	IO679	679	PP_STROBE_DRIVER_COOL_LED_1	
GND_INNER_NORTHWEST	590	IO590	IO680	680	GND_OUTER_NORTH	
GPIO_AP_CANARY1_PIN_591	591	IO591	IO681	681	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	
GND_INNER_NORTHWEST	592	IO592	IO682	682	PP_STROBE_DRIVER_COOL_LED_2	
GND_NORTHWEST	593	IO593	IO683	683	GPIO_AP_CANARY1_PIN_683	
GPIO_AP_CANARY1_PIN_594	594	IO594	IO684	684	GND_OUTER_NORTH	
GND_NORTHWEST	595	IO595	IO685	685	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	596	IO596	IO686	686	GND_OUTER_NORTH	
NC	597	IO597	IO687	687	SPI0_AOP_TO_IMU_R1_MOSI	
GND_NORTHWEST	598	IO598	IO688	688	PP_STROBE_DRIVER_WARM_LED_1	
GND_OUTER_NORTH	599	IO599	IO689	689	GPIO_AP_CANARY1_PIN_689	
GND_INNER_NORTHWEST	600	IO600	IO690	690	SPI0_AOP_TO_IMU_R1_SCLK	
GND_NORTHWEST	601	IO601	IO691	691	PP_STROBE_DRIVER_WARM_LED_2	
GND_INNER_NORTHWEST	602	IO602	IO692	692	GND_OUTER_NORTH	
GND_NORTHWEST	603	IO603	IO693	693	GND_OUTER_NORTH	
GND_NORTHWEST	604	IO604	IO694	694	GND_INNER_NORTHEAST	
GPIO_AP_CANARY1_PIN_605	605	IO605	IO695	695	GPIO_AP_CANARY1_PIN_695	
GND_INNER_NORTHWEST	606	IO606	IO696	696	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	607	IO607	IO697	697	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	608	IO608	IO698	698	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	609	IO609	IO699	699	GND_OUTER_NORTH	
GND_INNER_NORTHWEST	610	IO610	IO700	700	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	611	IO611	IO701	701	GND_OUTER_NORTH	
GND_OUTER_NORTH	612	IO612	IO702	702	GND_INNER_NORTHEAST	
GPIO_AP_CANARY1_PIN_613	613	IO613	IO703	703	GND_OUTER_NORTH	
PP_LDO6_VIO_1V8_NORTH	614	IO614	IO704	704	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	615	IO615	IO705	705	GND_OUTER_NORTH	
GPIO_BB_TO_R1_COEX	616	IO616	IO706	706	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	617	IO617	IO707	707	GND_OUTER_NORTH	
IO_BT_TO_R1_TIME_SYNC	618	IO618	IO708	708	GPIO_AP_CANARY6_PIN_708	
GND_OUTER_NORTH	619	IO619	IO709	709	GND_OUTER_NORTH	
GPIO_WLAN_TO_R1_COEX	620	IO620	IO710	710	NC	
GND_OUTER_NORTH	621	IO621	IO711	711	GND_NORTHEAST	
GND_INNER_NORTHEAST	622	IO622	IO712	712	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	623	IO623	IO713	713	GPIO_AP_CANARY6_PIN_713	
GND_INNER_NORTHEAST	624	IO624	IO714	714	GND_INNER_NORTHEAST	
50_TRX_ANT2_LB_LMB_MB_HB_L1	625	IO625	IO715	715	GND_NORTHEAST	
GND_INNER_NORTHEAST	626	IO626	IO716	716	GND_INNER_NORTHEAST	
50_LAA_RX_XCVR_DRX10	627	IO627	IO717	717	GPIO_AP_CANARY6_PIN_717	
GND_OUTER_NORTH	628	IO628	IO718	718	GND_INNER_NORTHEAST	
GND_OUTER_NORTH	629	IO629	IO719	719	GND_NORTHEAST	
SHIELD_RFFE5_SCLK_SDR	630	IO630	IO720	720	GPIO_AP_CANARY6_PIN_720	
			IO721	721	GPIO_AP_CANARY6_PIN_721	
			IO722	722	GND_NORTHEAST	
			IO723	723	GND_NORTHEAST	
			IO724	724	GND_INNER_NORTHEAST	
			IO725	725	GND_INNER_NORTHEAST	
			IO726	726	GND_INNER_NORTHWEST	
			IO727	727	GND_INNER_NORTHWEST	

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6 2 GND_OUTER_NORTHEAST_PENINSULA	1	IO1	IO91	91	GND_OUTER_ARMPIT 2 6
6 2 GND_INNER_NORTHEAST	2	IO2	IO92	92	PP_VDD_MAIN_2 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	3	IO3	IO93	93	GND_OUTER_ARMPIT 2 6
6 2 GND_INNER_NORTHEAST	4	IO4	IO94	94	PP_VDD_MAIN_3 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	5	IO5	IO95	95	GND_OUTER_ARMPIT 2 6
6 2 GND_INNER_NORTHEAST	6	IO6	IO96	96	PP_VDD_MAIN_4 2 6
6 2 GPIO_AP_CANARY6_PIN_7	7	IO7	IO97	97	GND_OUTER_ARMPIT 2 6
6 2 GND_INNER_NORTHEAST	8	IO8	IO98	98	GPIO_AP_CANARY3 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	9	IO9	IO99	99	GND_OUTER_ARMPIT 2 6
6 2 GPIO_AP_CANARY6_PIN_10	10	IO10	IO100	100	GND_INNER_ARMPIT 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	11	IO11	IO101	101	GND_OUTER_TAB_2 2 6
6 2 GND_INNER_NORTHEAST	12	IO12	IO102	102	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	13	IO13	IO103	103	GND_OUTER_TAB_2 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	14	IO14	IO104	104	PP_VDD_BOOST_NORTH_PA 2 6
6 2 GPIO_AP_CANARY6_PIN_15	15	IO15	IO105	105	GND_OUTER_TAB_2 2 6
6 2 GPIO_AP_CANARY6	16	IO16	IO106	106	PP1V2_S4 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	17	IO17	IO107	107	GND_OUTER_TAB_2 2 6
6 2 PP1V8_S2_1	18	IO18	IO108	108	GPIO_AOP_TO_WLAN_CONTEXT_A 2 6
6 2 GND_OUTER_NORTHEAST_PENINSULA	19	IO19	IO109	109	GND_OUTER_TAB_2 2 6
6 2 GND_INNER_NORTHEAST	20	IO20	IO110	110	PP1V8_S4 2 6
6 2 GND_OUTER_TAB_1	21	IO21	IO111	111	GND_OUTER_TAB_2 2 6
6 2 GND_INNER_NORTHEAST	22	IO22	IO112	112	RFFE_WLAN_TO_UAT_2G_FEM_RST_L 2 6
6 2 GND_OUTER_TAB_1	23	IO23	IO113	113	GND_OUTER_TAB_2 2 6
6 2 GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	24	IO24	IO114	114	RFFE_WLAN_TO_UAT_5G_FEM_RST_L 2 6
6 2 GND_OUTER_TAB_1	25	IO25	IO115	115	GND_OUTER_TAB_2 2 6
6 2 GND_INNER_NORTHEAST	26	IO26	IO116	116	GPIO_SE_TO_BT_PKT_RDY 2 6
6 2 GND_OUTER_TAB_1	27	IO27	IO117	117	GND_OUTER_EAST 2 6
6 2 IO_R1_TO_BB_LAA_SW_CTRL	28	IO28	IO118	118	GND_INNER_ARMPIT 2 6
6 2 GND_OUTER_TAB_1	29	IO29	IO119	119	GND_OUTER_EAST 2 6
6 2 IO_BT_TO_R1_WAKE	30	IO30	IO120	120	I2C_BT_TO_NFC_SCL 2 6
6 2 GND_OUTER_TAB_1	31	IO31	IO121	121	GND_OUTER_EAST 2 6
6 2 GND_INNER_NORTHEAST	32	IO32	IO122	122	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS 2 6
6 2 GND_OUTER_TAB_1	33	IO33	IO123	123	GND_OUTER_EAST 2 6
6 2 PPVAR_RCAM_PVDD	34	IO34	IO124	124	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8 2 6
6 2 GND_OUTER_TAB_1	35	IO35	IO125	125	GND_OUTER_EAST 2 6
6 2 GND_INNER_NORTHEAST	36	IO36	IO126	126	GND_INNER_ARMPIT 2 6
6 2 GND_OUTER_ARMPIT	37	IO37	IO127	127	GND_OUTER_EAST 2 6
6 2 GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	38	IO38	IO128	128	I2C_BT_TO_NFC_SDA 2 6
6 2 GND_OUTER_ARMPIT	39	IO39	IO129	129	GND_OUTER_EAST 2 6
6 2 GPIO_BB_TO_R1_CH9_REQ	40	IO40	IO130	130	GPIO_AP_FROM_WLAN_TIME_SYNC 2 6
6 2 GND_OUTER_ARMPIT	41	IO41	IO131	131	GND_OUTER_EAST 2 6
6 2 NTC_STROBE_MODULE	42	IO42	IO132	132	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN 2 6
6 2 GND_OUTER_ARMPIT	43	IO43	IO133	133	GND_OUTER_EAST 2 6
6 2 GND_OUTER_ARMPIT	44	IO44	IO134	134	GND_OUTER_EAST 2 6
6 2 GPIO_AP_CANARY5	45	IO45	IO135	135	GND_OUTER_EAST 2 6
6 2 GND_OUTER_ARMPIT	46	IO46	IO136	136	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN 2 6
6 2 GPIO_AP_CANARY5_PIN_47	47	IO47	IO137	137	GND_OUTER_EAST 2 6
6 2 GND_OUTER_ARMPIT	48	IO48	IO138	138	GPIO_AP_TO_BB_PEAK_PWR_IND 2 6
6 2 GND_OUTER_ARMPIT	49	IO49	IO139	139	GND_OUTER_EAST 2 6
6 2 GND_OUTER_ARMPIT	50	IO50	IO140	140	SWD_AP_BI_BB_SWDIO 2 6
6 2 GPIO_AP_CANARY5_PIN_51	51	IO51	IO141	141	GND_OUTER_EAST 2 6
6 2 GND_OUTER_ARMPIT	52	IO52	IO142	142	GND_INNER_EAST 2 6
6 2 GND_OUTER_ARMPIT	53	IO53	IO143	143	GND_OUTER_EAST 2 6
6 2 GPIO_AP_CANARY5_PIN_54	54	IO54	IO144	144	GPIO_AP_FROM_BB_RESET_DETECT_L 2 6
6 2 GND_OUTER_ARMPIT	55	IO55	IO145	145	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	56	IO56	IO146	146	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA 2 6
6 2 GND_OUTER_ARMPIT	57	IO57	IO147	147	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	58	IO58	IO148	148	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK 2 6
6 2 GND_OUTER_ARMPIT	59	IO59	IO149	149	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	60	IO60	IO150	150	GND_INNER_EAST 2 6
			IO151	151	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	62	IO62	IO152	152	GPIO_AP_FROM_BT_AUDIO_SYNC 2 6
6 2 GPIO_AP_CANARY5_PIN_63	63	IO63	IO153	153	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	64	IO64	IO154	154	GPIO_AP_TO_BB_TIME_MARK 2 6
6 2 GND_INNER_ARMPIT	65	IO65	IO155	155	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	66	IO66	IO156	156	NTC_RADIO_BB_P 2 6
6 2 GPIO_AP_CANARY5_PIN_67	67	IO67	IO157	157	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	68	IO68	IO158	158	GND_INNER_EAST 2 6
6 2 GPIO_AP_CANARY5_PIN_69	69	IO69	IO159	159	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	70	IO70	IO160	160	UART1_AOP_FROM_BB_RXD 2 6
6 2 GND_INNER_ARMPIT	71	IO71	IO161	161	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	72	IO72	IO162	162	UART1_AOP_TO_BB_TXD 2 6
6 2 GND_OUTER_ARMPIT	73	IO73	IO163	163	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	74	IO74	IO164	164	GPIO_AOP_TO_BB_FORCE_PWM 2 6
6 2 GND_OUTER_ARMPIT	75	IO75	IO165	165	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	76	IO76	IO166	166	GND_INNER_EAST 2 6
6 2 GND_OUTER_ARMPIT	77	IO77	IO167	167	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	78	IO78	IO168	168	PP_VDD_RF_1V2 2 6
6 2 GND_OUTER_ARMPIT	79	IO79	IO169	169	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	80	IO80	IO170	170	GND_INNER_EAST 2 6
6 2 GND_OUTER_ARMPIT	81	IO81	IO171	171	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	82	IO82	IO172	172	GPIO_AOP_TO_WLAN_CONTEXT_B 2 6
6 2 GND_OUTER_ARMPIT	83	IO83	IO173	173	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	84	IO84	IO174	174	GND_INNER_EAST 2 6
6 2 GND_OUTER_ARMPIT	85	IO85	IO175	175	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	86	IO86	IO176	176	PP_VDD_BOOST_BBPMU 2 6
6 2 GPIO_AP_CANARY5_PIN_87	87	IO87	IO177	177	GND_OUTER_EAST 2 6
6 2 GND_INNER_ARMPIT	88	IO88	IO178	178	GND_INNER_EAST 2 6
6 2 GND_OUTER_ARMPIT	89	IO89	IO179	179	GND_OUTER_EAST 2 6
6 2 PP_VDD_MAIN_1	90	IO90	IO180	180	PP_VDD_MAIN_5 2 6

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7 2 GND_OUTER_EAST	181	IO181	IO271	271	50_TRX_LB_PAD_ANT1 2 7
7 2 PP_VDD_MAIN_6	182	IO182	IO272	272	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	183	IO183	IO273	273	GND_PA_CAVITY 2 7
7 2 PP_VDD_MAIN_7	184	IO184	IO274	274	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	185	IO185	IO275	275	GND_OUTER_SOUTH 2 7
7 2 PP_VDD_MAIN_8	186	IO186	IO276	276	50_TRX_IN_LMB_PAD_2G_MB_OUT_M 2 7
7 2 GND_OUTER_EAST	187	IO187	IO277	277	GND_PA_CAVITY 2 7
7 2 GND_INNER_EAST	188	IO188	IO278	278	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	189	IO189	IO279	279	GND_PA_CAVITY 2 7
7 2 PP3V0_S2	190	IO190	IO280	280	50_TRX_IN_LMB_PAD_LMB_ANT_M 2 7
7 2 GND_OUTER_EAST	191	IO191	IO281	281	GND_OUTER_SOUTH 2 7
7 2 GND_INNER_EAST	192	IO192	IO282	282	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	193	IO193	IO283	283	GND_PA_CAVITY 2 7
7 2 GND_INNER_EAST	194	IO194	IO284	284	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	195	IO195	IO285	285	50_TRX_WLAN_G_BT_ANT3_NPLXR 2 7
7 2 GND_INNER_EAST	196	IO196	IO286	286	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	197	IO197	IO287	287	GND_OUTER_SOUTH 2 7
7 2 GND_INNER_EAST	198	IO198	IO288	288	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	199	IO199			
7 2 GPIO_BT_TO_BOT_SPKR_TRIG	200	IO200	IO290	290	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	201	IO201	IO291	291	50_TX_IN_XCVR_TX0_MB2G 2 7
7 2 GND_INNER_EAST	202	IO202	IO292	292	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	203	IO203	IO293	293	GND_OUTER_SOUTH 2 7
7 2 GND_INNER_EAST	204	IO204	IO294	294	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	205	IO205			
7 2 GND_INNER_EAST	206	IO206	IO296	296	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	207	IO207	IO297	297	50_TRX_ANT7_UHB_N79 2 7
7 2 GND_INNER_EAST	208	IO208	IO298	298	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	209	IO209	IO299	299	GND_OUTER_SOUTH 2 7
7 2 RFFE_WLAN_TO_LAT_2G_FEM_RST_L	210	IO210	IO300	300	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	211	IO211	IO301	301	50_TX_IN_XCVR_TX0_LMB 2 7
7 2 GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	212	IO212	IO302	302	GPIO_AOP_CANARY7_PIN_302 2 7
7 2 GND_OUTER_EAST	213	IO213	IO303	303	GND_PA_CAVITY 2 7
7 2 ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	214	IO214	IO304	304	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	215	IO215	IO305	305	GND_OUTER_SOUTH 2 7
7 2 PP_LDO6_VIO_1V8_SOUTH	216	IO216	IO306	306	PP_VDD_MAIN_9 2 7
7 2 GND_OUTER_EAST	217	IO217	IO307	307	PP_VDD_MAIN_10 2 7
7 2 SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	218	IO218	IO308	308	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	219	IO219	IO309	309	GND_OUTER_SOUTH 2 7
7 2 SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	220	IO220	IO310	310	GPIO_AOP_CANARY7_PIN_310 2 7
7 2 GND_OUTER_EAST	221	IO221	IO311	311	GND_SOUTHWEST 2 7
7 2 PP1V8_S2_2	222	IO222	IO312	312	GND_OUTER_SOUTH 2 7
7 2 GND_OUTER_EAST	223	IO223	IO313	313	×NC
7 2 GND_OUTER_EAST	224	IO224	IO314	314	GND_SOUTHWEST 2 7
7 2 GND_OUTER_EAST	225	IO225	IO315	315	GND_SOUTHWEST 2 7
7 2 50_RX_LMB_PAD_LMB_PRX_OUT_M	226	IO226	IO316	316	GND_PA_CAVITY 2 7
7 2 50_TX_IN_TX2_UHB_PAD_TX_N79_IN	227	IO227	IO317	317	GND_SOUTHWEST 2 7
7 2 GND_PA_CAVITY	228	IO228	IO318	318	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	229	IO229	IO319	319	GND_SOUTHWEST 2 7
7 2 GND_PA_CAVITY	230	IO230	IO320	320	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	231	IO231	IO321	321	GPIO_AOP_CANARY7_PIN_321 2 7
7 2 50_TX_IN_XCVR_TX0_LB	232	IO232	IO322	322	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	233	IO233	IO323	323	GND_SOUTHWEST 2 7
7 2 GND_PA_CAVITY	234	IO234	IO324	324	GND_SOUTHWEST 2 7
7 2 GND_OUTER_EAST	235	IO235	IO325	325	GND_SOUTHWEST 2 7
7 2 50_UHB_L_CPLR_OUT	236	IO236	IO326	326	GPIO_AOP_CANARY7_PIN_326 2 7
7 2 50_RX_XCVR_PRX6_LB_A_RX0	237	IO237	IO327	327	GND_SOUTHWEST 2 7
7 2 GND_PA_CAVITY	238	IO238	IO328	328	GPIO_AOP_CANARY7 2 7
7 2 GND_OUTER_EAST	239	IO239	IO329	329	GND_OUTER_WEST 2 7
7 2 GND_PA_CAVITY	240	IO240	IO330	330	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	241	IO241	IO331	331	GND_OUTER_WEST 2 7
7 2 PP_QET0_2G_PA_1	242	IO242	IO332	332	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	243	IO243	IO333	333	GND_OUTER_WEST 2 7
7 2 PP_QET0_2G_PA_2	244	IO244	IO334	334	GND_PA_CAVITY 2 7
7 2 GND_OUTER_EAST	245	IO245	IO335	335	GND_OUTER_WEST 2 7
7 2 PP_QET0_PA_1	246	IO246	IO336	336	50_TRX_PAUHBL_N79_ANT2_TO_ANT9 2 7
7 2 GND_OUTER_TAB_3	247	IO247	IO337	337	GND_OUTER_WEST 2 7
7 2 PP_QET0_PA_2	248	IO248	IO338	338	GND_PA_CAVITY 2 7
7 2 GND_OUTER_TAB_3	249	IO249	IO339	339	50_TRX_UHB_PAD_PORTB_TX_M 2 7
7 2 GND_PA_CAVITY	250	IO250	IO340	340	GND_PA_CAVITY 2 7
7 2 GND_OUTER_TAB_3	251	IO251	IO341	341	GND_OUTER_WEST 2 7
7 2 50_WLAN_G_C1_TXRX_FEM_M	252	IO252	IO342	342	50_TRX_UHB_PAD_N79_PORTB_TX_M 2 7
7 2 GND_OUTER_TAB_3	253	IO253	IO343	343	GND_OUTER_WEST 2 7
7 2 GND_PA_CAVITY	254	IO254	IO344	344	GND_PA_CAVITY 2 7
7 2 GND_OUTER_TAB_3	255	IO255	IO345	345	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9 2 7
7 2 SHIELD_RFFE1_SCLK_SDR	256	IO256	IO346	346	GND_PA_CAVITY 2 7
7 2 GND_OUTER_TAB_3	257	IO257	IO347	347	GND_OUTER_WEST 2 7
7 2 GND_OUTER_TAB_3	258	IO258	IO348	348	50_TRX_LB_PORTB_RX1_M 2 7
7 2 GND_OUTER_SOUTH	259	IO259	IO349	349	GND_OUTER_WEST 2 7
7 2 SHIELD_RFFE1_SDATA_SDR	260	IO260	IO350	350	GND_SOUTHWEST 2 7
7 2 GND_OUTER_SOUTH	261	IO261			
7 2 GND_PA_CAVITY	262	IO262	IO352	352	GND_PA_CAVITY 2 7
7 2 GPIO_AOP_CANARY7_PIN_263	263	IO263			
7 2 GND_PA_CAVITY	264	IO264	IO354	354	GND_INNER_WEST 2 7
7 2 GPIO_AOP_CANARY7_PIN_265	265	IO265	IO355	355	50_TX_IN_XCVR_TX0_LB2G 2 7
7 2 GND_PA_CAVITY	266	IO266	IO356	356	GND_INNER_WEST 2 7
7 2 GPIO_AOP_CANARY7_PIN_267	267	IO267	IO357	357	50_RX_XCVR_PRX10_LB_PRX_OUT2 2 7
7 2 GND_PA_CAVITY	268	IO268	IO358	358	50_TRX_LB_PORTB_TX_M 2 7
7 2 GND_OUTER_SOUTH	269	IO269	IO359	359	GND_PA_CAVITY 2 7
7 2 GND_PA_CAVITY	270	IO270	IO360	360	GND_INNER_WEST 2 7

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8 3	GND_PA_CAVITY	361	IO361	IO451	451 GND_OUTER_WEST 3 8
8 3	PP_APT_L_PA_1	362	IO362	IO452	452 GND_INNER_WEST 3 8
8 3	PP_APT_L_PA_2	363	IO363	IO453	453 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	364	IO364	IO454	454 GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA 3 8
8 3	GND_PA_CAVITY	365	IO365	IO455	455 GND_OUTER_WEST 3 8
8 3	PP_QET1_PA_1	366	IO366	IO456	456 I2S2_AP_FROM_BB_BCLK 3 8
8 3	PP_QET1_PA_2	367	IO367	IO457	457 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	368	IO368	IO458	458 I2S2_AP_FROM_BB_LRCLK 3 8
8 3	GND_PA_CAVITY	369	IO369	IO459	459 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	370	IO370	IO460	460 GND_INNER_WEST 3 8
8 3	50_RX_XCVR_PRX15_N79_RX_OUT2	371	IO371	IO461	461 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	372	IO372	IO462	462 I2S2_AP_FROM_BB_DIN 3 8
8 3	GND_PA_CAVITY	373	IO373	IO463	463 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	374	IO374	IO464	464 I2S2_AP_TO_BB_DOUT 3 8
8 3	50_RX_XCVR_PRX17_UHB_RX_OUT2	375	IO375	IO465	465 GND_OUTER_WEST 3 8
8 3	50_RX_XCVR_PRX14_N79_RX_OUT1	376	IO376	IO466	466 GND_INNER_WEST 3 8
8 3	GND_PA_CAVITY	377	IO377	IO467	467 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	378	IO378		
8 3	GND_PA_CAVITY	379	IO379	IO469	469 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	380	IO380	IO470	470 GND_INNER_WEST 3 8
8 3	50_RX_XCVR_PRX16_UHB_RX_OUT1	381	IO381	IO471	471 GND_OUTER_WEST 3 8
8 3	SHIELD_RFFE2_SDATA_SDR	382	IO382	IO472	472 GND_INNER_WEST 3 8
8 3	GND_PA_CAVITY	383	IO383	IO473	473 GND_OUTER_WEST 3 8
8 3	SHIELD_RFFE2_SCLK_SDR	384	IO384	IO474	474 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L 3 8
8 3	SHIELD_RFFE8_SDATA_SDR	385	IO385	IO475	475 GND_OUTER_WEST 3 8
8 3	SHIELD_RFFE8_SCLK_SDR	386	IO386	IO476	476 GPIO_S4_PMU_TO_WLAN_REG_ON 3 8
8 3	PP_VDD_BOOST_SOUTH_PA	387	IO387	IO477	477 GND_OUTER_WEST 3 8
8 3	GND_INNER_EAST	388	IO388	IO478	478 GPIO_PMU_FROM_WLAN_HOST_WAKE 3 8
8 3	GND_PA_CAVITY	389	IO389	IO479	479 GND_OUTER_WEST 3 8
8 3	GND_INNER_EAST	390	IO390	IO480	480 GND_INNER_WEST 3 8
8 3	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	391	IO391	IO481	481 GND_OUTER_WEST 3 8
8 3	GND_INNER_EAST	392	IO392	IO482	482 GPIO_SEQ_PMU_TO_BBPMU_RESET_L 3 8
8 3	GND_PA_CAVITY	393	IO393	IO483	483 GND_OUTER_WEST 3 8
8 3	GND_INNER_EAST	394	IO394	IO484	484 PCIE_GP1_AP_TO_WLAN_PERST_L 3 8
8 3	50_TX_IN_XCVR_TX1_LB_JB	395	IO395	IO485	485 GND_OUTER_WEST 3 8
8 3	SHIELD_RFFE3_SDATA_SDR	396	IO396	IO486	486 PCIE_GP1_AP_BI_WLAN_CLKREQ_L 3 8
8 3	GND_PA_CAVITY	397	IO397	IO487	487 GND_OUTER_WEST 3 8
8 3	SHIELD_RFFE3_SCLK_SDR	398	IO398	IO488	488 GND_OUTER_WEST 3 8
8 3	GND_PA_CAVITY	399	IO399	IO489	489 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	400	IO400	IO490	490 PCIE_GP2_AP_TO_BB_PERST_L 3 8
8 3	GND_OUTER_WEST	401	IO401	IO491	491 GND_OUTER_WEST 3 8
8 3	PP_VDD_MAIN_11	402	IO402	IO492	492 PCIE_GP2_AP_BI_BB_CLKREQ_L 3 8
8 3	GND_OUTER_WEST	403	IO403	IO493	493 GND_OUTER_WEST 3 8
8 3	PP_VDD_MAIN_12	404	IO404	IO494	494 SWD_AP_TO_MANY_SWCLK 3 8
8 3	GND_OUTER_WEST	405	IO405	IO495	495 GND_OUTER_WEST 3 8
8 3	PP_VDD_MAIN_13	406	IO406	IO496	496 GPIO_AP_TO_BB_COREDUMP 3 8
8 3	GND_OUTER_WEST	407	IO407	IO497	497 GND_OUTER_WEST 3 8
8 3	PP_VDD_MAIN_14	408	IO408		
8 3	GND_OUTER_WEST	409	IO409	IO499	499 GND_OUTER_WEST 3 8
8 3	GND_INNER_WEST	410	IO410	IO500	500 GPIO_AP_CANARY4 3 8
8 3	GND_OUTER_WEST	411	IO411	IO501	501 GND_OUTER_TAB_5 3 8
8 3	GND_INNER_WEST	412	IO412	IO502	502 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	413	IO413	IO503	503 GND_OUTER_TAB_5 3 8
8 3	PP1V2_S2_1	414	IO414	IO504	504 CLK_BBPMU_TO_NFC_38M4 3 8
8 3	GND_OUTER_WEST	415	IO415	IO505	505 GND_OUTER_TAB_5 3 8
8 3	GND_INNER_WEST	416	IO416	IO506	506 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	417	IO417	IO507	507 GND_OUTER_TAB_5 3 8
8 3	GND_INNER_WEST	418	IO418	IO508	508 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N 3 8
8 3	GND_OUTER_WEST	419	IO419	IO509	509 GND_OUTER_TAB_5 3 8
8 3	GPIO_SCM_AOP_FROM_JARVIS_INT	420	IO420	IO510	510 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P 3 8
8 3	GND_OUTER_WEST	421	IO421	IO511	511 GND_OUTER_TAB_5 3 8
8 3	I2C1_AOP_SCL	422	IO422	IO512	512 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	423	IO423	IO513	513 GND_OUTER_TAB_5 3 8
8 3	I2C1_AOP_SDA	424	IO424	IO514	514 90_PCIE_GP1_AP_FROM_WLAN_RX_N 3 8
8 3	GND_OUTER_WEST	425	IO425	IO515	515 GND_OUTER_TAB_5 3 8
8 3	GND_INNER_WEST	426	IO426	IO516	516 90_PCIE_GP1_AP_FROM_WLAN_RX_P 3 8
8 3	GND_OUTER_WEST	427	IO427	IO517	517 GND_OUTER_NORTHWEST 3 8
8 3	90_PCIE_GP2_AP_TO_BB_TX_N	428	IO428	IO518	518 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	429	IO429	IO519	519 GND_OUTER_NORTHWEST 3 8
8 3	90_PCIE_GP2_AP_TO_BB_TX_P	430	IO430	IO520	520 90_PCIE_GP1_AP_TO_WLAN_TX_P 3 8
8 3	GND_OUTER_WEST	431	IO431	IO521	521 GND_OUTER_NORTHWEST 3 8
8 3	GND_INNER_WEST	432	IO432	IO522	522 90_PCIE_GP1_AP_TO_WLAN_TX_N 3 8
8 3	GND_OUTER_WEST	433	IO433	IO523	523 GND_OUTER_NORTHWEST 3 8
8 3	90_PCIE_GP2_AP_FROM_BB_RX_P	434	IO434	IO524	524 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	435	IO435	IO525	525 GND_OUTER_NORTHWEST 3 8
8 3	90_PCIE_GP2_AP_FROM_BB_RX_N	436	IO436	IO526	526 CLK_BBPMU_TO_DOTARA_38M4 3 8
8 3	GND_OUTER_WEST	437	IO437	IO527	527 GND_OUTER_NORTHWEST 3 8
8 3	GND_INNER_WEST	438	IO438	IO528	528 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	439	IO439	IO529	529 GND_OUTER_NORTHWEST 3 8
8 3	90_PCIE_GP2_AP_TO_BB_REFCLK_N	440	IO440	IO530	530 GPIO_SP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG 3 8
8 3	GND_OUTER_WEST	441	IO441	IO531	531 GND_OUTER_NORTHWEST 3 8
8 3	90_PCIE_GP2_AP_TO_BB_REFCLK_P	442	IO442	IO532	532 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	443	IO443	IO533	533 GND_OUTER_NORTHWEST 3 8
8 3	GND_INNER_WEST	444	IO444	IO534	534 GPIO_AP_CANARY2 3 8
8 3	GND_OUTER_WEST	445	IO445	IO535	535 GND_OUTER_NORTHWEST 3 8
8 3	PP_VDD_MAIN_15	446	IO446		
8 3	GND_OUTER_WEST	447	IO447	IO537	537 GND_OUTER_NORTHWEST 3 8
8 3	PP_VDD_MAIN_16	448	IO448	IO538	538 GND_INNER_NORTHWEST 3 8
8 3	GND_OUTER_WEST	449	IO449	IO539	539 GND_INNER_NORTHWEST 3 8
8 3	PP_VDD_MAIN_17	450	IO450	IO540	540 GND_INNER_NORTHWEST 3 8

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9 3	GND_OUTER_NORTHWEST	541	IO541	IO631	631 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	542	IO542	IO632	632 SHIELD_RFFE5_SDATA_SDR 3 9
9 3	50_WLAN_A_C0_TXRX_FEM_M	543	IO543	IO633	633 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	544	IO544	IO634	634 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTHWEST	545	IO545	IO635	635 GND_OUTER_NORTH 3 9
9 3	50_WLAN_G_C0_TXRX_FEM_M	546	IO546	IO636	636 SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK 3 9
9 3	GND_OUTER_NORTHWEST	547	IO547	IO637	637 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	548	IO548	IO638	638 SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA 3 9
9 3	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	549	IO549	IO639	639 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	550	IO550	IO640	640 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTHWEST	551	IO551	IO641	641 GND_OUTER_NORTH 3 9
9 3	50_TRX_PAUHBU_N79_ANT1_TO_ANT4	552	IO552	IO642	642 UAT_SUBUS_B 3 9
9 3	GND_OUTER_NORTHWEST	553	IO553	IO643	643 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	554	IO554	IO644	644 UAT_SUBUS_A 3 9
9 3	GND_OUTER_NORTHWEST	555	IO555	IO645	645 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	556	IO556	IO646	646 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTHWEST	557	IO557	IO647	647 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	558	IO558	IO648	648 NTC_RADIO_PA_P 3 9
9 3	GND_OUTER_NORTHWEST	559	IO559	IO649	649 GND_OUTER_NORTH 3 9
9 3	IO_NFC_TO_BBPMU_CLKREQ	560	IO560	IO650	650 UAT_TUNER_TO_R1_STATE 3 9
9 3	GND_OUTER_NORTHWEST	561	IO561	IO651	651 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	562	IO562	IO652	652 GPIO_R1_TO_BB_CH9_COEX 3 9
9 3	GND_OUTER_NORTHWEST	563	IO563	IO653	653 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	564	IO564	IO654	654 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_TAB_6	565	IO565	IO655	655 GND_OUTER_NORTH 3 9
9 3	GND_OUTER_TAB_6	566	IO566	IO656	656 GPIO_R1_TO_WLAN_COEX 3 9
9 3	GND_OUTER_TAB_6	567	IO567	IO657	657 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	568	IO568	IO658	658 PP1V2_S2_2 3 9
9 3	GND_OUTER_TAB_6	569	IO569	IO659	659 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	570	IO570	IO660	660 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_TAB_6	571	IO571	IO661	661 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	572	IO572	IO662	662 GPIO_CAM_PMU1_TO_PVDD_RESET_L 3 9
9 3	GND_OUTER_TAB_6	573	IO573	IO663	663 GND_OUTER_NORTH 3 9
9 3	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	574	IO574	IO664	664 I2C4_CAM_PMU1_SCL_1V8 3 9
9 3	GND_OUTER_TAB_6	575	IO575	IO665	665 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	576	IO576	IO666	666 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_TAB_6	577	IO577	IO667	667 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	578	IO578	IO668	668 I2C4_CAM_PMU1_SDA_1V8 3 9
9 3	GND_OUTER_NORTH	579	IO579	IO669	669 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	580	IO580	IO670	670 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	581	IO581	IO671	671 GND_OUTER_NORTH 3 9
9 3	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	582	IO582	IO672	672 GND_OUTER_NORTH 3 9
9 3	GND_OUTER_NORTH	583	IO583	IO673	673 GND_OUTER_NORTH 3 9
9 3	50_TRX_ANT8_UHB_N79	584	IO584	IO674	674 GND_OUTER_NORTH 3 9
9 3	GND_OUTER_NORTH	585	IO585	IO675	675 GPIO_SCM_AOP_FROM_IMU_DATARDY 3 9
9 3	GND_OUTER_NORTH	586	IO586	IO676	676 GPIO_AP_CANARY1_PIN_676 3 9
9 3	GND_OUTER_NORTH	587	IO587	IO677	677 GPIO_AP_CANARY1_PIN_677 3 9
9 3	GND_INNER_NORTHWEST	588	IO588	IO678	678 SPI0_AOP_FROM_IMU_R1_MISO 3 9
9 3	GND_OUTER_NORTH	589	IO589	IO679	679 PP_STROBE_DRIVER_COOL_LED_1 3 9
9 3	GPIO_AP_CANARY1_PIN_591	591	IO591	IO680	680 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	592	IO592	IO681	681 GPIO_SCM_AOP_TO_IMU_SPI_CS_L 3 9
9 3	GND_NORTHWEST	593	IO593	IO682	682 PP_STROBE_DRIVER_COOL_LED_2 3 9
9 3	GPIO_AP_CANARY1_PIN_594	594	IO594	IO683	683 GPIO_AP_CANARY1_PIN_683 3 9
9 3	GND_NORTHWEST	595	IO595	IO684	684 GND_OUTER_NORTH 3 9
9 3	GND_OUTER_NORTH	596	IO596	IO685	685 GND_INNER_NORTHEAST 3 9
		597	IO597	IO686	686 GND_OUTER_NORTH 3 9
	NC		IO598	IO687	687 SPI0_AOP_TO_IMU_R1_MOSI 3 9
9 3	GND_NORTHWEST	598	IO599	IO688	688 PP_STROBE_DRIVER_WARM_LED_1 3 9
9 3	GND_OUTER_NORTH	599	IO600	IO689	689 GPIO_AP_CANARY1_PIN_689 3 9
9 3	GND_INNER_NORTHWEST	600	IO601	IO690	690 SPI0_AOP_TO_IMU_R1_SCLK 3 9
9 3	GND_NORTHWEST	601	IO602	IO691	691 PP_STROBE_DRIVER_WARM_LED_2 3 9
9 3	GND_INNER_NORTHWEST	602	IO603	IO692	692 GND_OUTER_NORTH 3 9
9 3	GND_NORTHWEST	603	IO604	IO693	693 GND_OUTER_NORTH 3 9
9 3	GND_NORTHWEST	604	IO605	IO694	694 GND_INNER_NORTHEAST 3 9
9 3	GPIO_AP_CANARY1_PIN_605	605	IO606	IO695	695 GPIO_AP_CANARY1_PIN_695 3 9
9 3	GND_INNER_NORTHWEST	606	IO607	IO696	696 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	607	IO608	IO697	697 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	608	IO609	IO698	698 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	609	IO610	IO699	699 GND_OUTER_NORTH 3 9
9 3	GND_INNER_NORTHWEST	610	IO611	IO700	700 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	611	IO612	IO701	701 GND_OUTER_NORTH 3 9
9 3	GND_OUTER_NORTH	612	IO613	IO702	702 GND_INNER_NORTHEAST 3 9
9 3	GPIO_AP_CANARY1_PIN_613	613	IO614	IO703	703 GND_OUTER_NORTH 3 9
9 3	PP_LDO6_VIO_1V8_NORTH	614	IO615	IO704	704 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	615	IO616	IO705	705 GND_OUTER_NORTH 3 9
9 3	GPIO_BB_TO_R1_COEX	616	IO617	IO706	706 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	617	IO618	IO707	707 GND_OUTER_NORTH 3 9
9 3	IO_BT_TO_R1_TIME_SYNC	618	IO619	IO708	708 GPIO_AP_CANARY6_PIN_708 3 9
9 3	GND_OUTER_NORTH	619	IO620	IO709	709 GND_OUTER_NORTH 3 9
9 3	GPIO_WLAN_TO_R1_COEX	620	IO621	IO710	710
9 3	GND_OUTER_NORTH	621	IO622	IO711	711 GND_NORTHEAST 3 9
9 3	GND_INNER_NORTHEAST	622	IO623	IO712	712 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	623	IO624	IO713	713 GPIO_AP_CANARY6_PIN_713 3 9
9 3	GND_INNER_NORTHEAST	624	IO625	IO714	714 GND_INNER_NORTHEAST 3 9
9 3	50_TRX_ANT2_LB_LMB_MB_HB_L1	625	IO626	IO715	715 GND_NORTHEAST 3 9
9 3	GND_INNER_NORTHEAST	626	IO627	IO716	716 GND_INNER_NORTHEAST 3 9
9 3	50_LAA_RX_XCVR_DRX10	627	IO628	IO717	717 GPIO_AP_CANARY6_PIN_717 3 9
9 3	GND_OUTER_NORTH	628	IO629	IO718	718 GND_INNER_NORTHEAST 3 9
9 3	GND_OUTER_NORTH	629	IO630	IO719	719 GND_NORTHEAST 3 9
9 3	SHIELD_RFFE5_SCLK_SDR	630		IO720	720 GPIO_AP_CANARY6_PIN_720 3 9
				IO721	721 GPIO_AP_CANARY6_PIN_721 3 9
				IO722	722 GND_NORTHEAST 3 9
				IO723	723 GND_NORTHEAST 3 9
				IO724	724 GND_INNER_NORTHEAST 3 9
				IO725	725 GND_INNER_NORTHEAST 3 9
				IO726	726 GND_INNER_NORTHWEST 3 9
				IO727	727 GND_INNER_NORTHWEST 3 9

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Interposer Aliases (1/4)

4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GPIO_AP_CANARY6_PIN_7	GPIO_AP_CANARY6_PIN_7	MAKE_BASE=TRUE	
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY6_PIN_10	GPIO_AP_CANARY6_PIN_10	MAKE_BASE=TRUE	
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY6_PIN_15	GPIO_AP_CANARY6_PIN_15	MAKE_BASE=TRUE	
4 2	GPIO_AP_CANARY6	GPIO_AP_CANARY6	MAKE_BASE=TRUE	
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	PP1V8_S2_1	PP1V8_S2_1	MAKE_BASE=TRUE	
4 2	GND_OUTER_NORTHEAST_PENINSULA	GND_OUTER_NORTHEAST_PENINSULA	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	GPIO_ISP_RCAM_TO_STROBE_TRIGGER_1V8	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	IO_R1_TO_BB_LAA_SW_CTRL	IO_R1_TO_BB_LAA_SW_CTRL	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	IO_BT_TO_R1_WAKE	IO_BT_TO_R1_WAKE	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	PPVAR_RCAM_PVDD	PPVAR_RCAM_PVDD	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_1	GND_OUTER_TAB_1	MAKE_BASE=TRUE	6
4 2	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_BB_TO_R1_CH9_REQ	GPIO_BB_TO_R1_CH9_REQ	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	NTC_STROBE_MODULE	NTC_STROBE_MODULE	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5	GPIO_AP_CANARY5	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5_PIN_47	GPIO_AP_CANARY5_PIN_47	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5_PIN_51	GPIO_AP_CANARY5_PIN_51	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5_PIN_54	GPIO_AP_CANARY5_PIN_54	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT		6
4 2	GPIO_AP_CANARY5_PIN_63	GPIO_AP_CANARY5_PIN_63	MAKE_BASE=TRUE	
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5_PIN_67	GPIO_AP_CANARY5_PIN_67	MAKE_BASE=TRUE	
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5_PIN_69	GPIO_AP_CANARY5_PIN_69	MAKE_BASE=TRUE	
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY5_PIN_87	GPIO_AP_CANARY5_PIN_87	MAKE_BASE=TRUE	
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	PP_VDD_MAIN_1	PP_VDD_MAIN_1	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	

4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	PP_VDD_MAIN_2	PP_VDD_MAIN_2	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	PP_VDD_MAIN_3	PP_VDD_MAIN_3	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	PP_VDD_MAIN_4	PP_VDD_MAIN_4	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GPIO_AP_CANARY3	GPIO_AP_CANARY3	MAKE_BASE=TRUE	
4 2	GND_OUTER_ARMPIT	GND_OUTER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	PP_VDD_BOOST_NORTH_PA	PP_VDD_BOOST_NORTH_PA	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2 CKPLUS_WAIVE=SYNONYM_CHECK	MAKE_BASE=TRUE	6
4 2	PP1V2_S4	PP1V2_S4	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	PP1V8_S4	PP1V8_S4	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	RFFE_WLAN_TO_UAT_2G_FEM_RST_L	RFFE_WLAN_TO_UAT_2G_FEM_RST_L	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	MAKE_BASE=TRUE	
4 2	GND_OUTER_TAB_2	GND_OUTER_TAB_2	MAKE_BASE=TRUE	6
4 2	GPIO_SE_TO_BT_PKT_RDY	GPIO_SE_TO_BT_PKT_RDY	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	I2C_BT_TO_NFC_SCL	I2C_BT_TO_NFC_SCL	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST CKPLUS_WAIVE=I2C_PULLUP	MAKE_BASE=TRUE	6 7
4 2	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_ARMPIT	GND_INNER_ARMPIT	MAKE_BASE=TRUE	6
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	I2C_BT_TO_NFC_SDA	I2C_BT_TO_NFC_SDA	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST CKPLUS_WAIVE=I2C_PULLUP	MAKE_BASE=TRUE	6 7
4 2	GPIO_AP_FROM_WLAN_TIME_SYNC	GPIO_AP_FROM_WLAN_TIME_SYNC	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_AP_TO_BB_PEAK_PWR_IND	GPIO_AP_TO_BB_PEAK_PWR_IND	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	SWD_AP_BI_BB_SWDIO	SWD_AP_BI_BB_SWDIO	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_AP_FROM_BB_RESET_DETECT_L	GPIO_AP_FROM_BB_RESET_DETECT_L	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_AP_FROM_BT_AUDIO_SYNC	GPIO_AP_FROM_BT_AUDIO_SYNC	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_AP_TO_BB_TIME_MARK	GPIO_AP_TO_BB_TIME_MARK	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	NTC_RADIO_BB_P	NTC_RADIO_BB_P	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST CKPLUS_WAIVE=MISS_N_DIFFPAIR	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	UART1_AOP_FROM_BB_RXD	UART1_AOP_FROM_BB_RXD	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	UART1_AOP_TO_BB_TXD	UART1_AOP_TO_BB_TXD	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_AOP_TO_BB_FORCE_PWM	GPIO_AOP_TO_BB_FORCE_PWM	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	PP_VDD_RF_1V2	PP_VDD_RF_1V2	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	PP_VDD_BOOST_BBPMU	PP_VDD_BOOST_BBPMU	MAKE_BASE=TRUE	
4 2	GND_OUTER_EAST	GND_OUTER_EAST CKPLUS_WAIVE=SYNONYM_CHECK	MAKE_BASE=TRUE	6 7
4 2	GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
4 2	GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
4 2	PP_VDD_MAIN_5	PP_VDD_MAIN_5	MAKE_BASE=TRUE	

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Interposer Aliases (2/4)

GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_VDD_MAIN_6	PP_VDD_MAIN_6	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_VDD_MAIN_7	PP_VDD_MAIN_7	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_VDD_MAIN_8	PP_VDD_MAIN_8	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP3V0_S2	PP3V0_S2	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GPIO_BT_TO_BOT_SPKR_TRIG	GPIO_BT_TO_BOT_SPKR_TRIG	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_INNER_EAST	GND_INNER_EAST	MAKE_BASE=TRUE	6 7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
RFFE_WLAN_TO_LAT_2G_FEM_RST_L	RFFE_WLAN_TO_LAT_2G_FEM_RST_L	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	ANALOG_LAT_2G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_LDO6_VIO_1V8_SOUTH	PP_LDO6_VIO_1V8_SOUTH	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	6 7
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP1V8_S2_2	PP1V8_S2_2	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
50_RX_LMB_PAD_LMB_PRX_OUT_M	50_RX_LMB_PAD_LMB_PRX_OUT_M	MAKE_BASE=TRUE	
50_TX_IN_TX2_UHB_PAD_TX_N79_IN	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
50_TX_IN_XCVR_TX0_LB	50_TX_IN_XCVR_TX0_LB	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
50_UHB_L_CPLR_OUT	50_UHB_L_CPLR_OUT	MAKE_BASE=TRUE	
50_RX_XCVR_PRX6_LB_A_RX0	50_RX_XCVR_PRX6_LB_A_RX0	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_QET0_2G_PA_1	PP_QET0_2G_PA_1	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_QET0_2G_PA_2	PP_QET0_2G_PA_2	MAKE_BASE=TRUE	
GND_OUTER_EAST	GND_OUTER_EAST	MAKE_BASE=TRUE	6 7
PP_QET0_PA_1	PP_QET0_PA_1	MAKE_BASE=TRUE	
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
PP_QET0_PA_2	PP_QET0_PA_2	MAKE_BASE=TRUE	
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
50_WLAN_G_C1_TXRX_FEM_M	50_WLAN_G_C1_TXRX_FEM_M	MAKE_BASE=TRUE	
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
SHIELD_RFFE1_SCLK_SDR	SHIELD_RFFE1_SCLK_SDR	MAKE_BASE=TRUE	
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
GND_OUTER_TAB_3	GND_OUTER_TAB_3	MAKE_BASE=TRUE	7
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
SHIELD_RFFE1_SDATA_SDR	SHIELD_RFFE1_SDATA_SDR	MAKE_BASE=TRUE	
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GPIO_AOP_CANARY7_PIN_263	GPIO_AOP_CANARY7_PIN_263	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GPIO_AOP_CANARY7_PIN_265	GPIO_AOP_CANARY7_PIN_265	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GPIO_AOP_CANARY7_PIN_267	GPIO_AOP_CANARY7_PIN_267	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8

50_TRX_LB_PAD_ANT1	50_TRX_LB_PAD_ANT1		
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
50_TRX_IN_LMB_PAD_2G_MB_OUT_M	50_TRX_IN_LMB_PAD_2G_MB_OUT_M	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
50_TRX_IN_LMB_PAD_LMB_ANT_M	50_TRX_IN_LMB_PAD_LMB_ANT_M	MAKE_BASE=TRUE	
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
50_TRX_WLAN_G_BT_ANT3_NPLXR	50_TRX_WLAN_G_BT_ANT3_NPLXR	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
50_TX_IN_XCVR_TX0_MB2G	50_TX_IN_XCVR_TX0_MB2G	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
50_TRX_ANT7_UHB_N79	50_TRX_ANT7_UHB_N79	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
50_TX_IN_XCVR_TX0_LMB	50_TX_IN_XCVR_TX0_LMB	MAKE_BASE=TRUE	
GPIO_AOP_CANARY7_PIN_302	GPIO_AOP_CANARY7_PIN_302	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
PP_VDD_MAIN_9	PP_VDD_MAIN_9	MAKE_BASE=TRUE	
PP_VDD_MAIN_10	PP_VDD_MAIN_10	MAKE_BASE=TRUE	
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GPIO_AOP_CANARY7_PIN_310	GPIO_AOP_CANARY7_PIN_310	MAKE_BASE=TRUE	
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_OUTER_SOUTH	GND_OUTER_SOUTH	MAKE_BASE=TRUE	7
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GPIO_AOP_CANARY7_PIN_321	GPIO_AOP_CANARY7_PIN_321	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GPIO_AOP_CANARY7_PIN_326	GPIO_AOP_CANARY7_PIN_326	MAKE_BASE=TRUE	
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GPIO_AOP_CANARY7	GPIO_AOP_CANARY7	MAKE_BASE=TRUE	
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
50_TRX_PAUHBL_N79_ANT2_TO_ANT9	50_TRX_PAUHBL_N79_ANT2_TO_ANT9	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
50_TRX_UHB_PAD_PORTB_TX_M	50_TRX_UHB_PAD_PORTB_TX_M	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	7 8
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
50_TRX_UHB_PAD_N79_PORTB_TX_M	50_TRX_UHB_PAD_N79_PORTB_TX_M	MAKE_BASE=TRUE	
GND_OUTER_WEST	GND_OUTER_WEST	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	7 8
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	7 8
GND_OUTER_WEST	GND_OUTER_WEST	MAKE_BASE=TRUE	7 8
50_TRX_LB_PORTB_RX1_M	50_TRX_LB_PORTB_RX1_M	MAKE_BASE=TRUE	
GND_OUTER_WEST	GND_OUTER_WEST	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	7 8
GND_SOUTHWEST	GND_SOUTHWEST	MAKE_BASE=TRUE	7 9
GND_PA_CAVITY	GND_PA_CAVITY	MAKE_BASE=TRUE	7 8
GND_INNER_WEST	GND_INNER_WEST	MAKE_BASE=TRUE	7 8
50_TX_IN_XCVR_TX0_LB2G	50_TX_IN_XCVR_TX0_LB2G	MAKE_BASE=TRUE	
GND_INNER_WEST	GND_INNER_WEST	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	7 8
50_RX_XCVR_PRX10_LB_PRX_OUT2	50_RX_XCVR_PRX10_LB_PRX_OUT2	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	
50_TRX_LB_PORTB_TX_M	50_TRX_LB_PORTB_TX_M	MAKE_BASE=TRUE	
GND_PA_CAVITY	GND_PA_CAVITY	CKPLUS_WAIVE=SYNONYM_CHECK MAKE_BASE=TRUE	7 8
GND_INNER_WEST	GND_INNER_WEST	MAKE_BASE=TRUE	7 8

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Interposer Aliases (3/4)

5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	PP_APT_L_PA_1	PP_APT_L_PA_1		MAKE_BASE=TRUE	
5 3	PP_APT_L_PA_2	PP_APT_L_PA_2		MAKE_BASE=TRUE	
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	PP_QET1_PA_1	PP_QET1_PA_1		MAKE_BASE=TRUE	
5 3	PP_QET1_PA_2	PP_QET1_PA_2		MAKE_BASE=TRUE	
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	50_RX_XCVR_PRX15_N79_RX_OUT2	50_RX_XCVR_PRX15_N79_RX_OUT2		MAKE_BASE=TRUE	
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	50_RX_XCVR_PRX17_UHB_RX_OUT2	50_RX_XCVR_PRX17_UHB_RX_OUT2		MAKE_BASE=TRUE	
5 3	50_RX_XCVR_PRX14_N79_RX_OUT1	50_RX_XCVR_PRX14_N79_RX_OUT1		MAKE_BASE=TRUE	
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	50_RX_XCVR_PRX16_UHB_RX_OUT1	50_RX_XCVR_PRX16_UHB_RX_OUT1		MAKE_BASE=TRUE	
5 3	SHIELD_RFFE2_SDATA_SDR	SHIELD_RFFE2_SDATA_SDR		MAKE_BASE=TRUE	
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	SHIELD_RFFE2_SCLK_SDR	SHIELD_RFFE2_SCLK_SDR		MAKE_BASE=TRUE	
5 3	SHIELD_RFFE8_SDATA_SDR	SHIELD_RFFE8_SDATA_SDR		MAKE_BASE=TRUE	
5 3	SHIELD_RFFE8_SCLK_SDR	SHIELD_RFFE8_SCLK_SDR		MAKE_BASE=TRUE	
5 3	PP_VDD_BOOST_SOUTH_PA	PP_VDD_BOOST_SOUTH_PA		MAKE_BASE=TRUE	
5 3	GND_INNER_EAST	GND_INNER_EAST	CKPLUS_WAIVE=SYNONYM_CHECK	MAKE_BASE=TRUE	6 7 8
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_EAST	GND_INNER_EAST		MAKE_BASE=TRUE	6 7 8
5 3	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1		MAKE_BASE=TRUE	
5 3	GND_INNER_EAST	GND_INNER_EAST		MAKE_BASE=TRUE	6 7 8
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_EAST	GND_INNER_EAST		MAKE_BASE=TRUE	6 7 8
5 3	50_TX_IN_XCVR_TX1_LB_JB	50_TX_IN_XCVR_TX1_LB_JB		MAKE_BASE=TRUE	
5 3	SHIELD_RFFE3_SDATA_SDR	SHIELD_RFFE3_SDATA_SDR		MAKE_BASE=TRUE	
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	SHIELD_RFFE3_SCLK_SDR	SHIELD_RFFE3_SCLK_SDR		MAKE_BASE=TRUE	
5 3	GND_PA_CAVITY	GND_PA_CAVITY		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_11	PP_VDD_MAIN_11		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_12	PP_VDD_MAIN_12		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_13	PP_VDD_MAIN_13		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_14	PP_VDD_MAIN_14		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP1V2_S2_1	PP1V2_S2_1		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST	CKPLUS_WAIVE=SYNONYM_CHECK	MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_SCM_AOP_FROM_JARVIS_INT	GPIO_SCM_AOP_FROM_JARVIS_INT		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	I2C1_AOP_SCL	I2C1_AOP_SCL		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST	CKPLUS_WAIVE=I2C_PULLUP	MAKE_BASE=TRUE	7 8
5 3	I2C1_AOP_SDA	I2C1_AOP_SDA		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST	CKPLUS_WAIVE=I2C_PULLUP	MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	90_PCIE_GP2_AP_TO_BB_TX_N	90_PCIE_GP2_AP_TO_BB_TX_N		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	90_PCIE_GP2_AP_TO_BB_TX_P	90_PCIE_GP2_AP_TO_BB_TX_P		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	90_PCIE_GP2_AP_FROM_BB_RX_P	90_PCIE_GP2_AP_FROM_BB_RX_P		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	90_PCIE_GP2_AP_FROM_BB_RX_N	90_PCIE_GP2_AP_FROM_BB_RX_N		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	90_PCIE_GP2_AP_TO_BB_REFCLK_N	90_PCIE_GP2_AP_TO_BB_REFCLK_N		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	90_PCIE_GP2_AP_TO_BB_REFCLK_P	90_PCIE_GP2_AP_TO_BB_REFCLK_P		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_15	PP_VDD_MAIN_15		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_16	PP_VDD_MAIN_16		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PP_VDD_MAIN_17	PP_VDD_MAIN_17		MAKE_BASE=TRUE	

5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	I2S2_AP_FROM_BB_BCLK	I2S2_AP_FROM_BB_BCLK		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	I2S2_AP_FROM_BB_LRCLK	I2S2_AP_FROM_BB_LRCLK		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	I2S2_AP_FROM_BB_DIN	I2S2_AP_FROM_BB_DIN		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	I2S2_AP_TO_BB_DOUT	I2S2_AP_TO_BB_DOUT		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO_S4_PMU_TO_WLAN_REG_ON		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_INNER_WEST	GND_INNER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	GPIO_SEQ_PMU_TO_BBPMU_RESET_L		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PCIE_GP1_AP_TO_WLAN_PERST_L	PCIE_GP1_AP_TO_WLAN_PERST_L		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	PCIE_GP1_AP_BI_WLAN_CLKREQ_L		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PCIE_GP2_AP_TO_BB_PERST_L	PCIE_GP2_AP_TO_BB_PERST_L		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	PCIE_GP2_AP_BI_BB_CLKREQ_L	PCIE_GP2_AP_BI_BB_CLKREQ_L		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	SWD_AP_TO_MANY_SWCLK	SWD_AP_TO_MANY_SWCLK		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_AP_TO_BB_COREDUMP	GPIO_AP_TO_BB_COREDUMP		MAKE_BASE=TRUE	
5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8

5 3	GND_OUTER_WEST	GND_OUTER_WEST		MAKE_BASE=TRUE	7 8
5 3	GPIO_AP_CANARY4	GPIO_AP_CANARY4		MAKE_BASE=TRUE	
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	CLK_BBPMU_TO_NFC_38M4	CLK_BBPMU_TO_NFC_38M4		MAKE_BASE=TRUE	
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N		MAKE_BASE=TRUE	
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P		MAKE_BASE=TRUE	
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	90_PCIE_GP1_AP_FROM_WLAN_RX_N	90_PCIE_GP1_AP_FROM_WLAN_RX_N		MAKE_BASE=TRUE	
5 3	GND_OUTER_TAB_5	GND_OUTER_TAB_5		MAKE_BASE=TRUE	8
5 3	90_PCIE_GP1_AP_FROM_WLAN_RX_P	90_PCIE_GP1_AP_FROM_WLAN_RX_P		MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	90_PCIE_GP1_AP_TO_WLAN_TX_P	90_PCIE_GP1_AP_TO_WLAN_TX_P		MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	90_PCIE_GP1_AP_TO_WLAN_TX_N	90_PCIE_GP1_AP_TO_WLAN_TX_N		MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	CLK_BBPMU_TO_DOTARA_38M4	CLK_BBPMU_TO_DOTARA_38M4		MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG		MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GPIO_AP_CANARY2	GPIO_AP_CANARY2		MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST		MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST		MAKE_BASE=TRUE	8 9

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Interposer Aliases (4/4)

5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	50_WLAN_A_C0_TXRX_FEM_M	50_WLAN_A_C0_TXRX_FEM_M	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	50_WLAN_G_C0_TXRX_FEM_M	50_WLAN_G_C0_TXRX_FEM_M	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	50_TRX_PAUHBU_N79_ANT1_TO_ANT4	50_TRX_PAUHBU_N79_ANT1_TO_ANT4	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	IO_NFC_TO_BBPMU_CLKREQ	IO_NFC_TO_BBPMU_CLKREQ	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTHWEST	GND_OUTER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	ANALOG_UAT_2G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE	
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_TAB_6	GND_OUTER_TAB_6	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	50_TRX_ANT8_UHB_N79	50_TRX_ANT8_UHB_N79	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_NORTHWEST	GND_NORTHWEST	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_NORTHWEST	GND_NORTHWEST	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_NORTHWEST	GND_NORTHWEST	MAKE_BASE=TRUE	9
5 3	GND_NORTHWEST	GND_NORTHWEST	MAKE_BASE=TRUE	9
5 3	GPIO_AP_CANARY1_PIN_605	GPIO_AP_CANARY1_PIN_605	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_AP_CANARY1_PIN_613	GPIO_AP_CANARY1_PIN_613	MAKE_BASE=TRUE	
5 3	PP_LDO6_VIO_1V8_NORTH	PP_LDO6_VIO_1V8_NORTH	CKPLUS_WAIVE=SYNONYM_CHECK	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_BB_TO_R1_COEX	GPIO_BB_TO_R1_COEX	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	IO_BT_TO_R1_TIME_SYNC	IO_BT_TO_R1_TIME_SYNC	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_WLAN_TO_R1_COEX	GPIO_WLAN_TO_R1_COEX	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	50_TRX_ANT2_LB_LMB_MB_HB_L1	50_TRX_ANT2_LB_LMB_MB_HB_L1	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	50_LAA_RX_XCVR_DRX10	50_LAA_RX_XCVR_DRX10	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	SHIELD_RFFE5_SCLK_SDR	SHIELD_RFFE5_SCLK_SDR	MAKE_BASE=TRUE	

5 3	GND_OUTER_NORTH	GND_OUTER_NORTH		9
5 3	SHIELD_RFFE5_SDATA_SDR	SHIELD_RFFE5_SDATA_SDR	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	UAT_SUBUS_B	UAT_SUBUS_B	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	UAT_SUBUS_A	UAT_SUBUS_A	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	NTC_RADIO_PA_P	NTC_RADIO_PA_P	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	CKPLUS_WAIVE=MISS_N_DIFFPAIR	9
5 3	UAT_TUNER_TO_R1_STATE	UAT_TUNER_TO_R1_STATE	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_R1_TO_BB_CH9_COEX	GPIO_R1_TO_BB_CH9_COEX	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_R1_TO_WLAN_COEX	GPIO_R1_TO_WLAN_COEX	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	PP1V2_S2_2	PP1V2_S2_2	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_CAM_PMU1_TO_PVDD_RESET_L	GPIO_CAM_PMU1_TO_PVDD_RESET_L	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	I2C4_CAM_PMU1_SCL_1V8	I2C4_CAM_PMU1_SCL_1V8	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	CKPLUS_WAIVE=I2C_PULLUP MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	I2C4_CAM_PMU1_SDA_1V8	I2C4_CAM_PMU1_SDA_1V8	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	CKPLUS_WAIVE=I2C_PULLUP MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_SCM_AOP_FROM_IMU_DATARDY	GPIO_SCM_AOP_FROM_IMU_DATARDY	MAKE_BASE=TRUE	
5 3	GPIO_AP_CANARY1_PIN_676	GPIO_AP_CANARY1_PIN_676	MAKE_BASE=TRUE	
5 3	GPIO_AP_CANARY1_PIN_677	GPIO_AP_CANARY1_PIN_677	MAKE_BASE=TRUE	
5 3	SPI0_AOP_FROM_IMU_R1_MISO	SPI0_AOP_FROM_IMU_R1_MISO	MAKE_BASE=TRUE	
5 3	PP_STROBE_DRIVER_COOL_LED_1	PP_STROBE_DRIVER_COOL_LED_1	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	MAKE_BASE=TRUE	
5 3	PP_STROBE_DRIVER_COOL_LED_2	PP_STROBE_DRIVER_COOL_LED_2	MAKE_BASE=TRUE	
5 3	GPIO_AP_CANARY1_PIN_683	GPIO_AP_CANARY1_PIN_683	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	SPI0_AOP_TO_IMU_R1_MOSI	SPI0_AOP_TO_IMU_R1_MOSI	MAKE_BASE=TRUE	
5 3	PP_STROBE_DRIVER_WARM_LED_1	PP_STROBE_DRIVER_WARM_LED_1	MAKE_BASE=TRUE	
5 3	GPIO_AP_CANARY1_PIN_689	GPIO_AP_CANARY1_PIN_689	MAKE_BASE=TRUE	
5 3	SPI0_AOP_TO_IMU_R1_SCLK	SPI0_AOP_TO_IMU_R1_SCLK	MAKE_BASE=TRUE	
5 3	PP_STROBE_DRIVER_WARM_LED_2	PP_STROBE_DRIVER_WARM_LED_2	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GPIO_AP_CANARY1_PIN_695	GPIO_AP_CANARY1_PIN_695	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GPIO_AP_CANARY6_PIN_708	GPIO_AP_CANARY6_PIN_708	MAKE_BASE=TRUE	
5 3	GND_OUTER_NORTH	GND_OUTER_NORTH	MAKE_BASE=TRUE	9
5 3	GND_NORTHEAST	GND_NORTHEAST	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GPIO_AP_CANARY6_PIN_713	GPIO_AP_CANARY6_PIN_713	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_NORTHEAST	GND_NORTHEAST	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GPIO_AP_CANARY6_PIN_717	GPIO_AP_CANARY6_PIN_717	MAKE_BASE=TRUE	
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_NORTHEAST	GND_NORTHEAST	MAKE_BASE=TRUE	9
5 3	GPIO_AP_CANARY6_PIN_720	GPIO_AP_CANARY6_PIN_720	MAKE_BASE=TRUE	
5 3	GPIO_AP_CANARY6_PIN_721	GPIO_AP_CANARY6_PIN_721	MAKE_BASE=TRUE	
5 3	GND_NORTHEAST	GND_NORTHEAST	MAKE_BASE=TRUE	9
5 3	GND_NORTHEAST	GND_NORTHEAST	MAKE_BASE=TRUE	9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_INNER_NORTHEAST	GND_INNER_NORTHEAST	MAKE_BASE=TRUE	6 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9
5 3	GND_INNER_NORTHWEST	GND_INNER_NORTHWEST	MAKE_BASE=TRUE	8 9

		ZT1
		3.2R2.2-NSP
9	GND_NORTHWEST	1
		ZT2
		3.2R2.2-NSP
9	GND_NORTHEAST	1
		ZT3
		3.2R2.2-NSP
7	GND_SOUTHWEST	1

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