1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D54 MLB TOP

CRB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

LAST_MODIFICATION=Wed Jul 1 16:52:56 2020

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4	4	CONSTRAINTS: Power	temp	07/01/2019
5	5	CONSTRAINTS: Misc.	temp	07/01/2019
6	6	CONSTRAINTS: 50-Ohm		07/01/2019
7	7	SYSTEM: Bootstrapping 主板版本配置		
8	8	SYSTEM: Mechanical 主板连接点页面		
9	10	SOC: NAND + USB & Misc		
10	11	SOC: PCIE CPU的PCIE模块		
11	12	SOC: ISP CPU的相机显示模块		
12	13	SOC: Display CPU的显示模块		
13	14	SOC: Serial		
14	15	SOC: GPIO CPU的可编程脚位		
15	16	SOC: AOP & SMC & NUB		
16	17	SOC: Ocelot		
17	18	SOC: Power (CPU/GPU & SRAM & SOC)		
18	19	SOC: Power (Fixed & 1V2)		
19	20	SOC: Power (DDR & AOP/AVE/ISP/USB)		
20	21	SOC: Power (GND)		
21	23	SOC: Aliases: I2C AP/ISP		
22	24	SOC: Aliases: I2C AOP/SMC		
23	25	SOC: Aliases: GPIOs		
24	26	SOC: Aliases: Misc		
25	27	SOC: Aliases: FF-Specific		
26	29	NAND		
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28	33	SYS PWR: PMU: Bucks (1/5)		
29	34	SYS PWR: PMU: Bucks (2/5)		
30	35	SYS PWR: PMU: LDOs (3/5)		
31	36	SYS PWR: PMU: GPIO (4/5)		
32	37	SYS PWR: PMU: Misc (5/5)		
33	38	SYS PWR: PMU: Aliases: GPIO		
34	39	SYS PWR: PMU: Aliases: Misc.		
35	40	SYS PWR: Charger		
36	41	SYS PWR: Charger/Boost: Aliases	D52_AP_MASTER_0.175.0	
37	42	SYS PWR: Boost		
38	44	SYS PWR: Wireless Charger		
39	45	SYS PWR: Wireless Charger: Level Shifters		
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41	47	SYS PWR: Wireless Charger: Aliases		
42	49	SYS PWR: NTCs (Top)		
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44	53	CAMERA: PMU 1: Power (1/2)		
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46	55	CAMERA: PMU 1: Aliases	0.143.0	05/14/2019
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51	62	CAMERA: Actuator Supply (Alex)		
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53	65	CAMERA: Strobe Driver		
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56	73	SENSORS: Accel / Gyro		
57	74	SENSORS: Jarvis (Top)		
58	78	AUDIO: Codec: Analog (1/2)		
59	79	AUDIO: Codec: Power & I/O (2/2)		
60	80	AUDIO: Bot Speaker Amp		
61	81	AUDIO: Top Speaker Amp		
62	82	AUDIO: Aliases	0.143.0	05/14/2019
63	83	HAPTIC: Haptic Amp		
64	84	HAPTIC: Sakonnet		
65	90	TOP MODULE: Touch Processor		
66	91	TOP MODULE: Display Power		
67	93	LIGHTNING: Lightning Controller		
68	94	LIGHTNING: USB-PD		
69	95	LIGHTNING: Accessory Buck		
70	96	LIGHTNING: eUSB		
71	97	LIGHTNING: Aliases		
72	99	LVL SHIFT: Misc Nets		
73	100	B2B: Battery	0.99.0	06/20/2019
74	101	B2B: Cyclone	0.99.0	06/20/2019
75	102	B2B: Camera Wide	0.99.0	04/03/2019
76	105	B2B: Camera Superflex	0.99.0	04/03/2019
77	106	B2B: Jasper	0.99.0	04/03/2019
78	107	B2B: FCAM	0.99.0	04/03/2019
79	108	B2B: Juliet	0.99.0	04/03/2019
80	109	B2B: Romeo	0.99.0	04/03/2019
81	110	B2B: Sensor		
82	111	B2B: Strobe	0.99.0	04/03/2019
83	112	B2B: Dock		
84	113	B2B: Dock (Cont)		
85	117	B2B: Display/Touch Combo (1/2)	0.99.0	04/03/2019
86	118	B2B: Display/Touch Combo (2/2)	0.99.0	04/03/2019
87	120	B2B: UAT1	D53_mlb_ice_0.19.0	02/01/2019
88	121	B2B: UAT2		
89	122	B2B: LAT		
90	123	B2B: SIM		
91	126	TESTING: Test Points	D52_AP_MASTER_0.199.0	
92	128	TESTING: Probe Points	D52_AP_MASTER_0.199.0	
93	130	INTERPOSER: Symbol (1/2)		
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97	134	INTERPOSER: Aliases (3/4)		
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99	138	HIERARCHIES	D53_mlb_ice_0.19.0	02/01/2019
100	1	FRONT PAGE		
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102	3	FILTERS MATCHING		
103	1	FRONT PAGE		
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105	20	LB PAD		08/01/2019
106	22	UHB LAT PAD		08/01/2019
107	30	COUPLER LOWER		08/01/2019
108	35	LOWER ANTENNA FEEDS_ANT3		08/01/2019
109	36	LOWER ANTENNA FEEDS_ANT7		08/01/2019
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112	1	NFC: TABLE OF CONTENTS		
113	74	NFC_F		
114	75	NFC_P_CP		
115	1	TABLE OF CONTENTS		05/08/2018
116	4	5G rFEM (UAT)	D52_WIFI_MASTER_0.17.0	
117	5	5G rFEM (LAT)	D52_WIFI_MASTER_0.17.0	

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-08572	MPYK	CRITICAL	EEEE:08572
825-7691	1	EEEE FOR 639-10112	NY8W	CRITICAL	EEEE:10112
825-7691	1	EEEE FOR 639-10113	NY9G	CRITICAL	EEEE:10113
825-7691	1	EEEE FOR 639-10115	NY9Y	CRITICAL	EEEE:10115
825-7691	1	EEEE FOR 639-10116	NYC9	CRITICAL	EEEE:10116
825-7691	1	EEEE FOR 639-10117	NYCN	CRITICAL	EEEE:10117

APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05170	1	SCH,MLB,TOP,D54	SCH	CRITICAL	?
820-01940	1	PCB,MLB,TOP,D54	PCB	CRITICAL	?

Sub-designs

Hierarchies

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/ SOFT	SYNC_DATE/TIME	FORCE SUBDESIGN
D52	HIER_ARROW	0.49.0	S	2020_06_30_13:39:10	N
D54	HIER_RADIO_MAV_TOP	3.25.0	S	2020_06_30_13:38:18	N
D54	HIER_NFC_TOP	0.19.0	S	2020_06_30_13:40:07	N
D54	HIER_WIFI_TOP	0.15.0	S	2020_06_30_13:37:33	N

Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	AP_MASTER	2,7,10-21,23-26,28,31,33-40,42,44-47,49,53-54,56-57,62,64-65,70-71,73-74,78-81,83-84,90-91,93-97,99	3.91.0	S	2020_07_01_16:41:16

Packaging Options

PACK_OPTIONS TO INCLUDE IN NETLIST
D54

TABLE OF CONTENTS

DRAWING TITLE: SCH,MLB,TOP,D54

DRAWING NUMBER: 051-05170 SIZE: D
REVISION: 10.0.0
BRANCH: crb-1
PAGE: 1 OF 138
SHEET: 1 OF 117

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Multi-Vendor Criticals

Capacitors

In descending order of value, then package size

CRITICAL PART#	COMMENT
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
132S0663	CAP,CER,X5R,1UF,10%,25V,0402
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
132S00008	CAP,CER,0.1UF,10%,50V,X7R,0402
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S0664	CAP,CER,0.047UF,10%,25V,X5R,0201
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S00093	CAP,X5R,0.022UF,20%,6.3V,01005
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S0396	CAP,CER,X5R,1000PF,10%,10V,01005
132S0296	CAP,CER,X5R,1000PF,10%,6.3V,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
131S0883	CAP,CER,NP0/C0G,220PF,2%,50V,0201
131S00170	CAP,CER,C0G,220PF,5%,25V,01005
131S00053	CAP,CER,C0G,220PF,5%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
131S0307	CAP,CER,NP0/C0G,100PF,5%,16V,01005

Capacitors (cont'd)

CRITICAL PART#	COMMENT
131S00303	CAP,CER,NPO/C0G,100PF,5%,16V,01005
131S00323	CAP,CER,NPO/C0G,56PF,5%,25V,01005
131S0643	CAP,CER,NP0/C0G,56PF,5%,25V,01005
131S0216	CAP,CER,NP0/C0G,47PF,5%,16V,01005
131S0804	CAP,CER,27PF,5%,C0G,25V,0201
131S0223	CAP,CER,NP0/C0G,27PF,5%,16V,01005
131S0215	CAP,CER,NPO/C0G,22PF,5%,16V,01005
131S0225	CAP,CER,NP0/C0G,15PF,5%,16V,01005
131S0220	CAP,CER,NP0/C0G,12PF,5%,16V,01005
131S00353	CAP,CER,NPO/C0G,10PF,5%,16V,01005

Ferrites

CRITICAL PART#	COMMENT
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605

Resistors

CRITICAL PART#	COMMENT
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
117S0055	RES,MF,1/20W,2M OHM,5,0201,SMD

Misc.

CRITICAL PART#	COMMENT
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005

2020 MLCCs

16uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00316	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402
138S00314	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402
138S00315	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402

Primary: Murata
Taiyo
Kyocera
Samsung

11uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00318	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T
138S00319	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T
138S00320	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T

Primary: Murata
Kyocera
Samsung
Taiyo

2.7uF, 0201, 6.3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00326	138S00325	0040D_ID:0S2A0040D_ID:064	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201
138S00327	138S00325	?	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201

Primary: Murata
Kyocera (61184814)
Samsung

2.7uF, 0201, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00324	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201
138S00322	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201
138S00323	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201

Primary: Murata
Taiyo
Kyocera
Samsung

MAV20 PDN Single-source

0.22uF, 01005

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Kyocera

(C70,C71,C72,C73,C74,C77,C78,C79,C81,C82,C84,C85,C86,C87,C88,C89,C90,C91,C92,C93,C94,C95,C96,C97,C98,C99,C100,C101,C102,C103,C104,C105,C106,C107,C108,C109,C110,C111,C112,C113,C114,C115,C116,C117,C118,C119,C120,C121,C122,C123,C124,C125,C126,C127,C128,C129,C130,C131,C132,C133,C134,C135,C136,C137,C138,C139,C140,C141,C142,C143,C144,C145,C146,C147,C148,C149,C150,C151,C152,C153,C154,C155,C156,C157,C158,C159,C160,C161,C162,C163,C164,C165,C166,C167,C168,C169,C170,C171,C172,C173,C174,C175,C176,C177,C178,C179,C180,C181,C182,C183,C184,C185,C186,C187,C188,C189,C190,C191,C192,C193,C194,C195,C196,C197,C198,C199,C200,C201,C202,C203,C204,C205,C206,C207,C208,C209,C210,C211,C212,C213,C214,C215,C216,C217,C218,C219,C220,C221,C222,C223,C224,C225,C226,C227,C228,C229,C230,C231,C232,C233,C234,C235,C236,C237,C238,C239,C240,C241,C242,C243,C244,C245,C246,C247,C248,C249,C250,C251,C252,C253,C254,C255,C256,C257,C258,C259,C260,C261,C262,C263,C264,C265,C266,C267,C268,C269,C270,C271,C272,C273,C274,C275,C276,C277,C278,C279,C280,C281,C282,C283,C284,C285,C286,C287,C288,C289,C290,C291,C292,C293,C294,C295,C296,C297,C298,C299,C300,C301,C302,C303,C304,C305,C306,C307,C308,C309,C310,C311,C312,C313,C314,C315,C316,C317,C318,C319,C320,C321,C322,C323,C324,C325,C326,C327,C328,C329,C330,C331,C332,C333,C334,C335,C336,C337,C338,C339,C340,C341,C342,C343,C344,C345,C346,C347,C348,C349,C350,C351,C352,C353,C354,C355,C356,C357,C358,C359,C360,C361,C362,C363,C364,C365,C366,C367,C368,C369,C370,C371,C372,C373,C374,C375,C376,C377,C378,C379,C380,C381,C382,C383,C384,C385,C386,C387,C388,C389,C390,C391,C392,C393,C394,C395,C396,C397,C398,C399,C400,C401,C402,C403,C404,C405,C406,C407,C408,C409,C410,C411,C412,C413,C414,C415,C416,C417,C418,C419,C420,C421,C422,C423,C424,C425,C426,C427,C428,C429,C430,C431,C432,C433,C434,C435,C436,C437,C438,C439,C440,C441,C442,C443,C444,C445,C446,C447,C448,C449,C450,C451,C452,C453,C454,C455,C456,C457,C458,C459,C460,C461,C462,C463,C464,C465,C466,C467,C468,C469,C470,C471,C472,C473,C474,C475,C476,C477,C478,C479,C480,C481,C482,C483,C484,C485,C486,C487,C488,C489,C490,C491,C492,C493,C494,C495,C496,C497,C498,C499,C500,C501,C502,C503,C504,C505,C506,C507,C508,C509,C510,C511,C512,C513,C514,C515,C516,C517,C518,C519,C520,C521,C522,C523,C524,C525,C526,C527,C528,C529,C530,C531,C532,C533,C534,C535,C536,C537,C538,C539,C540,C541,C542,C543,C544,C545,C546,C547,C548,C549,C550,C551,C552,C553,C554,C555,C556,C557,C558,C559,C560,C561,C562,C563,C564,C565,C566,C567,C568,C569,C570,C571,C572,C573,C574,C575,C576,C577,C578,C579,C580,C581,C582,C583,C584,C585,C586,C587,C588,C589,C590,C591,C592,C593,C594,C595,C596,C597,C598,C599,C600,C601,C602,C603,C604,C605,C606,C607,C608,C609,C610,C611,C612,C613,C614,C615,C616,C617,C618,C619,C620,C621,C622,C623,C624,C625,C626,C627,C628,C629,C630,C631,C632,C633,C634,C635,C636,C637,C638,C639,C640,C641,C642,C643,C644,C645,C646,C647,C648,C649,C650,C651,C652,C653,C654,C655,C656,C657,C658,C659,C660,C661,C662,C663,C664,C665,C666,C667,C668,C669,C670,C671,C672,C673,C674,C675,C676,C677,C678,C679,C680,C681,C682,C683,C684,C685,C686,C687,C688,C689,C690,C691,C692,C693,C694,C695,C696,C697,C698,C699,C700,C701,C702,C703,C704,C705,C706,C707,C708,C709,C710,C711,C712,C713,C714,C715,C716,C717,C718,C719,C720,C721,C722,C723,C724,C725,C726,C727,C728,C729,C730,C731,C732,C733,C734,C735,C736,C737,C738,C739,C740,C741,C742,C743,C744,C745,C746,C747,C748,C749,C750,C751,C752,C753,C754,C755,C756,C757,C758,C759,C760,C761,C762,C763,C764,C765,C766,C767,C768,C769,C770,C771,C772,C773,C774,C775,C776,C777,C778,C779,C780,C781,C782,C783,C784,C785,C786,C787,C788,C789,C790,C791,C792,C793,C794,C795,C796,C797,C798,C799,C800,C801,C802,C803,C804,C805,C806,C807,C808,C809,C810,C811,C812,C813,C814,C815,C816,C817,C818,C819,C820,C821,C822,C823,C824,C825,C826,C827,C828,C829,C830,C831,C832,C833,C834,C835,C836,C837,C838,C839,C840,C841,C842,C843,C844,C845,C846,C847,C848,C849,C850,C851,C852,C853,C854,C855,C856,C857,C858,C859,C860,C861,C862,C863,C864,C865,C866,C867,C868,C869,C870,C871,C872,C873,C874,C875,C876,C877,C878,C879,C880,C881,C882,C883,C884,C885,C886,C887,C888,C889,C890,C891,C892,C893,C894,C895,C896,C897,C898,C899,C900,C901,C902,C903,C904,C905,C906,C907,C908,C909,C910,C911,C912,C913,C914,C915,C916,C917,C918,C919,C920,C921,C922,C923,C924,C925,C926,C927,C928,C929,C930,C931,C932,C933,C934,C935,C936,C937,C938,C939,C940,C941,C942,C943,C944,C945,C946,C947,C948,C949,C950,C951,C952,C953,C954,C955,C956,C957,C958,C959,C960,C961,C962,C963,C964,C965,C966,C967,C968,C969,C970,C971,C972,C973,C974,C975,C976,C977,C978,C979,C980,C981,C982,C983,C984,C985,C986,C987,C988,C989,C990,C991,C992,C993,C994,C995,C996,C997,C998,C999,C1000,C1001,C1002,C1003,C1004,C1005,C1006,C1007,C1008,C1009,C1010,C1011,C1012,C1013,C1014,C1015,C1016,C1017,C1018,C1019,C1020,C1021,C1022,C1023,C1024,C1025,C1026,C1027,C1028,C1029,C1030,C1031,C1032,C1033,C1034,C1035,C1036,C1037,C1038,C1039,C1040,C1041,C1042,C1043,C1044,C1045,C1046,C1047,C1048,C1049,C1050,C1051,C1052,C1053,C1054,C1055,C1056,C1057,C1058,C1059,C1060,C1061,C1062,C1063,C1064,C1065,C1066,C1067,C1068,C1069,C1070,C1071,C1072,C1073,C1074,C1075,C1076,C1077,C1078,C1079,C1080,C1081,C1082,C1083,C1084,C1085,C1086,C1087,C1088,C1089,C1090,C1091,C1092,C1093,C1094,C1095,C1096,C1097,C1098,C1099,C1100,C1101,C1102,C1103,C1104,C1105,C1106,C1107,C1108,C1109,C1110,C1111,C1112,C1113,C1114,C1115,C1116,C1117,C1118,C1119,C1120,C1121,C1122,C1123,C1124,C1125,C1126,C1127,C1128,C1129,C1130,C1131,C1132,C1133,C1134,C1135,C1136,C1137,C1138,C1139,C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149,C1150,C1151,C1152,C1153,C1154,C1155,C1156,C1157,C1158,C1159,C1160,C1161,C1162,C1163,C1164,C1165,C1166,C1167,C1168,C1169,C1170,C1171,C1172,C1173,C1174,C1175,C1176,C1177,C1178,C1179,C1180,C1181,C1182,C1183,C1184,C1185,C1186,C1187,C1188,C1189,C1190,C1191,C1192,C1193,C1194,C1195,C1196,C1197,C1198,C1199,C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209,C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219,C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229,C1230,C1231,C1232,C1233,C1234,C1235,C1236,C1237,C1238,C1239,C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249,C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259,C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267,C1268,C1269,C1270,C1271,C1272,C1273,C1274,C1275,C1276,C1277,C1278,C1279,C1280,C1281,C1282,C1283,C1284,C1285,C1286,C1287,C1288,C1289,C1290,C1291,C1292,C1293,C1294,C1295,C1296,C1297,C1298,C1299,C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309,C1310,C1311,C1312,C1313,C1314,C1315,C1316,C1317,C1318,C1319,C1320,C1321,C1322,C1323,C1324,C1325,C1326,C1327,C1328,C1329,C1330,C1331,C1332,C1333,C1334,C1335,C1336,C1337,C1338,C1339,C1340,C1341,C1342,C1343,C1344,C1345,C1346,C1347,C1348,C1349,C1350,C1351,C1352,C1353,C1354,C1355,C1356,C1357,C1358,C1359,C1360,C1361,C1362,C1363,C1364,C1365,C1366,C1367,C1368,C1369,C1370,C1371,C1372,C1373,C1374,C1375,C1376,C1377,C1378,C1379,C1380,C1381,C1382,C1383,C1384,C1385,C1386,C1387,C1388,C1389,C1390,C1391,C1392,C1393,C1394,C1395,C1396,C1397,C1398,C1399,C1400,C1401,C1402,C1403,C1404,C1405,C1406,C1407,C1408,C1409,C1410,C1411,C1412,C1413,C1414,C1415,C1416,C1417,C1418,C1419,C1420,C1421,C1422,C1423,C1424,C1425,C1426,C1427,C1428,C1429,C1430,C1431,C1432,C1433,C1434,C1435,C1436,C1437,C1438,C1439,C1440,C1441,C1442,C1443,C1444,C1445,C1446,C1447,C1448,C1449,C1450,C1451,C1452,C1453,C1454,C1455,C1456,C1457,C1458,C1459,C1460,C1461,C1462,C1463,C1464,C1465,C1466,C1467,C1468,C1469,C1470,C1471,C1472,C1473,C1474,C1475,C1476,C1477,C1478,C1479,C1480,C1481,C1482,C1483,C1484,C1485,C1486,C1487,C1488,C1489,C1490,C1491,C1492,C1493,C1494,C1495,C1496,C1497,C1498,C1499,C1500,C1501,C1502,C1503,C1504,C1505,C1506,C1507,C1508,C1509,C1510,C1511,C1512,C1513,C1514,C1515,C1516,C1517,C1518,C1519,C1520,C1521,C1522,C1523,C1524,C1525,C1526,C1527,C1528,C1529,C1530,C1531,C1532,C1533,C1534,C1535,C1536,C1537,C1538,C1539,C1540,C1541,C1542,C1543,C1544,C1545,C1546,C1547,C1548,C1549,C1550,C1551,C1552,C1553,C1554,C1555,C1556,C1557,C1558,C1559,C1560,C1561,C1562,C1563,C1564,C1565,C1566,C1567,C1568,C1569,C1570,C1571,C1572,C1573,C1574,C1575,C1576,C1577,C1578,C1579,C1580,C1581,C1582,C1583,C1584,C1585,C1586,C1587,C1588,C1589,C1590,C1591,C1592,C1593,C1594,C1595,C1596,C1597,C1598,C1599,C1600,C1601,C1602,C1603,C1604,C1605,C1606,C1607,C1608,C1609,C1610,C1611,C1612,C1613,C1614,C1615,C1616,C1617,C1618,C1619,C1620,C1621,C1622,C1623,C1624,C1625,C1626,C1627,C1628,C1629,C1630,C1631,C1632,C1633,C1634,C1635,C1636,C1637,C1638,C1639,C1640,C1641,C1642,C1643,C1644,C1645,C1646,C1647,C1648,C1649,C1650,C1651,C1652,C1653,C1654,C1655,C1656,C1657,C1658,C1659,C1660,C1661,C1662,C1663,C1664,C1665,C1666,C1667,C1668,C1669,C1670,C1671,C1672,C1673,C1674,C1675,C1676,C1677,C1678,C1679,C1680,C1681,C1682,C1683,C1684,C1685,C1686,C1687,C1688,C1689,C1690,C1691,C1692,C1693,C1694,C1695,C1696,C1697,C1698,C1699,C1700,C1701,C1702,C1703,C1704,C1705,C1706,C1707,C1708,C1709,C1710,C1711,C1712,C1713,C1714,C1715,C1716,C1717,C1718,C1719,C1720,C1721,C1722,C1723,C1724,C1725,C1726,C1727,C1728,C1729,C1730,C1731,C1732,C1733,C1734,C1735,C1736,C1737,C1738,C1739,C1740,C1741,C1742,C1743,C1744,C1745,C1746,C1747,C1748,C1749,C1750,C1751,C1752,C1753,C1754,C1755,C1756,C1757,C1758,C1759,C1760,C1761,C1762,C1763,C1764,C1765,C1766,C1767,C1768,C1769,C1770,C1771,C1772,C1773,C1774,C1775,C1776,C1777,C1778,C1779,C1780,C1781,C1782,C1783,C1784,C1785,C1786,C1787,C1788,C1789,C1790,C1791,C1792,C1793,C1794,C1795,C1796,C1797,C1798,C1799,C1800,C1801,C1802,C1803,C1804,C1805,C1806,C1807,C1808,C1809,C1810,C1811,C1812,C1813,C1814,C1815,C1816,C1817,C1818,C1819,C1820,C1821,C1822,C1823,C1824,C1825,C1826,C1827,C1828,C1829,C1830,C1831,C1832,C1833,C1834,C1835,C1836,C1837,C1838,C1839,C1840,C1841,C1842,C1843,C1844,C1845,C1846,C1847,C1848,C1849,C1850,C1851,C1852,C1853,C1854,C1855,C1856,C1857,C1858,C1859,C1860,C1861,C1862,C1863,C1864,C1865,C1866,C1867,C1868,C1869,C1870,C1871,C1872,C1873,C1874,C1875,C1876,C1877,C1878,C1879,C1880,C1881,C1882,C1883,C1884,C1885,C1886,C1887,C1888,C1889,C1890,C1891,C1892,C1893,C1894,C1895,C1896,C1897,C1898,C1899,C1900,C1901,C1902,C1903,C1904,C1905,C1906,C1907,C1908,C1909,C1910,C1911,C1912,C1913,C1914,C1915,C1916,C1917,C1918,C1919,C1920,C1921,C1922,C1923,C1924,C1925,C1926,C1927,C1928,C1929,C1930,C1931,C1932,C1933,C1934,C1935,C1936,C1937,C1938,C1939,C1940,C1941,C1942,C1943,C1944,C1945,C1946,C1947,C1948,C1949,C1950,C1951,C1952,C1953,C1954,C1955,C1956,C1957,C1958,C1959,C1960,C1961,C1962,C1963,C1964,C1965,C1966,C1967,C1968,C1969,C1970,C1971,C1972,C1973,C1974,C1975,C1976,C1977,C1978,C1979,C1980,C1981,C1982,C1983,C1984,C1985,C1986,C1987,C1988,C1989,C1990,C1991,C1992,C1993,C1994,C1995,C1996,C1997,C1998,C1999,C2000,C2001,C2002,C2003,C2004,C2005,C2006,C2007,C2008,C2009,C2010,C2011,C2012,C2013,C2014,C2015,C2016,C2017,C2018,C2019,C2020,C2021,C2022,C2023,C2024,C2025,C2026,C2027,C2028,C2029,C2030,C2031,C2032,C2033,C2034,C2035,C2036,C2037,C2038,C2039,C2040,C2041,C2042,C2043,C2044,C2045,C2046,C2047,C2048,C2049,C2050,C2051,C2052,C2053,C2054,C2055,C2056,C2057,C2058,C2059,C2060,C2061,C2062,C2063,C2064,C2065,C2066,C2067,C2068,C2069,C2070,C2071,C2072,C2073,C2074,C2075,C2076,C2077,C2078,C2079,C2080,C2081,C2082,C2083,C2084,C2085,C2086,C2087,C2088,C2089,C2090,C2091,C2092,C2093,C2094,C2095,C2096,C2097,C2098,C2099,C2100,C2101,C2102,C2103,C2104,C2105,C2106,C2107,C2108,C2109,C2110,C2111,C2112,C2113,C2114,C2115,C2116,C2117,C2118,C2119,C2120,C2121,C2122,C2123,C2124,C2125,C2126,C2127,C2128,C2129,C2130,C2131,C2132,C2133,C2134,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2142,C2143,C2144,C2145,C2146,C2147,C2148,C2149,C2150,C2151,C2152,C2153,C2154,C2155,C2156,C2157,C2158,C2159,C2160,C2161,C2162,C2163,C2164,C2165,C2166,C2167,C2168,C2169,C2170,C2171,C2172,C2173,C2174,C2175,C2176,C2177,C2178,C2179,C2180,C2181,C2182,C2183,C2184,C2185,C2186,C2187,C2188,C2189,C2190,C2191,C2192,C2193,C2194,C2195,C2196,C2197,C2198,C2199,C2200,C2201,C2202,C2203,C2204,C2205,C2206,C2207,C2208,C2209,C2210,C2211,C2212,C2213,C2214,C2215,C2216,C2217,C2218,C2219,C2220,C2221,C2222,C2223,C2224,C2225,C2226,C2227,C2228,C2229,C2230,C2231,C2232,C2233,C2234,C2235,C2236,C2237,C2238,C2239,C2240,C2241,C2242,C2243,C2244,C2245,C2246,C2247,C2248,C2249,C2250,C2251,C2252,C2253,C2254,C2255,C2256,C2257,C2258,C2259,C2260,C2261,C2262,C2263,C2264,C2265,C2266,C2267,C2268,C2269,C2270,C2271,C2272,C2273,C2274,C2275,C2276,C2277,C2278,C2279,C2280,C2281,C2282,C2283,C2284,C2285,C2286,C2287,C2288,C2289,C2290,C2291,C2292,C2293,C2294,C2295,C2296,C2297,C2298,C2299,C2300,C2301,C2302,C2303,C2304,C2305,C2306,C2307,C2308,C2309,C2310,C2311,C2312,C2313,C2314,C2315,C2316,C2317,C2318,C2319,C2320,C2321,C2322,C2323,C2324,C2325,C2326,C2327,C2328,C2329,C2330,C2331,C2332,C2333,C2334,C2335,C2336,C2337,C2338,C2339,C2340,C2341,C2342,C2343,C2344,C2345,C2346,C2347,C2348,C2349,C2350,C2351,C2352,C2353,C2354,C2355,C2356,C2357,C2358,C2359,C2360,C2361,C2362,C2363,C2364,C2365,C2366,C2367,C2368,C2369,C2370,C2371,C2372,C2373,C2374,C2375,C2376,C2377,C2378,C2379,C2380,C2381,C2382,C2383,C2384,C2385,C2386,C2387,C2388,C2389,C2390,C2391,C2392,C2393,C2394,C2395,C2396,C2397,C2398,C2399,C2400,C2401,C2402,C2403,C2404,C2405,C2406,C2407,C2408,C2409,C2410,C2411,C2412,C2413,C2414,C2415,C2416,C2417,C2418,C2419,C2420,C2421,C2422,C2423,C2424,C2425,C2426,C2427,C2428,C2429,C2430,C2431,C2432,C2433,C2434,C2435,C2436,C2437,C2438,C2439,C2440,C2441,C2442,C2443,C2444,C2445,C2446,C2447,C2448,C2449,C2450,C2451,C2452,C2453,C2454,C2455,C2456,C2457,C2458,C2459,C2460,C2461,C2462,C2463,C2464,C2465,C2466,C2467,C2468,C2469,C2470,C2471,C2472,C2473,C2474,C2475,C2476,C2477,C2478,C2479,C2480,C2481,C2482,C2483,C2484,C2485,C2486,C2487,C2488,C2489,C2490,C2491,C2492,C2493,C2494,C2495,C2496,C2497,C2498,C2499,C2500,C2501,C2502,C2503,C2504,C2505,C2506,C2507,C2508,C2509,C2510,C2511,C2512,C2513,C2514,C2515,C2516,C2517,C2518,C2519,C2520,C2521,C2522,C2523,C2524,C2525,C2526,C2527,C2528,C2529,C2530,C2531,C2532,C2533,C2534,C2535,C2536,C2537,C2538,C2539,C2540,C2541,C2542,C2543,C2544,C2545,C2546,C2547,C2548,C2549,C2550,C2551,C2552,C2553,C2554,C2555,C2556,C2557,C2558,C2559,C2560,C2561,C2562,C2563,C2564,C2565,C2566,C2567,C2568,C2569,C2570,C2571,C2572,C2573,C2574,C2575,C2576,C2577,C2578,C2579,C2580,C2581,C2582,C2583,C2584,C2585,C2586,C2587,C2588,C2589,C2590,C2591,C2592,C2593,C2594,C2595,C2596,C2597,C2598,C2599,C2600,C2601,C2602,C2603,C2604,C2605,C2606,C2607,C2608,C2609,C2610,C2611,C2612,C2613,C2614,C2615,C2616,C2617,C2618,C2619,C2620,C2621,C2622,C2623,C2624,C2625,C2626,C2627,C2628,C2629,C2630,C2631,C2632,C2633,C2634,C2635,C2636,C2637,C2638,C2639,C2640,C2641,C2642,C2643,C2644,C2645,C2646,C2647,C2648,C2649,C2650,C2651,C2652,C2653,C2654,C2655,C2656,C2657,C2658,C2659,C2660,C2661,C2662,C2663,C2664,C2665,C2666,C2667,C2668,C2669,C2670,C2671,C2672,C2673,C2674,C2675,C2676,C2677,C2678,C2679,C2680,C2681,C2682,C2683,C2684,C2685,C2686,C2687,C2688,C2689,C2690,C2691,C2692,C2693,C2694,C2695,C2696,C2697,C2698,C2699,C2700,C2701,C2702,C2703,C2704,C2705,C2706,C2707,C2708,C2709,C2710,C2711,C2712,C2713,C2714,C2715,C2716,C2717,C2718,C2719,C2720,C2721,C2722,C2723,C2724,C2725,C2726,C2727,C2728,C2729,C2730,C2731,C2732,C2733,C2734,C2735,C2736,C2737,C2738,C2739,C2740,C2741,C2742,C2743,C2744,C2745,C2746,C2747,C2748,C2749,C2750,C2751,C2752,C2753,C2754,C2755,C2756,C2757,C2758,C2759,C2760,C2761,C2762,C2763,C2764,C2765,C2766,C2767,C2768,C2769,C2770,C2771,C2772,C2773,C2774,C2775,C2776,C2777,C2778,C2779,C2780,C2781,C2782,C2783,C2784,C2785,C2786,C2787,C2788,C2789,C2790,C2791,C2792,C2793,C2794,C2795,C2796,C2797,C2798,C2799,C2800,C2801,C2802,C2803,C2804,C2805,C2806,C2807,C2808,C2809,C2810,C2811,C2812,C2813,C2814,C2815,C2816,C2817,C2818,C2819,C2820,C2821,C2822,C2823,C2824,C2825,C2826,C2827,C2828,C2829,C2830,C2831,C2832,C2833,C2834,C2835,C2836,C2837,C2838,C2839,C2840,C2841,C2842,C2843,C2844,C2845,C2846,C2847,C2848,C2849,C2850,C2851,C2852,C2853,C2854,C2855,C2856,C2857,C2858,C2859,C2860,C2861,C2862,C2863,C2864,C2865,C2866,C2867,C2868,C2869,C2870,C2871,C2872,C2873,C2874,C2875,C2876,C2877,C2878,C2879,C2880,C2881,C2882,C2883,C2884,C2885,C2886,C2887,C2888,C2889,C2890,C2891,C2892,C2893,C2894,C2895,C2896,C2897,C2898,C2899,C2900,C2901,C2902,C2903,C2904,C2905,C2906,C2907,C2908,C2909,C2910,C2911,C2912,C2913,C2914,C2915,C2916,C2917,C2918,C2919,C2920,C2921,C2922,C2923,C2924,C2925,C2926,C2927,C2928,C2929,C2930,C2931,C2932,C2933,C2934,C2935,C2936,C2937,C2938,C2939,C2940,C2941,C2942,C2943,C2944,C2945,C2946,C2947,C2948,C2949,C2950,C2951,C2952,C2953,C2954,C2955,C2956,C2957,C2958,C2959,C2960,C2961,C2962,C2963,C2964,C2965,C2966,C2967,C2968,C2969,C2970,C2971,C2972,C2973,C2974,C2975,C2976,C2977,C2978,C2979,C2980,C2981,C2982,C2983,C2984,C2985,C2986,C2987,C2988,C2989,C2990,C2991,C2992,C2993,C2994,C2995,C2996,C2997,C2998,C2999,C3000,C3001,C3002,C3003,C3004,C3005,C3006,C3007,C3008,C3009,C3010,C3011,C3012,C3013,C3014,C3015,C3016,C3017,C3018,C3019,C3020,C3021,C3022,C3023,C3024,C3025,C3026,C3027,C3028,C3029,C3030,C3031,C3032,C3033,C3034,C3035,C3036,C3037,C3038,C3039,C3040,C3041,C3042,C3043,C3044,C3045,C3046,C3047,C3048,C3049,C3050,C3051,C3052,C3053,C3054,C3055,C3056,C3057,C3058,C3059,C3060,C3061,C3062,C3063,C3064,C3065,C3066,C3067,C3068,C3069,C3070,C3071,C3072,C3073,C3074,C3075,C3076,C3077,C3078,C3079,C3080,C3081,C3082,C3083,C3084,C3085,C3086,C3087,C3088,C3089,C3090,C3091,C3092,C3093,C3094,C3095,C3096,C3097,C3098,C3099,C3100,C3101,C3102,C3103,C3104,C3105,C3106,C3107,C3108,C3109,C3110,C3111,C3112,C3113,C3114,C3115,C3116,C3117,C3118,C3119,C3120,C3121,C3122,C3123,C3124,C3125,C3126,C3127,C3128,C3129,C3130,C3131,C3132,C3133,C3134,C3135,C3136,C3137,C3138,C3139,C3140,C3141,C3142,C3143,C3144,C3145,C3146,C3147,C3148,C3149,C3150,C3151,C3152,C3153,C3154,C3155,C3156,C3157,C3158,C3159,C3160,C3161,C3162,C3163,C3164,C3165,C3166,C3167,C3168,C3169,C3170,C3171,C3172,C3173,C3174,C3175,C3176,C3177,C3178,C3179,C3180,C3181,C3182,C3183,C3184,C3185,C3186,C3187,C3188,C3189,C3190,C3191,C3192,C3193,C3194,C3195,C3196,C3197,C3198,C3199,C3200,C3201,C3202,C3203,C3204,C3205,C3206,C3207,C3208,C3209,C3210,C3211,C3212,C3213,C3214,C3215,C3216,C3217,C3218,C3219,C3220,C3221,C3222,C3223,C3224,C3225,C3226,C3227,C3228,C3229,C3230,C3231,C3232,C3233,C3234,C3235,C3236,C3237,C3238,C3239,C3240,C3241,C3242,C3243,C3244,C3245,C3246,C3247,C3248,C3249,C3250,C3251,C3252,C3253,C3254,C3255,C3256,C3257,C3258,C3259,C3260,C3261,C3262,C3263,C3264,C3265,C3266,C3267,C3268,C3269,C3270,C3271,C3272,C3273,C3274,C3275,C3276,C3277,C3278,C3279,C3280,C3281,C3282,C3283,C3284,C3285,C3286,C3287,C3288,C3289,C3290,C3291,C3292,C3293,C3294,C3295,C3296,C3297,C3298,C3299,C3300,C3301,C3302,C3303,C3304,C3305,C3306,C3307,C3308,C3309,C3310,C3311,C3312,C3313,C3314,C3315,C3316,C3317,C3318,C3319,C3320,C3321,C3322,C3323,C3324,C3325,C3326,C3327,C3328,C3329,C3330,C3331,C3332,C3333,C3334,C3335,C3336,C3337,C3338,C3339,C3340,C3341,C3342,C3343,C3344,C3345,C3346,C3347,C3348,C3349,C3350,C3351,C3352,C3353,C3354,C3355,C3356,C3357,C3358,C3359,C3360,C3361,C3362,C3363,C3364,C3365,C3366,C3367,C3368,C3369,C3370,C3371,C3372,C3373,C3374,C3375,C3376,C3377,C3378,C3379,C3380,C3381,C3382,C3383,C3384,C3385,C3386,C3387,C3388,C3389,C3390,C3391,C3392,C3393,C3394,C3395,C3396,C3397,C3398,C3399,C3400,C3401,C3402,C3403,C3404,C3405,C3406,C3407,C3408,C3409,C3410,C3411,C3412,C3413,C3414,C3415,C3416,C3417,C3418,C3419,C3420,C3421,C3422,C3423,C3424,C3425,C3426,C3427,C3428,C3429,C3430,C3431,C3432,C3433,C3434,C3435,C3436,C3437,C3438,C3439,C3440,C3441,C3442,C3443,C3444,C3445,C3446,C3447,C3448,C3449,C3450,C3451,C3452,C3453,C3454,C3455,C3456,C3457,C3458,C3459,C3460,C3461,C3462,C3463,C3464,C3465,C3466,C3467,C3468,C3469,C3470,C3471,C3472,C3473,C3474,C3475,C3476,C3477,C3478,C3479,C3480,C3481,C3482,C3483,C3484,C3485,C3486,C3487,C3488,C3489,C3490,C3491,C3492,C3493,C3494,C3495,C3496,C3497,C3498,C3499,C3500,C3501,C3502,C3503,C3504,C3505,C3506,C3507,C3508,C3509,C3510,C3511,C3512,C3513,C3514,C3515,C3516,C3517,C3518,C3519,C3520,C3521,C3522,C3523,C3524,C3525,C3526,C3527,C3528,C3529,C3530,C3531,C3532,C3533,C3534,C3535,C3536,C3537,C3538,C3539,C3540,C3541,C3542,C3543,C3544,C3545,C3546,C3547,C3548,C3549,C3550,C3551,C3552,C3553,C3554,C3555,C3556,C3557,C3558,C3559,C3560,C3561,C3562,C3563,C3564,C3565,C3566,C3567,C3568,C3569,C3570,C3571,C3572,C3573,C3574,C3575,C3576,C3577,C3578,C3579,C3580,C3581,

90-ohm Diff Pair Constraints

Electrical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	E_LPDP_WIDE	E	DIFF_PAIR	DP:DP_90_LPDP*_WIDE*	Y
	E_LPDP_SWIDE	E	DIFF_PAIR	DP:DP_90_LPDP*_SWIDE*	Y
	E_LPDP_TELE	E	DIFF_PAIR	DP:DP_90_LPDP*_TELE*	Y
	E_LPDP_FCAM	E	DIFF_PAIR	DP:DP_90_LPDP*_FCAM*	Y
	E_LPDP_JASPER	E	DIFF_PAIR	DP:DP_90_LPDP*_JASPER*	Y
MIPI	E_MIPI_DISPLAY	E	DIFF_PAIR_MIPI-D	DP:DP_90_MIPI*DISPLAY*	N
	E_MIPI_IRCAM	E	DIFF_PAIR_MIPI-C	DP:DP_90_MIPI*_IRCAM*	N
PCIE	E_PCIE_NAND	E	DIFF_PAIR	DP:DP_90_PCIE*_NAND*	Y
	E_PCIE_WLAN	E	DIFF_PAIR	DP:DP_90_PCIE*_WLAN*	Y
	E_PCIE_BB	E	DIFF_PAIR	DP:DP_90_PCIE*_BB*	Y
USB	E_KRAKEN_DP	E	DIFF_PAIR	DP:DP_90_KRAKEN*	Y
	E_MIKEYBUS_DP	E	DIFF_PAIR	DP:DP_90_MIKEYBUS*	Y
	E_USB_DP	E	DIFF_PAIR	DP:DP_90_USB*	Y
	E_EUSB_DP	E	DIFF_PAIR	DP:DP_90_EUSB*	Y

Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	90_LPDP_WIDE	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_WIDE*	Y
	90_LPDP_SWIDE	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_SWIDE*	Y
	90_LPDP_TELE	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_TELE*	Y
	90_LPDP_FCAM	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_FCAM*	Y
	90_LPDP_JASPER	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_JASPER*	Y
MIPI-D	90_MIPI_DISPLAY	P	A_90_OHM_DIFF	DP:DP_90_MIPI*DISPLAY*	Y
MIPI-C	90_MIPI_IRCAM	P	A_90_OHM_DIFF	DP:DP_90_MIPI*_IRCAM*	Y
PCIE (Gen4)	90_PCIE_NAND	P	A_90_OHM_DIFF	DP:DP_90_PCIE*_NAND*	Y
	90_PCIE_BB	P	A_90_OHM_DIFF	DP:DP_90_PCIE*_BB*	Y
PCIE (Gen2)	90_PCIE_WLAN	P	A_90_OHM_DIFF	DP:DP_90_PCIE*_WLAN*	Y
USB	90_KRAKEN_DP	P	A_90_OHM_DIFF	DP:DP_90_KRAKEN*	Y
	90_USB_DP	P	A_90_OHM_DIFF	DP:DP_90_USB*	Y
	90_EUSB_DP	P	A_90_OHM_DIFF	DP:DP_90_EUSB*	Y
MIKEYBUS	90_MIKEYBUS_DP	P	A_90_OHM_DIFF	DP:DP_90_MIKEYBUS*	Y

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	90_LPDP_WIDE	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_SWIDE	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_TELE	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_FCAM	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_JASPER	S	A_DIELECTRIC_3X	=	Y
MIPI-D	90_MIPI_DISPLAY	S	A_DIELECTRIC_3X	=	Y
MIPI-C	90_MIPI_IRCAM	S	A_DIELECTRIC_2X	=	Y
PCIE (Gen4)	90_PCIE_NAND	S	A_DIELECTRIC_3X	=	Y
	90_PCIE_BB	S	A_DIELECTRIC_3X	=	Y
PCIE (Gen2)	90_PCIE_WLAN	S	A_DIELECTRIC_3X	=	Y
USB	90_KRAKEN_DP	S	A_DIELECTRIC_3X	=	Y
	90_USB_DP	S	A_DIELECTRIC_3X	=	Y
	90_EUSB_DP	S	A_DIELECTRIC_3X	=	Y
MIKEYBUS	90_MIKEYBUS_DP	S	A_DIELECTRIC_2X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
	CLASS NAME	CLASS NAME	CONSTRAINT SET
LPDP <-> LPDP	90_LPDP_WIDE	90_LPDP_WIDE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_SWIDE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_TELE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_SWIDE	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_TELE	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_TELE	90_LPDP_TELE	A_DIELECTRIC_2X
	90_LPDP_TELE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_TELE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_FCAM	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_FCAM	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_JASPER	90_LPDP_JASPER	A_DIELECTRIC_2X
MIPI-D	90_MIPI_DISPLAY	90_MIPI_DISPLAY	A_DIELECTRIC_2X
PCIE (Gen2)	90_PCIE_WLAN	90_PCIE_WLAN	A_DIELECTRIC_2X
USB	90_KRAKEN_DP	90_KRAKEN_DP	A_DIELECTRIC_2X
	90_KRAKEN_DP	90_USB_DP	A_DIELECTRIC_2X
	90_KRAKEN_DP	90_EUSB_DP	A_DIELECTRIC_2X
	90_USB_DP	90_USB_DP	A_DIELECTRIC_2X
	90_USB_DP	90_EUSB_DP	A_DIELECTRIC_2X
	90_EUSB_DP	90_EUSB_DP	A_DIELECTRIC_2X

Spacing CSet Definitions

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_{N}X Calculate dielectric distance from reference, shortest distance is used unless 'L' is defined	EXAMPLE: 1,2.5,3,4X, 10L 1.5,2,2.5,3,4
A_DIELECTRIC_{N}XO.XV,XVL,X Calculate dielectric distance from hybrid Table and interop, shortest distance is used unless 'L' defined	EXAMPLE: 2.2X,3X,4.5X,5X,6X PLEASE USE HYBRID TABLE
A_DIELECTRIC_{N}XIN_{N}XOUT Calculate dielectric distance from two pairs, shortest distance is used unless 'L' is defined	EXAMPLE: 3"_4.5L,5L ?

Pin Delay Check

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
U1000	SicilyPinDelay.csv
J10800	D54_JulietPinDelay.csv

*Location: /physical/rule/pindelays

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Power Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LX/CX Nodes	PWR_SHAPE_LX	P	PWR_SHAPE	LX*,!LX_CHARGER_BOOT*,!LX_DPMIC*	Y
	PWR_SHAPE_LX_DPMIC	P	PWR_SHAPE	LX_DPMIC*	Y
	PWR_SHAPE_LX	P	PWR_SHAPE	CX*	Y
System-Wide	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_BOOST*	Y
	PWR_50UM	P	PWR_50UM	PP3V0_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_IO	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_S4	Y
	PWR_200UM	P	PWR_200UM	PP1V2_IO	Y
	PWR_200UM	P	PWR_200UM	PP1V2_S2	Y
	PWR_200UM	P	PWR_200UM	PP1V2_S4	Y
SoC:CPU/GPU	PWR_SHAPE	P	PWR_SHAPE	PP_CPU_PCORE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_CPU_ECORE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_GPU	Y
SoC:SRAM/SOC	PWR_SHAPE	P	PWR_SHAPE	PP_CPU_SRAM	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SRAM_S1	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SOC_S1	Y
SoC:Fixed	PWR_SHAPE	P	PWR_SHAPE	PP0V78_SOC_FIXED_S1	Y
	PWR_80UM	P	PWR_80UM	PP0V78_VDD_FIXED_XTAL	Y
	PWR_80UM	P	PWR_80UM	PP0V78_SOC_FIXED_PCIE_REFBUF	Y
SoC:VDD12	PWR_80UM	P	PWR_80UM	PP1V2_S1	Y
	PWR_80UM	P	PWR_80UM	PP1V2_S1_XTAL	Y
	PWR_200UM	P	PWR_200UM	PP1V2_SOC	Y
	PWR_80UM	P	PWR_80UM	PP1V2_SOC_FILT	Y
	PWR_80UM	P	PWR_80UM	PP1V2_VDD12_FMON	Y
	PWR_80UM	P	PWR_80UM	PP1V2_VDD12_ULPPLL_S2	Y
	PWR_80UM	P	PWR_80UM	PP1V2_IO_GRP*	Y
SoC:DDR	PWR_SHAPE	P	PWR_SHAPE	PP_DCS_S1	Y
	PWR_200UM	P	PWR_200UM	PP0V6_VDDQL_S1	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V06_S2	Y
SoC:Misc.	PWR_SHAPE	P	PWR_SHAPE	PP0V7_VDD_LOW_S2	Y
	PWR_80UM	P	PWR_80UM	PP0V7_VDD_LOW_*LPPLL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_AVE_S1	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_DISP_S1	Y
	PWR_200UM	P	PWR_200UM	PP0V6_VDDIO06_GRP1_*	Y
NAND	PWR_100UM	P	PWR_100UM	PP_NAND_VDDIO1_R	Y
	PWR_300UM	P	PWR_300UM	PP_NAND_VDDIO1_F	Y
	PWR_SHAPE	P	PWR_SHAPE	PP0V83_NAND	Y
	PWR_100UM	P	PWR_100UM	PP0V83_NAND_PLL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP2V625_NAND	Y
PMU	PWR_SHAPE	P	PWR_SHAPE	PP1V5_VLDOINT	Y
	PWR_SHAPE	P	PWR_SHAPE	PP0V9_S1	Y
Yangtze	PWR_SHAPE	P	PWR_SHAPE	PP_VBUS1_E75	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VBUS2_DOTARA	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_CHARGER_PMID	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_BATT_VCC_YANGTZE	Y
	PWR_100UM_LX	P	PWR_100UM	LX_CHARGER_BOOT*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP6V0_CHARGER_LDO_INTERNAL	Y
	PWR_80UM	P	PWR_80UM	PP1V8_ALWAYS	Y
Dotara	PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_COIL1	Y
	PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_AC2	Y
	PWR_SHAPE	P	PWR_SHAPE	DOTARA_TX_BANK_2	Y
	PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_COIL2	Y
	PWR_100UM	P	PWR_100UM	DOTARA_COMM*	Y
	PWR_200UM	P	PWR_200UM	DOTARA_CLAMP*	Y
	PWR_200UM	P	PWR_200UM	DOTARA_BOOT*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_DOTARA_VMID	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_DOTARA_VRECT	Y
	PWR_200UM	P	PWR_200UM	PP1V8_DOTARA_LDO	Y
	PWR_100UM	P	PWR_100UM	PP5V0_VDD_DOTARA	Y
	PWR_100UM	P	PWR_100UM	PP5V0_DOTARA_VMID	Y
	PWR_80UM	P	PWR_80UM	PP1V2_DOTARA_S2	Y
Camera PMUs	PWR_SHAPE	P	PWR_SHAPE	PP1V3_CAM_PMU*_BUCK0	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAX_CAM_PMU*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_RTC_CAM_PMU*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_CAM_PMU1_IO_SW	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V2_INT_CAM_PMU*	Y
Will/Jasper	PWR_100UM	P	PWR_100UM	PP3V0_WILL_VDD	Y
	PWR_100UM	P	PWR_100UM	PP1V8_CAM_PMU2_IO_SW	Y
	PWR_100UM_HV	P	PWR_100UM	PN_JASPER_VDDHV*	Y
	PWR_100UM	P	PWR_100UM	PP_JASPER_VDDLAS*	Y
Strobe	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_COOL_LED	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_WARM_LED	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_BOOST_OUT	Y
Rigel/Pearl	PWR_SHAPE	P	PWR_SHAPE	PP_VANA	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_VINCORE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_BUCK_BOOST_A	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_BUCK_BOOST_B	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_CATHODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_DENSE_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_SPARSE_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_A_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_B_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_BANE_ANODE	Y
	PWR_100UM	P	PWR_100UM	PP3V3_MAMABEAR_VDD	Y
Audio	PWR_50UM	P	PWR_50UM	PP1V8_AUDIO_VA_S2	Y
Codec	PWR_200UM	P	PWR_200UM	AGND_CODEC	Y
BotSpk	PWR_50UM	P	PWR_50UM	PP_VA_BOT_SPK_INTERNAL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SPKRAMP_BOT_VBOOST	Y
	PWR_SHAPE	P	PWR_SHAPE	SPKRAMP_BOT_TO_COIL_OUT_*	Y
	PWR_80UM	P	PWR_80UM	AGND_BOT_SPK	Y
TopSpk	PWR_50UM	P	PWR_50UM	PP_VA_TOP_SPK_INTERNAL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SPKRAMP_TOP_VBOOST	Y
	PWR_SHAPE	P	PWR_SHAPE	SPKRAMP_TOP_TO_COIL_OUT_*	Y
	PWR_80UM	P	PWR_80UM	AGND_TOP_SPK	Y

Physical (continued)

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Arc	PWR_50UM	P	PWR_50UM	PP1V2_ARCAMP_VD_FILT_INTERNAL	Y
	PWR_50UM	P	PWR_50UM	PP1V8_ARCAMP_VA_VL_INTERNAL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ARCAMP_VBOOST	Y
	PWR_SHAPE	P	PWR_SHAPE	ARCAMP_TO_SOLENOID_OUT*	Y
	PWR_80UM	P	PWR_80UM	AGND_ARCAMP	Y
Touch	PWR_100UM	P	PWR_100UM	PP1V2_TOUCH_S2*	Y
	PWR_80UM	P	PWR_80UM	PP3V1_TOUCH_S2*	Y
	PWR_200UM	P	PWR_200UM	PP1V8_TOUCH_S2*	Y
Display PMIC	PWR_SHAPE	P	PWR_SHAPE	PP7V3_DISPLAY_AVDDH*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP4V6_DISPLAY_VDDEL*	Y
	PWR_SHAPE	P	PWR_SHAPE	PNVAR_DISPLAY_VSSEL*	Y
Kraken	PWR_SHAPE	P	PWR_SHAPE	PP_ACC_VAR	Y
	PWR_80UM	P	PWR_80UM	PP_VAR_USB_RVP	Y
	PWR_200UM	P	PWR_200UM	PP_KRAKEN_ACC1*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_KRAKEN_ACC2*	Y
	PWR_80UM	P	PWR_80UM	ANALOG_VDD_MAIN_OV_R	Y
Parrot	PWR_80UM	P	PWR_80UM	PP3V3_USB_S2	Y
AF/OIS (Shared)	PWR_SHAPE	P	PWR_SHAPE	PPVAR_RCAM_PVDD	Y
Wide RCAM	PWR_100UM	P	PWR_100UM	PPVAR_WIDE_PVDD_CONN	Y
	PWR_100UM	P	PWR_100UM	PP3V2_WIDE_AVDD1	Y
	PWR_200UM	P	PWR_200UM	PPVAR_WIDE_AVDD2	Y
	PWR_100UM	P	PWR_100UM	PP1V6_WIDE_DVDD*	Y
SWide RCAM	PWR_100UM	P	PWR_100UM	PP2V85_SWIDE_AVDD1	Y
	PWR_200UM	P	PWR_200UM	PPVAR_SWIDE_AVDD2	Y
	PWR_100UM	P	PWR_100UM	PP1V2_SWIDE_DVDD	Y
Camera VDDIO	PWR_80UM	P	PWR_80UM	PP1V8_*VDDIO*	Y
Tele RCAM	PWR_100UM	P	PWR_100UM	PPVAR_TELE_PVDD_CONN	Y
	PWR_100UM	P	PWR_100UM	PP0V8_TELE_DVDD1	Y
	PWR_100UM	P	PWR_100UM	PP0V975_TELE_DVDD2	Y
	PWR_100UM	P	PWR_100UM	PP2V85_TELE_AVDD1	Y
	PWR_200UM	P	PWR_200UM	PP1V35_TELE_AVDD2	Y
FCAM	PWR_200UM	P	PWR_200UM	PP1V1_FCAM_DVDD	Y
	PWR_200UM	P	PWR_200UM	PP2V85_FCAM_AVDD*	Y
Juliet IRCAM	PWR_80UM	P	PWR_80UM	PP2V85_IRCAM_AVDD	Y
	PWR_80UM	P	PWR_80UM	PP1V2_IRCAM_DVDD	Y
Jasper	PWR_80UM	P	PWR_80UM	PP3V0_JASPER_RX_AVDD*	Y
	PWR_80UM	P	PWR_80UM	PP3V3_JASPER_TX_AVDD*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V1_JASPER_DVDD*	Y
B2B	PWR_DEFAULT	P	PWR_DEFAULT	PP1V8_ALS_S2	Y
	PWR_80UM	P	PWR_80UM	PP1V8_COMPASS_S2_CONN	Y
Kobol	PWR_80UM	P	PWR_80UM	PP_VDDIO_IMU	Y
Penrose	PWR_80UM	P	PWR_80UM	PP3V0_PENROSE_SVDD*	Y
Dock	PWR_80UM	P	PWR_80UM	PP1V8_DOCK_S2_CONN	Y
	PWR_200UM	P	PWR_200UM	PPVAR_EIGER_S2*	Y
Display	PWR_80UM	P	PWR_80UM	PP1V2_DISPLAY_S2_CONN	Y
	PWR_80UM	P	PWR_80UM	PP1V8_DISPLAY_DVDD_CONN	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1VX_DISPLAY_S2*	Y
	PWR_80UM	P	PWR_80UM	PP3V0_DISPLAY_S2*	Y
NFC/Ironman NFC	PWR_80UM	P	PWR_80UM	PP1V2_NFC_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*_VDDBOOST	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDC	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDNV	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_TVDD	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDPLL	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VHV	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX,PP_NFC_*_VCASCHI,PP_NFC_*_VCASLO	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VREF	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_AVDD	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*_VUP	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_P_ANT_POS, NFC_P_ANT_NEG	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_F_ANT_POS, NFC_F_ANT_NEG	Y
Arrow	PWR_SHAPE	P	PWR_SHAPE	PP1V0_S4	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V0_R1_ANA_S4	Y
QETs/APTs	PWR_SHAPE	P	PWR_SHAPE	PP_APT_L_PA	Y
Radio	PWR_100UM	P	PWR_100UM	PP_VDD_RF_1V2	Y
	PWR_100UM	P	PWR_100UM	PP_VIO_RFFE*_1V8*,PP_RFFE*1V8*	Y
	PWR_80UM	P	PWR_80UM	PP_1V8_LDO6	Y
	PWR_80UM	P	PWR_80UM	PP_UIM1_LDO11	Y
	PWR_80UM	P	PWR_80UM	PP_UIM2_LDO13	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_VDD_AMP*	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_VAUX_S	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_PA_VBAT_LDO	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_AMP_OUT	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_QET1_PA	Y
	PWR_100UM	P	PWR_100UM	SUBUS_UAT_A*	Y
	PWR_100UM	P	PWR_100UM	SUBUS_UAT_B*	Y
	PWR_100UM	P	PWR_100UM	SUBUS_LAT_B*	Y
	PWR_100UM	P	PWR_100UM	SUBUS_LAT_C*	Y

DOMAIN: D.P.SI	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	ANALOG_NAND_ZQ*

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CONSTRAINTS: Power

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Power Spacing

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	S	MSAP_YIELD	GND	Y
PWR_DEFAULT	S	DEFAULT	=	Y
PWR_50UM	S	DEFAULT	=	Y
PWR_80UM	S	DEFAULT	=	Y
PWR_100UM	S	DEFAULT	=	Y
PWR_200UM	S	DEFAULT	=	Y
PWR_300UM	S	DEFAULT	=	Y
PWR_SHAPE	S	DEFAULT	=	Y
PWR_100UM_HV	S	HV_SPACING	=	Y
PWR_SHAPE_LX	S	NA_DIELECTRIC_2X_LX	=	Y
PWR_100UM_LX	S	NA_DIELECTRIC_2X_LX	=	Y
PWR_SHAPE_LX_DPMIC	S	NA_DIELECTRIC_2X_LX	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_100UM	GND	100UM-249UM_SPACING
PWR_100UM	PWR_100UM	100UM-249UM_SPACING
PWR_100UM	PWR_200UM	100UM-249UM_SPACING
PWR_100UM	PWR_300UM	100UM-249UM_SPACING
PWR_100UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_200UM	GND	100UM-249UM_SPACING
PWR_200UM	PWR_200UM	100UM-249UM_SPACING
PWR_200UM	PWR_300UM	100UM-249UM_SPACING
PWR_200UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_300UM	GND	250UM+_SPACING
PWR_300UM	PWR_300UM	250UM+_SPACING
PWR_SHAPE	GND	250UM+_SPACING
PWR_SHAPE	PWR_SHAPE	250UM+_SPACING
PWR_100UM_HV	GND	DEFAULT

Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_DP_GENERIC	E	GENERIC_DP	DP:DP_CODEC_AOUT*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_MIC*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_PENROSE*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_NTC_*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_*MTR*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_ANALOG*SENSE*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_ANALOG_VIN_SAKONNET_FROM_HALL*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_PMU_VDD_MAIN_SENSE*	Y
E_DP_NC	E	GENERIC_DP	DP:DP_NC*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_PWR	P	PWR_DP	DP:DP_CODEC_AOUT*	Y
DP_MIC	P	GENERIC_DP	DP:DP_*MIC*	Y
DP_PENROSE	P	GENERIC_DP	DP:DP_PENROSE*	Y
DP_NTC	P	GENERIC_DP	DP:DP_NTC_*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_*MTR*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_ANALOG*GPU_SENSE*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_ANALOG*SOC_SENSE*	Y
DP_PCPU_SENSE	P	GENERIC_DP	DP:DP_ANALOG*PCPU_SENSE*	Y
DP_SAKONNET	P	GENERIC_DP	DP:DP_ANALOG_VIN_SAKONNET_FROM_HALL*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_PMU_VDD_MAIN_SENSE*	Y
DP_NC	P	GENERIC_DP	DP:DP_NC*	Y
DP_ETDAC_QET1	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_PWR	S	DEFAULT	=	Y
DP_MIC	S	A_DIELECTRIC_1.5X	=	Y
DP_PENROSE	S	A_DIELECTRIC_1.5X	=	Y
DP_NTC	S	A_DIELECTRIC_1.5X	=	Y
DP_SAKONNET	S	A_DIELECTRIC_1.5X	=	Y
DP_PCPU_SENSE	S	A_DIELECTRIC_1.5X	=	Y
DP_GENERIC	S	DEFAULT	=	Y
DP_NC	S	DEFAULT	=	Y
DP_ETDAC_QET1	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
DP_MIC	DP_MIC	DEFAULT
DP_MIC	GND	DEFAULT
DP_MIC	PWR_MIC	DEFAULT
DP_MIC	DP_SAKONNET	DEFAULT
DP_MIC	ANALOG_SAKONNET	DEFAULT
DP_SAKONNET	DP_SAKONNET	DEFAULT
DP_SAKONNET	ANALOG_SAKONNET	DEFAULT
DP_SAKONNET	GND	DEFAULT
CLK	GND	DEFAULT
ANALOG	GND	DEFAULT
ANALOG_NTC	GND	DEFAULT
ANALOG_SAKONNET	GND	DEFAULT
ANALOG_AMP_FILT	GND	DEFAULT

Clocks

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	P	DEFAULT	CLK_*	Y
CLK	P	DEFAULT	SPMI*CLK*	Y
CLK	P	DEFAULT	I2S*MCLK*	Y
CLK	P	DEFAULT	SPI*SCLK*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	S	A_DIELECTRIC_1.5X	=	Y

Sensitive Analog

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG_SAKONNET	P	DEFAULT	ANALOG*SAKONNET_TO_HALL*	Y
ANALOG	P	DEFAULT	ANALOG*DOTARA*	Y
ANALOG	P	DEFAULT	ANALOG*DOMBRA*	Y
ANALOG	P	DEFAULT	ANALOG*SENSE,ANALOG*SENSE_SE,ANALOG*SENSE_FILT	Y
ANALOG	P	DEFAULT	ANALOG*ZQ*	Y
ANALOG	P	DEFAULT	ANALOG*REXT*	Y
ANALOG	P	DEFAULT	ANALOG*CAL*	Y
ANALOG	P	DEFAULT	ANALOG_*REF*	Y
ANALOG	P	DEFAULT	ANALOG_FB*	Y
ANALOG	P	DEFAULT	ANALOG*PDTS*	Y
ANALOG	P	DEFAULT	ANALOG_KRAKEN_BYPASS	Y
GRP_GPIO	P	DEFAULT	ANALOG_KRAKEN_BI_CCG2B_CC	Y
ANALOG	P	DEFAULT	ANALOG_RIGEL_LSCP	Y
ANALOG_AMP_FILT	P	PWR_80UM	ANALOG_*_SPK_FILT,ANALOG_ARC_FILT	Y
ANALOG	P	DEFAULT	VSS_PMU_XTAL	Y
ANALOG	P	DEFAULT	AMUX*	Y
ANALOG_NTC	P	DEFAULT	NTC_STROBE_MODULE*	Y
ANALOG_NTC	P	DEFAULT	NTC_PEARL_VCSEL_TO_RIGEL	Y
ANALOG_NTC	P	DEFAULT	NTC_STOCKHOLM	Y
ANALOG	P	DEFAULT	COIL_TO_SPKRAMP_*_VSENSE_*, SOLENOID_TO_ARCAMP_VSENSE_*	Y
PWR_MIC	P	PWR_DEFAULT	PP_CODEC_TO_MIC*_BIAS*,RET_CODEC_FROM_MIC*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_AMP_FILT	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_NTC	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_SAKONNET	S	A_DIELECTRIC_1.5X	=	Y
PWR_MIC	S	DEFAULT	=	Y

Grouping Constraints

Physical

Used to clean up CM

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	P	DEFAULT	GPIO*, IO_*	Y
GRP_NC	P	DEFAULT	NC_*	Y
GRP_I2C	P	DEFAULT	I2C*	Y
GRP_I2S	P	DEFAULT	I2S*LRCLK*, I2S*BCLK*, I2S*DOUT*, I2S*DIN*	Y
GRP_SPI	P	DEFAULT	SPI*MOSI*, SPI*MISO*, SPI*CS*	Y
GRP_UART	P	DEFAULT	UART*	Y
GRP_SWD	P	DEFAULT	SWD*	Y
GRP_SPMI_DATA	P	DEFAULT	SPMI*DATA*	Y
GRP_PCIE_SIDE	P	DEFAULT	PCIE*CLKREQ*, PCIE*PERST*	Y
GRP_LPDP_AUX	P	DEFAULT	LPDP*AUX*	Y
GRP_RFFE_WLAN	P	DEFAULT	RFFE_WLAN_*	Y
GRP_RFFE_BB	P	DEFAULT	SHIELD_RFFE*	Y
GRP_CODEC_FILT	P	PWR_200UM	CODEC_*FILTP,CODEC_*FILTN	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SPACING STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	S	DEFAULT	=	Y
GRP_NC	S	DEFAULT	=	Y
GRP_I2C	S	DEFAULT	=	Y
GRP_I2S	S	DEFAULT	=	Y
GRP_SPI	S	DEFAULT	=	Y
GRP_UART	S	DEFAULT	=	Y
GRP_SWD	S	DEFAULT	=	Y
GRP_SPMI_DATA	S	DEFAULT	=	Y
GRP_PCIE_SIDE	S	DEFAULT	=	Y
GRP_LPDP_AUX	S	DEFAULT	=	Y
GRP_RFFE_WLAN	S	DEFAULT	=	Y
GRP_RFFE_BB	S	DEFAULT	=	Y
GRP_CODEC_FILT	S	DEFAULT	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_SHAPE_LX	GND	DEFAULT
PWR_SHAPE_LX	PWR_SHAPE_LX	DEFAULT
PWR_SHAPE_LX	ANALOG	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_AMP_FILT	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_NTC	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_SAKONNET	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK	A_DIELECTRIC_3X
PWR_100UM_LX	GND	DEFAULT
PWR_SHAPE_LX_DPMIC	GND	A_DIELECTRIC_3X

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50 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
ISL2	TOP,ISL3	50	0.029
ISL6	ISL7,ISL5	50	0.038
ISL8	ISL9,ISL7	50	0.029
BOTTOM	ISL9	50	0.057

50 Wide

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
ISL6	ISL4,ISL8	50	0.098
ISL7	ISL9,ISL5	50	0.092
ISL8	BOTTOM,ISL6	50	0.085
BOTTOM	ISL8	50	0.167

50 Wide, External Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_SURFACE_THIN		ZONE NAME= PRIMARY	
ISL6	ISL4,ISL8	50	0.098
ISL7	ISL9,ISL5	50	0.092
ISL8	BOTTOM,ISL6	50	0.085
BOTTOM	ISL9	50	0.057

50 Wide, L8 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_L8_THIN		ZONE NAME= PRIMARY	
ISL6	ISL4,ISL8	50	0.098
ISL7	ISL9,ISL5	50	0.092
ISL8	ISL9,ISL7	50	0.029
BOTTOM	ISL8	50	0.167

50 Wide, L6 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_L6_THIN		ZONE NAME= PRIMARY	
ISL6	ISL7,ISL5	50	0.038
ISL7	ISL9,ISL5	50	0.092
ISL8	BOTTOM,ISL6	50	0.085
BOTTOM	ISL8	50	0.167

50-ohm (Wide) Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT7*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT9*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PAD_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_RX1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_RX1_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_TX_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_L5_LNA_IN,50_TRX_ANT3_L5	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_UHB_ANT1_TO_ANT7_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT2_TO_ANT9*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT1_TO_ANT7*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_UHB_PAD_PORTB_TX_M	Y
	50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_UHB_PAD_N79_PORTB_TX_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_UHB_PAD_PORTB_TX	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_CPLR_L_CPL2_IN_LB_LMB_MB_HB	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HB_PAD_ANT1_M	Y
Arrow	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_R1_AOA1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_R1_AOA2	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_R1_ANT*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_UWB_ANT*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT6_WLAN_A_LAA	Y
WiFi	50_TRX_WIDE	P	A_50_WIDE_SE	50_R1_WLAN_A_LAA_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT5_WLAN_A_LAA	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_A_LAA_DPLXR	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_A_LAA_BPF_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_A_LAA_BPF	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBU_N79_ANT2_TO_ANT8*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT2_TO_ANT8*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBL_N77_ANT2_TO_ANT8*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_TRX_WIDE	GND	NA_DIELECTRIC_2X_50_WIDE_SE
50_TRX_WIDE_SURFACE_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_THIN_SE
50_TRX_WIDE_L8_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_L8_THIN_SE
50_TRX_WIDE_L6_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_L6_THIN_SE

50-ohm (Thin) Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Wildcards	50_RX_THIN	P	A_50_THIN_SE	50_RX_*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_XCVR_PRX12	Y
Direct Net	50_TX0_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_TX0_LB	Y
	50_TX0_THIN	P	A_50_THIN_SE	50_TX_IN_TX0_LB_PAD_TX_LB_IN	Y
	50_TX0_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_TX1_LB_JB	Y
	50_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_TX1_LB_JB_M	Y
	50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	Y
	50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	Y
	50_RX_THIN	P	A_50_THIN_SE	50_L5_LNA_NOTCH1	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_UHB_L_CPLR_OUT	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_C0_TXRX_FEM_M	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_UAT_TXRX_FEM	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_ANT2_LB_LMB_MB_HB_L1	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_R1_AOA3	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_TRX_UHB_PAD_N79_PORTB_TX	Y
	50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_LAA_ANT5_B2B_M	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TX_IN_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX0_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX0_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX2_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_RX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TRX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y

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50-ohm Thin Overrides

DOMAIN B.P.S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_TRX_LB_PAD_ANT1_M
P	A_50_THIN_SE	50_TRX_ANT3_L5
P	A_50_THIN_SE	50_TRX_DPLX_LB_LMB_MB_HB_ANT1
P	A_50_THIN_SE	50_TRX_ANT7_UHB_N79_M
P	A_50_THIN_SE	50_TRX_ANT7_UHB_N79_L
P	A_50_THIN_SE	50_TRX_ANT7_UHB_N79_NOTCH
P	A_50_THIN_SE	50_TRX_ANT8_UHB_N79_L
P	A_50_THIN_SE	50_TRX_ANT8_UHB_N79_NOTCH
P	A_50_THIN_SE	50_TRX_ANT9_UHB_N79_L
P	A_50_THIN_SE	50_TRX_ANT9_UHB_N79_NOTCH
P	A_50_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB_M

DOMAIN B.P.S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_LB_PAD_ANT1_M
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT3_L5
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_DPLX_LB_LMB_MB_HB_ANT1
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT7_UHB_N79_M
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT7_UHB_N79_L
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT7_UHB_N79_NOTCH
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT8_UHB_N79_L
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT8_UHB_N79_NOTCH
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT9_UHB_N79_L
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT9_UHB_N79_NOTCH
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB_M

50-ohm (Hybrid) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBL_UHB_ANT1_TO_ANT7	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_FEM_M	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_WLAN_G_BT_ANT3_NPLXR	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9_M	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LB_LMB_MB_HB	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_WLAN_G_BT_ANT3_NPLXR_M	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_R1_ANT2_CH9	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_ANT8_UHB_N79_M	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_CPLR_L_CPL3_ANT_LMB_MB_HB	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_LB_PORTB_TX_ANT2	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_WLAN_A_LAT_TXRX_FEM	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_ANT1_LB_LMB_MB_HB	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_ANT8_R1_UHB_N79	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_WLAN_A_LAA_DPLXR_M	Y
50_TRX_WIDE_L6_THIN	P	A_50_WIDE_L6_THIN_SE	50_TRX_R1_ANT2_CH5	Y
50_TRX_WIDE_L6_THIN	P	A_50_WIDE_L6_THIN_SE	50_LAA_RX_XCVR_DRX10	Y
50_TRX_WIDE_L6_THIN	P	A_50_WIDE_L6_THIN_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE_SURFACE_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_SURFACE_THIN_SE	=	Y
50_TRX_WIDE_L8_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_L8_THIN_SE	=	Y
50_TRX_WIDE_L6_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_L6_THIN_SE	=	Y

(Thin) Class-Class Spacing

	CLASS TO CLASS SPACING		
	CLASS NAME	CLASS NAME	CONSTRAINT SET
Same Class	50_TX0_THIN	50_TX0_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX0_TX1_THIN	50_TX0_TX1_THIN	DEFAULT
	50_TX1_THIN	50_TX1_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	50_TX2_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	50_RX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
GND	50_TX0_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX0_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TRX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
TX <-> TX	50_TX0_THIN	50_TX0_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TX2_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TX0_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TX2_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX2_THIN	50_TX0_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE

SYNC_DATE=07/01/2019

PAGE TITLE
CONSTRAINTS: 50-Ohm

DRAWING NUMBER 051-05170
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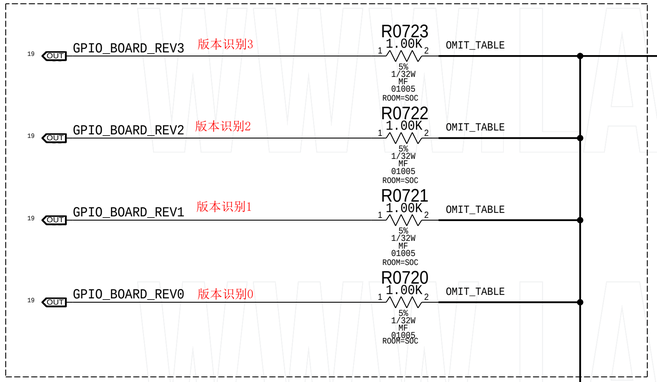
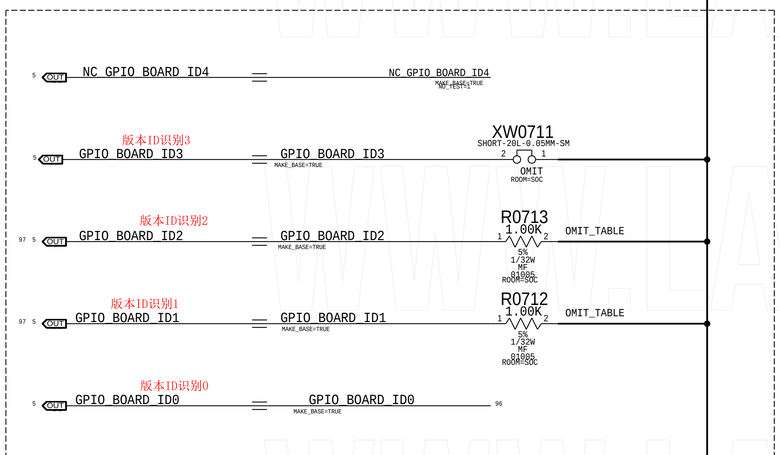
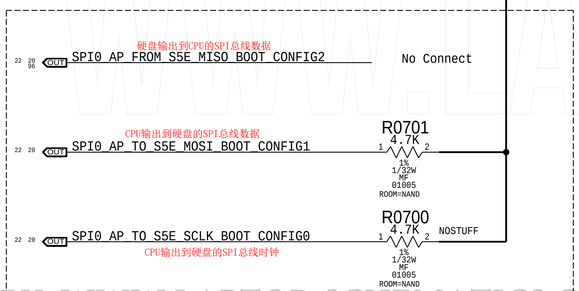
BOOTSTRAPPING

BOARD REV + BOARD ID + BOOT CONFIG







Board Rev [3:0]

* Float = 0 | PU = 1

Note: iBoot uses the inverse of BOARD_REV[3:0], so that it counts up (Pre-Proto = 0x0, PVT = 0xF)

	BOARD_REV[3:0]	[3]	[2]	[1]	[0]
Pre-Proto	4'b1111	1	1	1	1
Proto 1	4'b1110	1	1	1	0
Proto 1.5	4'b1101	1	1	0	1
Proto 2	4'b1100	1	1	0	0
Proto 2.5	4'b1011	1	0	1	1
Pre-EVT	4'b1010	1	0	1	0
EVT	4'b1001	1	0	0	1
Carrier	4'b1000	1	0	0	0
(Allocate more as necessary in descending order)					
DVT	4'b0001	0	0	0	1
PVT	4'b0000	0	0	0	0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0156	4	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0721,R0720	BOARD_REV:PROTO0	PROTO0
117S0156	3	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0721	BOARD_REV:PROTO1	PROTO1
117S0156	3	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0720	BOARD_REV:PROTO1.5	PROTO1.5
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722	BOARD_REV:PROTO2	PROTO2
117S0156	3	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0721,R0720	BOARD_REV:PROTO2.5	PROTO2.5
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0721	BOARD_REV:PRE-EVT	PRE-EVT
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0720	BOARD_REV:EVT	EVT
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723	BOARD_REV:CRB	CRB
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0720	BOARD_REV:DVT	DVT

(PVT NOSTUFF ALL)

Board ID [4:0]

* Float = 0 | PU = 1

	BOARD_ID[4:0]	[4] Unused	[3] 1=MAV20	[2]	[1]	[0] 0=MLB, 1=DEV
MLB D52G	5'b01010	0	1	0	1	0
DEV D52G	5'b01011	0	1	0	1	1
MLB D53G	5'b01100	0	1	1	0	0
DEV D53G	5'b01101	0	1	1	0	1
MLB D53P	5'b01110	0	1	1	1	0
DEV D53P	5'b01111	0	1	1	1	1
MLB D54P	5'b01000	0	1	0	0	0
DEV D54P	5'b01001	0	1	0	0	1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0712	BOARD_ID:D52	D52 = 01
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0713	BOARD_ID:D53G	D53G = 10
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0713,R0712	BOARD_ID:D53P	D53P = 11
(D54 both NOSTUFF)					D54 = 00

Boot Config [2:0]

* Float = 0 | PU = 1

	USAGE	SPEED	TEST	[2]	[1]	[0]	
SPI1 NOR	--	12MHz	--	0	0	0	
SPI1 NOR	--	12MHz	Test	0	0	1	
SPI0 NAND	POR	12MHz	--	0	1	0	<-- POR
SPI0 NAND	Proto	12MHz	Test	0	1	1	<-- Proto Builds
SPI1 NOR	--	24MHz	--	1	0	0	
SPI1 NOR	--	24MHz	Test	1	0	1	
SPI1 NOR	--	6MHz	--	1	1	0	
SPI1 NOR	--	6MHz	Test	1	1	1	<--- Remove at EVT

PAGE TITLE

SYSTEM: Bootstrapping

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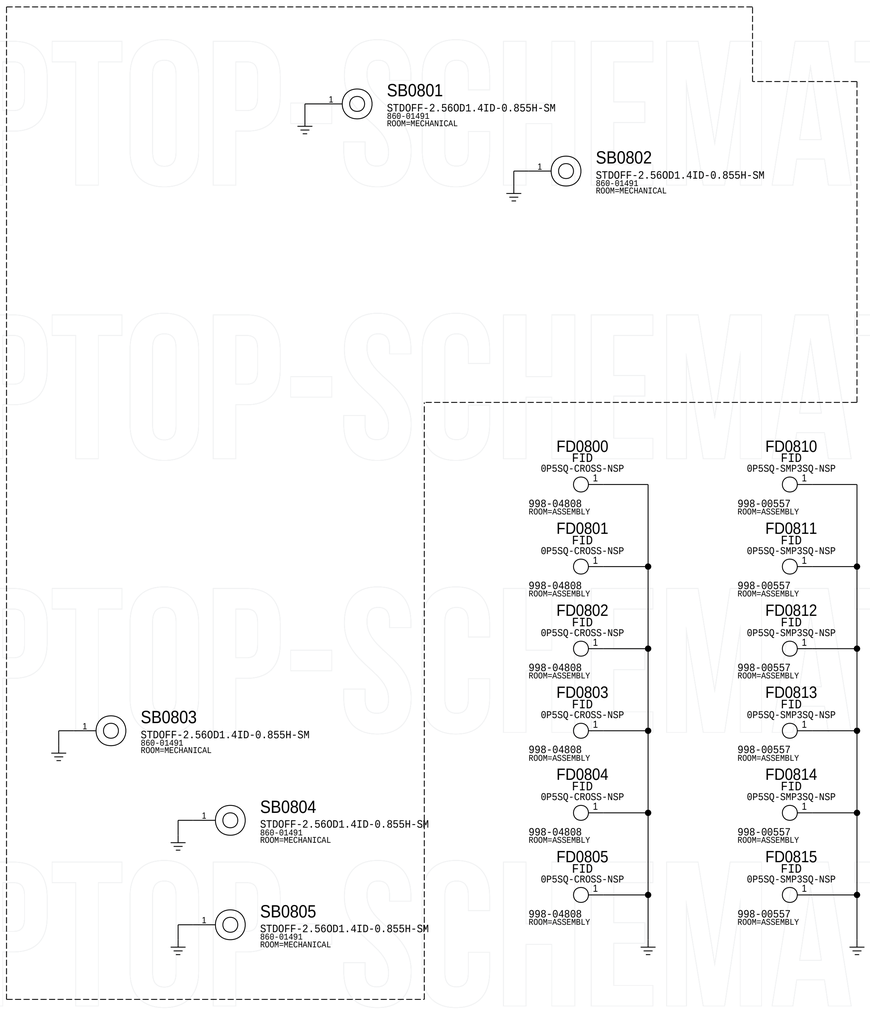
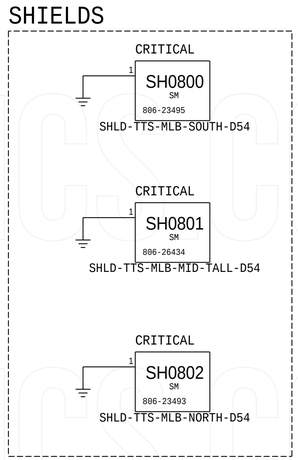
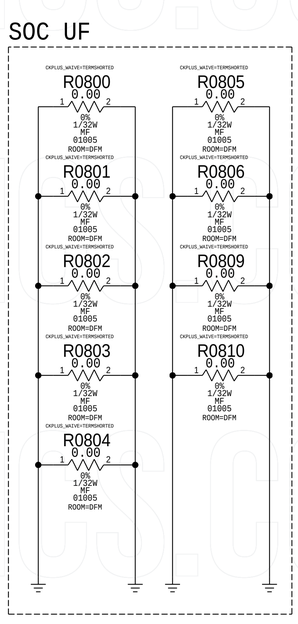
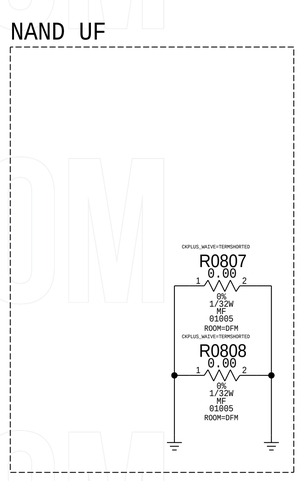
Conventions:

1. Nets which are not connected on FFs but probed out on dev board should start with "NC_DEV_"
2. Nets that contain "_1V8" are 1.8V logic, all other nets are implied 1.2V logic
3. Components with PACK_IGNORE=TRUE will not be included in the netlist









Interposer Spacers

RefDes called out below

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-03604	20	SPACER,INTERPOSER,SMALL,X891		CRITICAL	?

SP0801, SP0802, SP0803, SP0804, SP0805, SP0806, SP0807, SP0808, SP0809, SP0810, SP0811, SP0812, SP0813, SP0814, SP0815, SP0816, SP0817, SP0818, SP0819, SP0820

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PAGE TITLE: SYSTEM: Mechanical

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SOC

4GB DRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22473	1	Sicily,B1,4GB,M	U1000	CRITICAL	BOARD_ID:0526B0ARD_ID:0536

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-22472	998-22473	BOARD_ID:0526B04RD_ID:0536	U1000	Sicily,B1,4GB,H
998-22471	998-22473	BOARD_ID:0526B04RD_ID:0536	U1000	Sicily,B1,4GB,S

6GB DRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22474	1	Sicily,B1,6GB,M	U1000	CRITICAL	BOARD_ID:053FB0ARD_ID:054

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-22475	998-22474	BOARD_ID:053FB0ARD_ID:054	U1000	Sicily,B1,6GB,H
998-22476	998-22474	BOARD_ID:053FB04RD_ID:054	U1000	Sicily,B1,6GB,S

24M XTAL Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0612	197S00118	?	Y1000	XTAL, 24M, 1612
197S00120	197S00118	?	Y1000	XTAL, 24M, 1612

SOC: Misc

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 1 OF 21
OMIT_TABLE

BOARD ID
- GPIO_BOARD_ID0 版本ID识别0 — CN11 — BOARD_ID0
- GPIO_BOARD_ID1 版本ID识别1 — CM15 — BOARD_ID1
- GPIO_BOARD_ID2 版本ID识别2 — CP9 — BOARD_ID2
- GPIO_BOARD_ID3 版本ID识别3 — CJ62 — BOARD_ID3
- NC_GPIO_BOARD_ID4 版本ID识别3 — CP11 — BOARD_ID4

REQUEST_DFUx: Legacy button detection
MLB: Hard tie to PP1V2_IO
DEV: Wire to PMU BUTTONO

DFU
- PP1V2_IO 1.2V供电 — BK61 — REQUEST_DFU1
- PP1V2_IO 1.2V供电 — BJ62 — REQUEST_DFU2
- IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 强制DFU信号 — AN60 — FORCE_DFU
- IO_SOC_DFU_STATUS DFU状态信号 — BK62 — DFU_STATUS

PP (dev board only)

FPWM
- NC_DEV_AP_TMR32_PWM0 — AG3 — FPWM0
- NC_DEV_AP_TMR32_PWM1 — AG2 — FPWM1
- NC_DEV_AP_TMR32_PWM2 — AJ3 — FPWM2

MISC
- IO_PAD_MTR_ANALOG_TEST_P — CB60 — PAD_MTR_ANALOG_TEST_P
- IO_PAD_MTR_ANALOG_TEST_N — CB61 — PAD_MTR_ANALOG_TEST_N

PP (dev board only)

MTR
- NC_DEV_PAD_MTR_VREF_P — CD60 — PAD_MTR_VREF_P
- NC_DEV_PAD_MTR_VREF_N — CD61 — PAD_MTR_VREF_N

THROTTLERS
- THROTTLE_TRIGGER0 — BJ61 — NC_DEV_SOC_THROTTLE_TRIGGER0
- THROTTLE_TRIGGER1 — BJ60 — IO_AP_FROM_PMU_SW_SHDN_L CPU到主电源节能开启信号
- THROTTLE_TRIGGER2 — BG62 — IO_AP_FROM_PMU_PRE_UVLO_L
- THROTTLE_TRIGGER3 — BG61 — NC_DEV_SOC_THROTTLE_TRIGGER3
- THROTTLE_TRIGGER4 — BE62 — NC_DEV_SOC_THROTTLE_TRIGGER4

THROTTLE_TRIGGER[0:4]:
These need an internal pull-up enabled on SoC

- SOCHOT1 — BE61 — IO_SOC_TO_PMU_SOCHOT_RESET_L
- SWD_TCK_OUT1 — CP15 — SWD_AP_TO_MANY_SWCLK CPU输出的SWD总线时钟
- SWD_TMS2 — CN15 — SWD_AP_BI_NAND_SWDIO CPU到硬盘的SWD总线数据
- SWD_TMS3 — CP13 — SWD_AP_BI_BB_SWDIO CPU到基带的SWD总线数据
- SWD_TMS4 — CK62 — SWD_AP_BI_R1_SWDIO CPU到U1的SWD总线数据

Clocked by SWD_TCK_OUT1

- TST_CLKOUT — BE60 — CLK_AP_TO_PMU_TST_CLKOUT CPU到电源的测试时钟
- ANALOGMUX_OUT — CN3 — AMUX_SOC_TO_PMU_AMUX_OUT CPU到电源模拟信号
- CFSB — CL7 — IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY 电源输出的准备就绪信号
- CFSB_XTAL — F5 — IO_AON_TO_AP_XTAL_CFSB CPU内部端口休眠唤醒信号
- HOLD_RESET — AG60 — GND
- TESTMODE — AF62 — GND

PP0V6_VDDQL_S1

R1010 R1011 R1012 R1013 R1014 R1015
240 1% 1/32W MF 01005 ROOM=SOC

DDR
- DDR0_RREF — CJ3 — ANALOG_DDR0_RREF
- DDR0_ZQ — BM2 — ANALOG_DDR0_ZQ
- DDR1_RREF — BV60 — ANALOG_DDR1_RREF
- DDR2_RREF — K3 — ANALOG_DDR2_RREF
- DDR3_RREF — Y61 — ANALOG_DDR3_RREF
- DDR3_ZQ — AB62 — ANALOG_DDR3_ZQ
- LP4_IN_RESET* — V60 — IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位

XTAL
- XI0 — E9 — CLK_AP_XTAL_24M_IN
- XO0 — D9 — CLK_AP_XTAL_24M_OUT

R1021 499 1% 1/32W MF 01005 ROOM=SOC_XTAL
CLK_AP_XTAL_24M_OUT_R

197S00118
CRITICAL
ROOM=SOC_XTAL
Y1000
1.60X1.20MM-SM
24MHZ-30PPM-9.5PF-600HM

C1020 12PF 5% 16V NP0-C0G 01005-1 ROOM=SOC_XTAL
C1021 12PF 5% 16V NP0-C0G 01005-1 ROOM=SOC_XTAL
SOC_XTAL_GND

XW1000
SHORT-20L-0.05MM-SM
OMIT
NO_XNET_CONNECTION
ROOM=SOC_XTAL

SOC: NAND + USB

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 2 OF 21
OMIT_TABLE

R1001 33.2 1% 1/32W MF 01005 ROOM=SOC

- CLK_AP_TO_NAND_24M CPU到硬盘24M时钟
- CLK_AP_TO_NAND_24M_R CPU到硬盘24M时钟 — AR2 — NAND_SYS_CLK
- IO_AP_TO_NAND_RESET_L CPU到硬盘复位 — AJ62 — SSD_RESET*
- IO_AP_TO_NAND_FW_STRAP CPU到硬盘的启动信号 — AL60 — SSD_BFH

NAND - IOS

USB
- USB_EDP — A28 — 90_EUSB_PARROT_BI_AP_P CPU输出的USB信号P
- USB_EDM — B28 — 90_EUSB_PARROT_BI_AP_N CPU输出的USB信号N
- USB_RESREF — D28 — ANALOG_SOC_USB_RESREF CPU内部USB模块复位
- EUSB_VBUS_DETECT — AG61 — PP1V2_IO 1.2V供电

R1002 200 1% 1/32W MF 01005 ROOM=SOC

SYNCING: D52, D53, D54

PAGE TITLE	SOC: NAND + USB & Misc
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SOC: PCIe

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 3 OF 21
OMIT_TABLE

LINK0 | LINK1 | LINK2

PCIE GEN4 - ST LINK 0

20 NC_DEV_PCIE_GP0_AP_CLKREQ_L — CB3 GP_PCIE_CLKREQ0*
ST_PCIE_CLKREQ0* CB2 — 硬盘到CPU的PCIE总线时钟请求 PCIE_ST0_AP_BI_NAND_CLKREQ_L (BI 22)

30 6 PP1V2_IO 1.2V供电 — R1100 47.0K 5% 1/32W MF 01005 ROOM=SOC (1–2)

20 NC_DEV_PCIE_GP0_AP_RX_P — B15 GP_PCIE_RX0_P
20 NC_DEV_PCIE_GP0_AP_RX_N — A15 GP_PCIE_RX0_N
ST_PCIE_RX0_P B11 — 硬盘到CPU的PCIE总线接收P 90_PCIE_ST0_AP_FROM_NAND_C_RX_P (IN 21)
ST_PCIE_RX0_N A11 — 硬盘到CPU的PCIE总线接收N 90_PCIE_ST0_AP_FROM_NAND_C_RX_N (IN 21)
RX CAPS LIVE OFF-PAGE

20 NC_DEV_PCIE_GP0_AP_TX_P — C17 GP_PCIE_TX0_P
20 NC_DEV_PCIE_GP0_AP_TX_N — D17 GP_PCIE_TX0_N
ST_PCIE_TX0_P C13 — 硬盘到CPU的PCIE总线发射P 90_PCIE_ST0_AP_TO_NAND_C_TX_P
ST_PCIE_TX0_N D13 — 硬盘到CPU的PCIE总线发射N 90_PCIE_ST0_AP_TO_NAND_C_TX_N
C1102 GND_VOID ROOM=SOC 1 2 0.22UF CER-X5R 10% 6.3V 01005 — 硬盘到CPU的PCIE总线发射P 90_PCIE_ST0_AP_TO_NAND_TX_P (OUT 22)
C1103 GND_VOID ROOM=SOC 1 2 0.22UF CER-X5R 10% 6.3V 01005 — 硬盘到CPU的PCIE总线发射N 90_PCIE_ST0_AP_TO_NAND_TX_N (OUT 22)

20 NC_DEV_PCIE_GP0_AP_RESET_L — CF2 GP_PCIE_PERST0*
ST_PCIE_PERST0* CD3 — CPU到硬盘的PCIE总线复位 PCIE_ST0_AP_TO_NAND_PERST_L (OUT 22)

R1101 47.0K 5% 1/32W MF 01005 ROOM=SOC (1–2)

30 6 PP1V2_IO 1.2V供电 — R1130 47.0K 5% 1/32W MF 01005 ROOM=SOC (1–2)

GP_PCIE_CLKREQ2* CD2 — 基带到CPU的PCIE总线时钟请求 PCIE_GP2_AP_BI_BB_CLKREQ_L (BI 99)
BB CLKREQ PULL-UP LIVES IN RADIO HIERARCHY

WIFI到CPU的 PCIE总线时钟请求 PCIE_GP1_AP_BI_WLAN_CLKREQ_L (BI 98) — CB4 GP_PCIE_CLKREQ1*

PCIE GEN2 - LINK 1

RX CAPS LIVE OFF-PAGE
21 IN — CPU到WIFI PCIE总线接收P 90_PCIE_GP1_AP_FROM_WLAN_C_RX_P — B19 GP_PCIE_RX1_P
21 IN — CPU到WIFI PCIE总线接收N 90_PCIE_GP1_AP_FROM_WLAN_C_RX_N — A19 GP_PCIE_RX1_N

CPU到WIFI PCIE总线发射P 90_PCIE_GP1_AP_TO_WLAN_TX_P (OUT 98)
CPU到WIFI PCIE总线发射N 90_PCIE_GP1_AP_TO_WLAN_TX_N (OUT 98)
C1112 GND_VOID ROOM=SOC 1 2 0.1UF X5R-CERM 20% 6.3V 01005 — CPU到WIFI PCIE总线发射P 90_PCIE_GP1_AP_TO_WLAN_C_TX_P — C21 GP_PCIE_TX1_P
C1113 GND_VOID ROOM=SOC 1 2 0.1UF X5R-CERM 20% 6.3V 01005 — CPU到WIFI PCIE总线发射N 90_PCIE_GP1_AP_TO_WLAN_C_TX_N — D21 GP_PCIE_TX1_N

PCIE_GP1_AP_TO_WLAN_PERST_L (OUT 98) — CPU到WIFI PCIE总线复位 — CF4 GP_PCIE_PERST1*

R1131 100K 5% 1/32W MF 01005 ROOM=SOC (1–2)

ANALOG_PCIE_RCAL_POS — E19 PCIE_RCAL_P
R1140 NO_XNET_CONNECTION=1 200 1% 1/32W MF 01005 ROOM=SOC (1–2)
ANALOG_PCIE_RCAL_NEG — F19 PCIE_RCAL_N
C1140 10PF 5% 16V NP0/C0G 01005 ROOM=SOC (1–2)

PCIE GEN4 - LINK 2

GP_PCIE_RX2_P B22 — CPU到基带的PCIE总线数据接收P 90_PCIE_GP2_AP_FROM_BB_RX_P (IN 21)
GP_PCIE_RX2_N A22 — CPU到基带的PCIE总线数据接收N 90_PCIE_GP2_AP_FROM_BB_RX_N (IN 21)
RX CAPS LIVE OFF-PAGE

GP_PCIE_TX2_P C24 — CPU到基带的PCIE总线数据发射P 90_PCIE_GP2_AP_TO_BB_TX_P (OUT 99)
GP_PCIE_TX2_N D24 — CPU到基带的PCIE总线数据发射N 90_PCIE_GP2_AP_TO_BB_TX_N (OUT 99)
C1122 GND_VOID ROOM=SOC 1 2 0.22UF CER-X5R 10% 6.3V 01005
C1123 GND_VOID ROOM=SOC 1 2 0.22UF CER-X5R 10% 6.3V 01005

GP_PCIE_PERST2* CF3 — CPU到基带的PCIE总线复位 PCIE_GP2_AP_TO_BB_PERST_L (OUT 99)

R1121 100K 5% 1/32W MF 01005 ROOM=SOC (1–2)

GP_PCIE_REF_CLK0_P A7 — NC_DEV_PCIE_GP0_AP_REFCLK_P (20)
GP_PCIE_REF_CLK0_N B7 — NC_DEV_PCIE_GP0_AP_REFCLK_N (20)
GP_PCIE_REF_CLK1_P B5 — CPU到WIFI的PCIE总线时钟P 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P (OUT 98)
GP_PCIE_REF_CLK1_N A5 — CPU到WIFI的PCIE总线时钟N 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N (OUT 98)
GP_PCIE_REF_CLK2_P B4 — CPU到基带的PCIE总线时钟P 90_PCIE_GP2_AP_TO_BB_REFCLK_P (OUT 99)
GP_PCIE_REF_CLK2_N A4 — CPU到基带的PCIE总线时钟N 90_PCIE_GP2_AP_TO_BB_REFCLK_N (OUT 99)
ST_PCIE_REF_CLK0_P B6 — CPU到硬盘的PCIE总线时钟P 90_PCIE_ST0_AP_TO_NAND_REFCLK_P (OUT 22)
ST_PCIE_REF_CLK0_N A6 — CPU到硬盘的PCIE总线时钟N 90_PCIE_ST0_AP_TO_NAND_REFCLK_N (OUT 22)

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: PCIE
DRAWING NUMBER	051-05170
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SOC: ISP

DO NOT SWIZZLE LPDP LANES UNLESS ROUTING NECESSITATES IT
LPDP Swizzle Options:
-P/N can be switched
-Non-sequential lanes can be grouped
(e.g. FCAM 0 -> SOC 5, FCAM 1 -> SOC 2)
-AUX pin (one per device) doesn't have to match lane numbers

Note: LPDP RX and AUX lanes need a series 0.1uF cap

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
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OMIT_TABLE

MIPI-C

CPU到广角相机LDPD总线数据0接收N	90_LPDP_ISP_FROM_WIDE_RX_D0_N	CP19	LPDPRX_RX_D0_P
CPU到广角相机LDPD总线数据0接收P	90_LPDP_ISP_FROM_WIDE_RX_D0_P	CN19	LPDPRX_RX_D0_N
CPU到广角相机LDPD总线数据1接收N	90_LPDP_ISP_FROM_WIDE_RX_D1_N	CN21	LPDPRX_RX_D1_P
CPU到广角相机LDPD总线数据1接收P	90_LPDP_ISP_FROM_WIDE_RX_D1_P	CM21	LPDPRX_RX_D1_N
CPU到广角相机LDPD总线数据2接收N	90_LPDP_ISP_FROM_WIDE_RX_D2_N	CP22	LPDPRX_RX_D2_P
CPU到广角相机LDPD总线数据2接收P	90_LPDP_ISP_FROM_WIDE_RX_D2_P	CN22	LPDPRX_RX_D2_N
CPU到前摄LDPD总线数据0接收N	90_LPDP_ISP_FROM_FCAM_RX_D0_N	CP26	LPDPRX_RX_D3_P
CPU到前摄LDPD总线数据0接收P	90_LPDP_ISP_FROM_FCAM_RX_D0_P	CN26	LPDPRX_RX_D3_N
CPU到前摄LDPD总线数据1接收N	90_LPDP_ISP_FROM_FCAM_RX_D1_N	CN28	LPDPRX_RX_D4_P
CPU到前摄LDPD总线数据1接收P	90_LPDP_ISP_FROM_FCAM_RX_D1_P	CM28	LPDPRX_RX_D4_N
CPU到长焦相机LDPD总线数据0接收P	90_LPDP_ISP_FROM_TELE_RX_D0_P	CP30	LPDPRX_RX_D5_P
CPU到长焦相机LDPD总线数据0接收N	90_LPDP_ISP_FROM_TELE_RX_D0_N	CN30	LPDPRX_RX_D5_N
CPU到长焦相机LDPD总线数据1接收P	90_LPDP_ISP_FROM_TELE_RX_D1_P	CN32	LPDPRX_RX_D6_P
CPU到长焦相机LDPD总线数据1接收N	90_LPDP_ISP_FROM_TELE_RX_D1_N	CM32	LPDPRX_RX_D6_N
CPU到长焦相机LDPD总线数据2接收P	90_LPDP_ISP_FROM_TELE_RX_D2_P	CP34	LPDPRX_RX_D7_P
CPU到长焦相机LDPD总线数据2接收N	90_LPDP_ISP_FROM_TELE_RX_D2_N	CN34	LPDPRX_RX_D7_N
CPU到超广角相机LDPD总线数据2接收N	90_LPDP_ISP_FROM_SWIDE_RX_D2_N	CN36	LPDPRX_RX_D8_P
CPU到超广角相机LDPD总线数据2接收P	90_LPDP_ISP_FROM_SWIDE_RX_D2_P	CM36	LPDPRX_RX_D8_N
CPU到超广角相机LDPD总线数据0接收P	90_LPDP_ISP_FROM_SWIDE_RX_D0_P	CN40	LPDPRX_RX_D9_P
CPU到超广角相机LDPD总线数据0接收N	90_LPDP_ISP_FROM_SWIDE_RX_D0_N	CM40	LPDPRX_RX_D9_N
CPU到超广角相机LDPD总线数据1接收N	90_LPDP_ISP_FROM_SWIDE_RX_D1_N	CP42	LPDPRX_RX_D10_P
CPU到超广角相机LDPD总线数据1接收P	90_LPDP_ISP_FROM_SWIDE_RX_D1_P	CN42	LPDPRX_RX_D10_N
CPU到点阵LDPD总线数据0接收P	90_LPDP_ISP_FROM_JASPER_RX_D0_P	CN43	LPDPRX_RX_D11_P
CPU到点阵LDPD总线数据0接收N	90_LPDP_ISP_FROM_JASPER_RX_D0_N	CM43	LPDPRX_RX_D11_N
	ANALOG_LPDP_ISP_RX0_RCAL_POS	CM24	LPDPRX0_RCAL_P
	ANALOG_LPDP_ISP_RX0_RCAL_NEG	CN24	LPDPRX0_RCAL_N
	ANALOG_LPDP_ISP_RX1_RCAL_POS	CN38	LPDPRX1_RCAL_P
	ANALOG_LPDP_ISP_RX1_RCAL_NEG	CP38	LPDPRX1_RCAL_N

R1200 200 1% 1/32W MF 01005 ROOM=SOC
C1200 10PF 5% 16V NP0/C0G 01005 ROOM=SOC
R1210 200 1% 1/32W MF 01005 ROOM=SOC
C1210 10PF 5% 16V NP0/C0G 01005 ROOM=SOC

LPDPRX-GPIO

	NC_LPDP_ISP_AUX_RX_D0P	CL22	LPDPRX_AUX_D0_P
	NC_LPDP_ISP_AUX_RX_D1P	CK24	LPDPRX_AUX_D1_P
	LPDP_ISP_BI_SWIDE_AUX_RX_D2P	CL26	LPDPRX_AUX_D2_P
	NC_LPDP_ISP_AUX_RX_D3P	CK28	LPDPRX_AUX_D3_P
	NC_LPDP_ISP_AUX_RX_D4P	CL30	LPDPRX_AUX_D4_P
	NC_LPDP_ISP_AUX_RX_D5P	CK32	LPDPRX_AUX_D5_P
	NC_LPDP_ISP_AUX_RX_D6P	CL34	LPDPRX_AUX_D6_P
	NC_LPDP_ISP_AUX_RX_D7P	CK36	LPDPRX_AUX_D7_P
	NC_LPDP_ISP_AUX_RX_D8P	CL38	LPDPRX_AUX_D8_P
	NC_LPDP_ISP_AUX_RX_D9P	CK40	LPDPRX_AUX_D9_P
	NC_LPDP_ISP_AUX_RX_D10P	CL42	LPDPRX_AUX_D10_P
	NC_LPDP_ISP_AUX_RX_D11P	CK43	LPDPRX_AUX_D11_P

I2C

ISP_I2C0_SCL	NC_I2C0_ISP_SCL	CL58	17
ISP_I2C0_SDA	NC_I2C0_ISP_SDA	CL57	17
ISP_I2C1_SCL	NC_I2C1_ISP_SCL	CM6	17
ISP_I2C1_SDA	NC_I2C1_ISP_SDA	CM4	17

PP (dev board only)

R1250 200 1% 1/32W MF 01005 ROOM=SOC

MIPI-C

MIPI0C_DPCLK	90_MIPI_ISP_FROM_IRCAM_CLK_P (CPU到红外相机LDPD总线时钟P)	CP60	82
MIPI0C_DNCLK	90_MIPI_ISP_FROM_IRCAM_CLK_N (CPU到红外相机LDPD总线时钟N)	CN60	82
MIPI0C_DPDATA0	90_MIPI_ISP_FROM_IRCAM_D0_P (CPU到红外相机LDPD总线0组数据P)	CN58	BI 82
MIPI0C_DNDATA0	90_MIPI_ISP_FROM_IRCAM_D0_N (CPU到红外相机LDPD总线0组数据N)	CP58	BI 82
MIPI0C_DPDATA1	90_MIPI_ISP_FROM_IRCAM_D1_P (CPU到红外相机LDPD总线1组数据P)	CN59	82
MIPI0C_DNDATA1	90_MIPI_ISP_FROM_IRCAM_D1_N (CPU到红外相机LDPD总线1组数据N)	CP59	82
MIPI0C_REXT	ANALOG_MIPI_ISP_REXT (CPU管理红外相机模块基准设定信号)	CL55	

GPIO

ISP_GPIO_0	GPIO_ISP_TO_CAM_PMU1_CAM_PMU2_RESET_L (CPU到相机电源1电源2的复位信号)	CK59	OUT 43 46
ISP_GPIO_1	NC_ISP_GPIO_1	CM7	20
ISP_GPIO_2	NC_ISP_GPIO_2	CL59	20
ISP_GPIO_3	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG (CPU输出的同步信号)	CN5	OUT 70 75 98

External flash trigger:
Kraken sends signal to Lightning accessory

SENSOR CLK

SENSOR0_CLK	CLK_ISP_TO_CAM_PMU1_24M_R (R1240 33.2 1% 1/32W MF 01005 ROOM=SOC)	AL2	CLK_ISP_TO_CAM_PMU1_24M (CPU到相机电源1的24M时钟) OUT 43
SENSOR1_CLK	CLK_ISP_TO_CAM_PMU2_24M_R (R1260 33.2 1% 1/32W MF 01005 ROOM=SOC)	AN4	CLK_ISP_TO_CAM_PMU2_24M (CPU到相机电源2的24M时钟) OUT 46
SENSOR2_CLK	NC_SENSOR2_CLK_AP	AN3	20
SENSOR3_CLK	NC_SENSOR3_CLK_AP	AR3	20

PACK_OPTION=D53,D54,DEV
BOMOPTION=PRO

SYNCING: D52, D53, D54, DEV

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SOC: DISPLAY / ISP

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 5 OF 21
OMIT_TABLE

CPU到显示屏数据时钟P	OUT	90 MIPI_AP_TO_DISPLAY_CLK_P	CN51	MIPID_DPCLK	ISP_SPMI	ISP_SPMI0_SCLK BJ4 SPMI_ISP_TO_CAM_PMU1_CLK (CPU到相机电源1 SPMI总线时钟) OUT 43
CPU到显示屏数据时钟N	OUT	90 MIPI_AP_TO_DISPLAY_CLK_N	CP51	MIPID_DNCLK		ISP_SPMI0_SDATA BJ2 SPMI_ISP_BI_CAM_PMU1_DATA (CPU到相机电源1 SPMI总线数据) BI 43 97
CPU到显示屏0组数据P	OUT	90 MIPI_AP_TO_DISPLAY_D0_P	CN55	MIPID_DPDATA0		ISP_SPMI1_SCLK BK2 SPMI_ISP_TO_CAM_PMU2_CLK (CPU到相机电源2 SPMI总线时钟) OUT 46
CPU到显示屏0组数据N	OUT	90 MIPI_AP_TO_DISPLAY_D0_N	CP55	MIPID_DNDATA0		ISP_SPMI1_SDATA BJ3 SPMI_ISP_BI_CAM_PMU2_DATA (CPU到相机电源2 SPMI总线数据) BI 46 97
CPU到显示屏1组数据P	OUT	90 MIPI_AP_TO_DISPLAY_D1_P	CP53	MIPID_DPDATA1	DWI	1.8V DWI_CLK CM3 NC_SOC_DWI_CLK 20
CPU到显示屏1组数据N	OUT	90 MIPI_AP_TO_DISPLAY_D1_N	CN53	MIPID_DNDATA1		DWI_DO CK5 NC_SOC_DWI_DATA 20
CPU到显示屏2组数据P	OUT	90 MIPI_AP_TO_DISPLAY_D2_P	CP47	MIPID_DPDATA2	MIPI-D	DISP_TOUCH_BSYNC0 CM11 NC_TOUCH_BSYNC0_DISP 21
CPU到显示屏2组数据N	OUT	90 MIPI_AP_TO_DISPLAY_D2_N	CN47	MIPID_DNDATA2		DISP_TOUCH_BSYNC1 CN6 NC_TOUCH_BSYNC1_DISP 20
CPU到显示屏3组数据P	OUT	90 MIPI_AP_TO_DISPLAY_D3_P	CN49	MIPID_DPDATA3		DISP_TOUCH_EB CM9 NC_SOC_DISP_TOUCH_EB 20
CPU到显示屏3组数据N	OUT	90 MIPI_AP_TO_DISPLAY_D3_N	CP49	MIPID_DNDATA3		DISP_TE F34 IO_AOP_FROM_DISPLAY_TE (CPU到显示屏的显示数据同步信号) IN 87 90
ANALOG_MIPI_AP_REXT (CPU管理显示模块设定信号)			CL53	MIPID_REXT		DISP_MIPI_PWR_DWN D47 IO_AOP_TO_DISPLAY_MIPI_PWR_DWN (CPU到显示屏的开启信号) OUT 87 90
						DISP_HPD CK61 NC_EDP_HPD_DISP 20
						DISP_I2C_SCL CL13 NC_SOC_DISP_I2C_SCL 20
						DISP_I2C_SDA CL60 NC_SOC_DISP_I2C_SDA 20
						DISP_POL CL62 NC_SOC_DISP_POL 20
						DISP_AGPIO D45 NC_SOC_DISP_AGPIO 20
						DISP_EXT_HPD BG3 NC_SOC_DISP_EXT_HPD 20
						DP_WAKEUP CK17 NC_DEV_SOC_DP_WAKEUP 21

R1300 200 1% 1/32W MF 01005 800MHz@DC

Dev breaks out to baseboard LPDP header

20	NC_DEV_LPDP_AP_TX0P	A40	LPDP_TX0P
20	NC_DEV_LPDP_AP_TX0N	B40	LPDP_TX0N
20	NC_DEV_LPDP_AP_TX1P	A42	LPDP_TX1P
20	NC_DEV_LPDP_AP_TX1N	B42	LPDP_TX1N
20	NC_DEV_LPDP_AP_TX2P	A43	LPDP_TX2P
20	NC_DEV_LPDP_AP_TX2N	B43	LPDP_TX2N
20	NC_DEV_LPDP_AP_TX3P	A45	LPDP_TX3P
20	NC_DEV_LPDP_AP_TX3N	B45	LPDP_TX3N
20	NC_DEV_LPDP_AP_AUXP	A47	LPDP_AUX_P
20	NC_DEV_LPDP_AP_AUXN	B47	LPDP_AUX_N
20	NC_DEV_LPDP_AP_RCALP	A49	LPDP_RCAL_P
20	NC_DEV_LPDP_AP_RCALN	B49	LPDP_RCAL_N

LPDP_RCAL_P/N are for LPDP TX, NC if unused

External LPDP not used

20	NC_LPDP_EXT_AP_TX0_P	A53	LPDP_EXT_TX0P
20	NC_LPDP_EXT_AP_TX0_N	B53	LPDP_EXT_TX0N
20	NC_LPDP_EXT_AP_TX1_P	A55	LPDP_EXT_TX1P
20	NC_LPDP_EXT_AP_TX1_N	B55	LPDP_EXT_TX1N
20	NC_LPDP_EXT_AP_TX2_P	A57	LPDP_EXT_TX2P
20	NC_LPDP_EXT_AP_TX2_N	B57	LPDP_EXT_TX2N
20	NC_LPDP_EXT_AP_TX3_P	A58	LPDP_EXT_TX3P
20	NC_LPDP_EXT_AP_TX3_N	B58	LPDP_EXT_TX3N
20	NC_LPDP_EXT_AP_AUX_P	A59	LPDP_EXT_AUX_P
20	NC_LPDP_EXT_AP_AUX_N	B59	LPDP_EXT_AUX_N
20	NC_LPDP_EXT_AP_RCAL_P	A60	LPDP_EXT_RCAL_P
20	NC_LPDP_EXT_AP_RCAL_N	B60	LPDP_EXT_RCAL_N

LPDP-TX

GPIOS

DISPLAY_TE also provides WDG functionality

PP (dev board only)

SPMI Address Map

BUS	DEVICE	ADDR	LOCATION
SPMI0 ISP	Adams1	0x09	Top MLB
SPMI1 ISP	Adams2	0x09	Top MLB

NOTE: SPMI1 ISP is for D53P/D54 only

SYNCING: D52, D53, D54, DEV

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PAGE TITLE
SOC: Display

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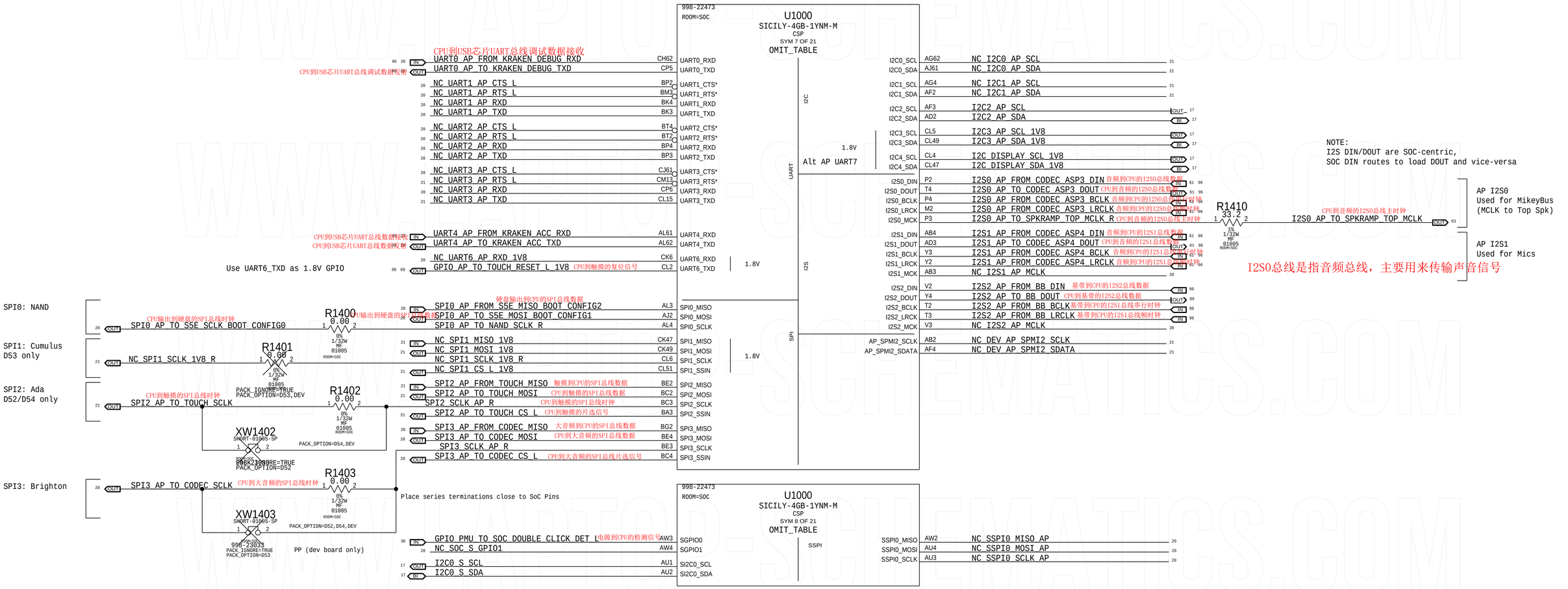
SOC: AP Serial



SYNCING: D52, D53, D54, DEV

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SOC: AP GPIO

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
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OMIT_TABLE
GPIO

19	GPIO_BOARD_REV3	版本识别3	BT3	GPIO0	
19	GPIO_BOARD_REV2	版本识别2	BV2	GPIO1	
19	GPIO_BOARD_REV1		BY2	GPIO2	
19	GPIO_BOARD_REV0		BV3	GPIO3	
19	GPIO_AP_CANARY1		BY3	GPIO4	
19	GPIO_AP_CANARY2		BY4	GPIO5	
19	GPIO_AP_BI_CCG2B_SWDIO	CPU到快充芯片SWD总线数据	CK58	GPIO6	
19	GPIO_AP_TO_CCG2B_SWCLK	CPU到快充芯片SWD总线时钟	CL11	GPIO7	
19	GPIO_AP_FROM_DISPLAY_PANEL_ID	CPU到显示屏ID识别信号	CM5	GPIO8	
19	GPIO_AP_FROM_WLAN_TIME_SYNC	CPU到WIFI的时间同步信号	CK15	GPIO9	
19	GPIO_AP_TO_BB_PEAK_PWR_IND		CN9	GPIO10	
19	GPIO_AP_TO_BB_COREDUMP	CPU到基带的纠错信号	CP7	GPIO11	
19	GPIO_AP_FROM_BB_RESET_DETECT_L	CPU到基带的复位检测	CK19	GPIO12	
19	GPIO_AP_FROM_CODEC_INT_L	CPU到音频的中断信号	CL17	GPIO13	
19	NC_AP_GPIO14		CJ60	GPIO14	
19	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	CPU到听筒功放的复位信号	BC62	GPIO15	

GPIO16	BC61	GPIO_AP_FROM_BT_AUDIO_SYNC	CPU到蓝牙声音同步信号	19
GPIO17	BC60	GPIO_AP_TO_AMUX_PMU_SYNC	CPU到电源数模转换同步信号	19
GPIO18	AW62	NC_DEV_AP_GPIO18		19
GPIO19	AW61	NC_DEV_AP_GPIO19		19
GPIO20	AW60	NC_DEV_AP_GPIO20		19
GPIO21	AU62	NC_DEV_AP_GPIO21		19
GPIO22	AU61	NC_DEV_AP_GPIO22		19
GPIO23	AU60	NC_DEV_AP_GPIO23		19
GPIO24	AR62	NC_DEV_AP_GPIO24		19
GPIO25	AR61	GPIO_AP_TO_BB_TIME_MARK	CPU到基带时间标记信号	19
GPIO26	AN61	NC_DEV_AP_GPIO26		19

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: GPIO
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SOC: AOP

NOTE:
I2S DIN/DOUT are SOC-centric,
SOC DIN routes to load DOUT and vice-versa

CPU到陀螺仪 U1芯片SPI总线时钟
SPI0_AOP_TO_IMU_R1_SCLK
R1601 33.2 1% 1/32W MF 01005 ROOM=SOC

R1603 33.2 1% 1/32W MF 01005 ROOM=SOC

AOP I2S0
Penrose, LDCM,
Borealis
(MCLK to Codec)

I2S0_AOP_TO_CODEC_MCLK1 CPU逻辑模块到音频的I2S0总线主时钟

音频到CPU逻辑模块的I2S1总线数据
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN
R1606 0.00 0% 1/32W MF 01005 ROOM=SOC

AOP I2S1
Out to BotSpk,
TopSpk, Arc,
in from Sak.
(MCLK to Arc
and BotSpk)

CPU逻辑模块到音频的I2S1总线数据
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT
R1607 0.00 0% 1/32W MF 01005 ROOM=SOC

CPU逻辑模块到音频的I2S1总线主时钟
I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK
R1608 0.00 0% 1/32W MF 01005 ROOM=SOC

CPU到蓝牙WIFI NFC的SPMI总线时钟
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
R1622 33.2 1% 1/32W MF 01005 ROOM=SOC

SPMI Address Map

BUS	DEVICE	ADDR	LOCATION
SPMI0 AOP	WLAN	0x0E	Bottom MLB
SPMI0 AOP	Ceres (P)	0x0C	D52/D53: Top MLB D54: Bottom MLB
SPMI0 AOP	Ceres (F)	0x0B	D53/D54: Top MLB D52: Bottom MLB

NOTE: Ceres (F) default address is 0x0C, programmed to 0x0B on SMT line

BUS	DEVICE	ADDR	LOCATION
SPMI0 NUB	Cota	0x0F	Top MLB
SPMI0 NUB	DotaraLV	0x0E	Top MLB

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 9 OF 21
OMIT_TABLE

I2C0_AOP_SCL	F61	AOP_I2CM0_SCL	I2C
I2C0_AOP_SDA	F62	AOP_I2CM0_SDA	
I2C1_AOP_SCL	F45	AOP_I2CM1_SCL	
I2C1_AOP_SDA	D42	AOP_I2CM1_SDA	
SPI0_AOP_FROM_IMU_R1_MISO CPU到陀螺仪 U1芯片SPI总线数据输出	H60	AOP_SPI0_MISO	SPI
SPI0_AOP_TO_IMU_R1_MOSI CPU到陀螺仪 U1芯片SPI总线数据输入	H62	AOP_SPI0_MOSI	
SPI0_AOP_TO_IMU_R1_SCLK_R CPU到陀螺仪 U1芯片SPI总线时钟	G62	AOP_SPI0_SCLK	
SPI1_SCLK/SSIN: Use as AOP GPIO			
I2C2_AOP_SCL	D55	AOP_SPI1_MISO	AOP I2C2 SCL
I2C2_AOP_SDA	D57	AOP_SPI1_MOSI	AOP I2C2 SDA
GPIO_AOP_TO_WLAN_CONTEXT_B	D58	AOP_SPI1_SCLK	
GPIO_AOP_TO_WLAN_CONTEXT_A	E34	AOP_SPI1_SSIN	
I2S0_AOP_FROM_CODEC_ASP1_DIN音频到CPU逻辑模块的I2S0总线数据	D59	AOP_I2S0_DIN	GPIO
I2S0_AOP_TO_CODEC_ASP1_DOUT CPU逻辑模块到音频的I2S0总线数据	E49	AOP_I2S0_DOUT	
I2S0_AOP_FROM_CODEC_ASP1_BCLK CPU逻辑模块到音频的I2S0总线串行时钟	D36	AOP_I2S0_BCLK	
I2S0_AOP_FROM_CODEC_ASP1_LRCLK CPU逻辑模块到音频的I2S0总线帧时钟	E36	AOP_I2S0_LRCK	
I2S0_AOP_TO_CODEC_MCLK1_R CPU逻辑模块到音频的I2S0总线主时钟	F36	AOP_I2S0_MCK	
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_R	C36	AOP_I2S1_DIN	I2S
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT_R_SOC	B36	AOP_I2S1_DOUT	
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK	E53	AOP_I2S1_BCLK	
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK CPU逻辑模块到音频的I2S1总线帧时钟	E51	AOP_I2S1_LRCK	
I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK_R	E47	AOP_I2S1_MCK	
UART1_AOP_FROM_BB_RXD CPU到基带的UART1总线数据接收	K62	AOP_SPMI1_SDATA	SUPPORTS UART
UART1_AOP_TO_BB_TXD CPU到基带的UART1总线数据发射	G61	AOP_SPMI1_SCLK	ALT FUNC1
SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA CPU到蓝牙WIFI NFC的SPMI总线数据	D43	AOP_SPMI0_SDATA	SUPPORTS UART
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK_R	F47	AOP_SPMI0_SCLK	ALT FUNC1
UART2_AOP_FROM_TOUCH_RXD CPU到触摸的UART总线接收	G60	AOP_UART2_RXD	UART
UART2_AOP_TO_TOUCH_TXD CPU到触摸的UART总线发射	E45	AOP_UART2_TXD	

CPU到陀螺仪中断信号

AOP_FUNC0	E62	GPIO_SCM_AOP_FROM_IMU_DATARDY
AOP_FUNC1	F60	GPIO_SCM_AOP_TO_IMU_SPI_CS_L CPU到陀螺仪SPI总线片选信号
AOP_FUNC2	E43	GPIO_AOP_FROM_PEARL_B2B_DETECT 点阵到CPU的插入检测信号
AOP_FUNC3	E60	NC_DEV_AOP_FUNC3
AOP_FUNC4	K61	GPIO_SCM_AOP_FROM_R1_INT CPU到U1超带宽芯片的中断信号
AOP_FUNC5	D60	GPIO_AOP_TO_R1_COREDUMP_TRIGGER CPU到U1超带宽芯片的纠错信号
AOP_FUNC6	D62	GPIO_AOP_TO_R1_TIME_SYNC_L CPU到U1超带宽芯片的时间同步信号
AOP_FUNC7	A36	GPIO_AOP_TO_CODEC_RESET_L CPU到音频芯片复位信号
AOP_FUNC8	E42	GPIO_AOP_TO_BB_FORCE_PWM CPU到基带强制调节信号
AOP_FUNC9	E59	GPIO_AOP_FROM_IRCAM_B2B_DETECT 红外相机到CPU插入检测信号
AOP_FUNC10	F57	GPIO_SCM_AOP_TO_R1_SPI_CS_L CPU到U1超带宽芯片的片选信号
AOP_FUNC11	F42	NC_AOP_FUNC11
AOP_FUNC12	D40	GPIO_AOP_TO_ALS_COEX
AOP_FUNC13	F58	GPIO_AOP_TO_NFC_IRONMAN_EN CPU到NFC的开启信号
AOP_FUNC14	F53	NC_GPIO_AOP_FROM_TOUCH_CTS
AOP_FUNC15	E58	GPIO_SCM_AOP_BI_PROX_INT_L CPU到感距中断信号
AOP_FUNC16	E40	GPIO_SCM_AOP_FROM_ALS_INT_L CPU到感光中断信号
AOP_FUNC17	F51	GPIO_SCM_AOP_FROM_EIGER_INT_L
AOP_FUNC18	E57	GPIO_SCM_AOP_FROM_COMPASS_INT CPU到指南针中断信号
AOP_FUNC19	F40	GPIO_SCM_AOP_FROM_JARVIS_INT
AOP_FUNC20	D38	GPIO_AOP_FROM_TOUCH_INT_L CPU到触摸中断信号
AOP_FUNC21	E55	NC_AOP_FUNC21
AOP_FUNC22	E38	NC_DEV_AOP_FUNC22

Touch UART
D52/D54: WIRED TO ADA
D53: WIRED TO TOUCH B2B

R1621 1.00M 5% 1/32W MF 01005
R1620 1.00M 5% 1/32W MF 01005

SOC: SMC

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 10 OF 21
OMIT_TABLE

I2C0_SMC_SCL	G4	SMC_I2CM0_SCL	I2C
I2C0_SMC_SDA	F26	SMC_I2CM0_SDA	
I2C1_SMC_SCL	G2	SMC_I2CM1_SCL	
I2C1_SMC_SDA	H2	SMC_I2CM1_SDA	
I2C2_SMC_SCL	G3	SMC_I2CM2_SCL	
I2C2_SMC_SDA	F2	SMC_I2CM2_SDA	

SOC: NUB

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 11 OF 21
OMIT_TABLE

SPMI0_NUB_TO_PMU_DOTARA_CLK_R	D32	NUB_SPMI0_SCLK	SPMI
SPMI0_NUB_BI_PMU_DOTARA_DATA	D4	NUB_SPMI0_SDATA	
SWD_NUB_TO_PMU_TOUCH_SWCLK CPU到电源和触摸电源的SPMI总线时钟	F6	NUB_SWD_TCK_OUT0	SWD
SWD_NUB_BI_PMU_SWDIO CPU到电源的SPMI总线数据	F13	NUB_SWD_TMS0	
SWD_NUB_BI_TOUCH_SWDIO	F11	NUB_SWD_TMS1	
IO_NUB_FROM_KRAKEN_DOCK_CONNECT USB到CPU的供电插入检测信号	F30	NUB_DOCK_CONNECT	DOCK
IO_NUB_FROM_KRAKEN_INT USB到CPU的中断信号	E30	NUB_DOCK_ATTENTION	
GPIO_NUB_FROM_CCG2B_INT_L 快充芯片到CPU的中断信号	D2	NUB_GPIO_0	GPIO
GPIO_NUB_FROM_GECKO_IRQ_L附件供电芯片到CPU的中断请求信号	E4	NUB_GPIO_1	
GPIO_NUB_FROM_PARROT_INT_L USB数据转换芯片到CPU的中断信号	E3	NUB_GPIO_2	
GPIO_NUB_TO_GECKO_RESET_L CPU到附件供电芯片复位信号	F28	NUB_GPIO_3	
GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA CPU到基带电源时钟开启信号	E2	NUB_GPIO_4	
NC_NUB_GPIO5	F3	NUB_GPIO_5	
NC_NUB_GPIO6	E28	NUB_GPIO_6	
SWD_DOCK_TO_AP_SWCLK USB到CPU的SWD总线时钟	E5	JTAG_TCK	JTAG
SWD_DOCK_BI_AP_SWDIO USB到CPU的SWD总线数据	C34	JTAG_TMS	
GND	D6	JTAG_SEL	
NC_DEV_JTAG_TDI	B34	JTAG_TDI	
NC_DEV_JTAG_TDO	E6	JTAG_TDO	
NC_DEV_JTAG_TRST_L	D5	JTAG_TRST*	
90_EUSB_DBG_PARROT_BI_AP_N 到数据转换芯片测试数据	B30	DBG_USB_EDM	DEBUG USB
90_EUSB_DBG_PARROT_BI_AP_P CPU到USB数据转换芯片测试数据P	A30	DBG_USB_EDP	
ANALOG_DBG_USB_RESREF CPU内部USB测试模块复位信号	D30	DBG_USB_RESREF	
PP1V2_S2	E32	DBG_PROBE_VALID	
IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	D51	COLD_RESET*	MISC
IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	D53	CFSB_AON	
CLK_PMU_TO_AOP_32K 电源到CPU的32KHz时钟	D49	RT_CLK32768	
IO_SOC_TO_PMU_WDOG_RESET CPU到电源的看门狗信号	D34	WDOG	
IO_AON_TO_AP_XTAL_CFSB CPU内部端口休眠唤醒信号	A34	AON_SLEEP1_RESET*	
	F15	NUB_CLK_OUT0	
GND	CP4	KIS_DFU_SELECT	

MLB: DBG_PROBE_VALID=1
DEV: Jumper for DBG_PROBE_VALID to 0 or 1

R1650 200 1% 1/32W MF 01005 ROOM=SOC

XW1660 SHORT-01005-SP
R1660 0.00 5% 1/32W MF 01005 ROOM=SOC
PACK_OPTION=D52
PACK_OPTION=D54,DEV

CLK_NUB_TO_TOUCH_24M
CLK_NUB_TO_TOUCH_24M_R

Touch SWDIO: Wired to Touch B2B (D52/D54)
Touch SWDIO: No connect (D53)

Gecko IRQ needs SOC weak internal PU
Parrot INT needs external or SOC pull-up

Can use Dotara GPIO for BBPMU Clock EN

KIS_DFU_SELECT:
POR = 0 (GND): USB0 for DFU (legacy)
Debug = 1 (1V2): USB1 for DFU (Kanzi-in-System)

SYNCING: D52, D53, D54, DEV

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DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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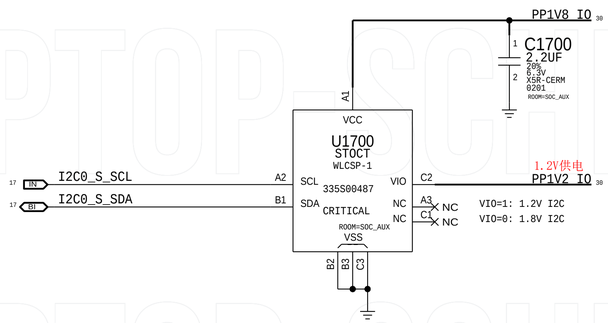
OCELOT



SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Ocelot
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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SOC: CPU/GPU

PP_CPU_PCORE — CPU核心供电

C1802 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1803 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1801 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1807 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1805 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
2020-MLCC 138S00317 ROOM=SOC_FILT C1804 11UF 20% 4V X5R 0402 ROOM=SOC_FILT C1806 14UF 20% 4V X5R 0402-D2X-1
ROOM=SOC_FILT C1805 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT C1807 14UF 20% 4V X5R 0402-D2X-1
PACK_OPTION=D54 ... PACK_OPTION=D54

PP_CPU_ECORE — CPU静态核心供电

C1895 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1894 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1893 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1891 14UF 20% 4V X5R 0402-D2X-1 / C1892 14UF 20% 4V X5R 0402-D2X-1 / C1893 14UF 20% 4V X5R 0402-D2X-1 PACK_OPTION=D54

PP_CPU_SRAM — CPU暂存供电

C1812 10UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1812 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D54
C1811 16UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT 2020-MLCC
C1808 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
2020-MLCC 138S00317 ROOM=SOC_FILT C1809 14UF 20% 4V X5R 0402-D2X-1 / C1810 11UF 20% 4V X5R 0402 / C1808 14UF 20% 4V X5R 0402-D2X-1 PACK_OPTION=D54

PP_SRAM_S1 — 暂存供电

138S00313 C1872 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D54 2020-MLCC
C1872 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1873 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1874 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1865 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53

998-22473 ROOM=SOC U1000 SICILY-4GB-1YNM-M CSP SYM 12 OF 21 OMIT_TABLE CPU/GPU

AP56	VDD_PCPU	VDD_GPU	AA27
AP48	VDD_PCPU	VDD_GPU	AA31
AP52	VDD_PCPU	VDD_GPU	AA44
AT41	VDD_PCPU	VDD_GPU	AA48
AT50	VDD_PCPU	VDD_GPU	AA52
AT54	VDD_PCPU	VDD_GPU	AC25
AV39	VDD_PCPU	VDD_GPU	AC33
AV54	VDD_PCPU	VDD_GPU	AC41
BF39	VDD_PCPU	VDD_GPU	AC50
BH54	VDD_PCPU	VDD_GPU	AE27
BL39	VDD_PCPU	VDD_GPU	AE35
BL48	VDD_PCPU	VDD_GPU	AE44
BL52	VDD_PCPU	VDD_GPU	AE48
BN37	VDD_PCPU	VDD_GPU	AE52
BN41	VDD_PCPU	VDD_GPU	N31
BN46	VDD_PCPU	VDD_GPU	N35
BN50	VDD_PCPU	VDD_GPU	N39
BN54	VDD_PCPU	VDD_GPU	N44
BR44	VDD_PCPU	VDD_GPU	R25
BR52	VDD_PCPU	VDD_GPU	R33
BU37	VDD_PCPU	VDD_GPU	R41
BU50	VDD_PCPU	VDD_GPU	R50
BW39	VDD_PCPU	VDD_GPU	U27
BW52	VDD_PCPU	VDD_GPU	U31
CA37	VDD_PCPU	VDD_GPU	U44
CA50	VDD_PCPU	VDD_GPU	U48
CC37	VDD_PCPU	VDD_GPU	U52
CC44	VDD_PCPU	VDD_GPU	W29
CC52	VDD_PCPU	VDD_GPU	W46
		VDD_GPU	AE31
BL37	VDD_PCPU_SENSE	VDD_GPU_SENSE	AH29
AT29	VDD_ECPU		
AT33	VDD_ECPU		
AT37	VDD_ECPU		
AV31	VDD_ECPU		
BB27	VDD_ECPU		
BD37	VDD_ECPU		
BF31	VDD_ECPU		
BF35	VDD_ECPU		
BH37	VDD_ECPU		
BL33	VDD_ECPU_SENSE		

ANALOG_PCPU_SENSE_P (OUT 96 24) — ANALOG_ECPU_SENSE_SE (OUT 96)

CPU集显供电 PP_GPU

C1831 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1832 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1833 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1834 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT

ANALOG_GPU_SENSE_P (OUT 96)

CPU内部微处理模块供电 PP_SOC_S1

C1860 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1861 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT PACK_OPTION=D54
C1830 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1862 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1863 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D54
138S00313 C1863 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV 2020-MLCC
C1864 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1866 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT

SOC: SOC

998-22473 ROOM=SOC U1000 SICILY-4GB-1YNM-M CSP SYM 13 OF 21 OMIT_TABLE SOC

AY25	VDD_SOC_S1	VDD_SOC_S1	BF56
AA14	VDD_SOC_S1	VDD_SOC_S1	BL18
AA18	VDD_SOC_S1	VDD_SOC_S1	BL23
AH20	VDD_SOC_S1	VDD_SOC_S1	BL31
AM54	VDD_SOC_S1	VDD_SOC_S1	BN20
AH37	VDD_SOC_S1	VDD_SOC_S1	BN29
AH46	VDD_SOC_S1	VDD_SOC_S1	AE14
AH54	VDD_SOC_S1	VDD_SOC_S1	BR18
AK10	VDD_SOC_S1	VDD_SOC_S1	BR23
AK14	VDD_SOC_S1	VDD_SOC_S1	BR27
AK18	VDD_SOC_S1	VDD_SOC_S1	BR31
AK23	VDD_SOC_S1	VDD_SOC_S1	BR35
AK27	VDD_SOC_S1	VDD_SOC_S1	BU25
AA23	VDD_SOC_S1	VDD_SOC_S1	BU33
AK31	VDD_SOC_S1	VDD_SOC_S1	BW35
AK35	VDD_SOC_S1	VDD_SOC_S1	CE44
AK39	VDD_SOC_S1	VDD_SOC_S1	CE52
AK44	VDD_SOC_S1	VDD_SOC_S1	AE18
AK48	VDD_SOC_S1	VDD_SOC_S1	CG18
AK52	VDD_SOC_S1	VDD_SOC_S1	CG29
AK56	VDD_SOC_S1	VDD_SOC_S1	N14
AM16	VDD_SOC_S1	VDD_SOC_S1	N18
AM25	VDD_SOC_S1	VDD_SOC_S1	N23
AM33	VDD_SOC_S1	VDD_SOC_S1	N27
AC16	VDD_SOC_S1	VDD_SOC_S1	N37
AM50	VDD_SOC_S1	VDD_SOC_S1	N56
AP10	VDD_SOC_S1	VDD_SOC_S1	R16
AP14	VDD_SOC_S1	VDD_SOC_S1	U14
BH25	VDD_SOC_S1	VDD_SOC_S1	AE23
AP23	VDD_SOC_S1	VDD_SOC_S1	U18
AP27	VDD_SOC_S1	VDD_SOC_S1	U23
AP31	VDD_SOC_S1	VDD_SOC_S1	W12
N46	VDD_SOC_S1	VDD_SOC_S1	W20
BL27	VDD_SOC_S1	VDD_SOC_S1	AH12
AT12	VDD_SOC_S1	VDD_SOC_S1	AP39
CA12	VDD_SOC_S1		
AT20	VDD_SOC_S1		
AV10	VDD_SOC_S1		
AV14	VDD_SOC_S1		
AV18	VDD_SOC_S1		
AV23	VDD_SOC_S1		
AY16	VDD_SOC_S1		
BB10	VDD_SOC_S1		
BB14	VDD_SOC_S1		
BB18	VDD_SOC_S1		
BB23	VDD_SOC_S1		
AE10	VDD_SOC_S1		
BD12	VDD_SOC_S1		
BD20	VDD_SOC_S1		
BF18	VDD_SOC_S1		
BF23	VDD_SOC_S1		
AP16	VDD_SOC_SENSE		

ANALOG_SOC_SENSE_P (OUT 96)

SOC: SRAM

998-22473 ROOM=SOC U1000 SICILY-4GB-1YNM-M CSP SYM 14 OF 21 OMIT_TABLE SRAM

AT46	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AH50
AV27	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM12
CC48	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM20
AV35	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM29
BB39	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM37
BD54	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AM46
BH33	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AT16
BL44	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AT25
BR39	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AY12
BR48	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	AY20
CC39	VDD_CPU_SRAM	VDD_SRAM_SOC_S1	BD16
		VDD_SRAM_SOC_S1	BD25
R29	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BH12
R37	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BH20
AC29	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN16
AC37	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN25
AC46	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN33
R46	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BN8
W25	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BU12
W33	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BU20
W50	VDD_SRAM_GPU_S1	VDD_SRAM_SOC_S1	BU29
		VDD_SRAM_SOC_S1	BU52
		VDD_SRAM_SOC_S1	CA16
		VDD_SRAM_SOC_S1	CA25
		VDD_SRAM_SOC_S1	CA33
		VDD_SRAM_SOC_S1	CE29
		VDD_SRAM_SOC_S1	CE50
		VDD_SRAM_SOC_S1	AC12
		VDD_SRAM_SOC_S1	AC20
		VDD_SRAM_SOC_S1	AH16
		VDD_SRAM_SOC_S1	AH25
		VDD_SRAM_SOC_S1	AH33
		VDD_SRAM_SOC_S1	AH41
		VDD_SRAM_SOC_S1	AM56
		VDD_SRAM_SOC_S1	L25
		VDD_SRAM_SOC_S1	N52
		VDD_SRAM_SOC_S1	R20
		VDD_SRAM_SOC_S1	U12
		VDD_SRAM_SOC_S1	W16

PP_SRAM_S1 — 暂存供电

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: Power (CPU/GPU & SRAM & SOC)
DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: crb-1
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SUBSYSTEM SPECIFIC BOM TABLES

2.2uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	(C1970)	CAP,CER,X5R,2.2UF,20%,6.3V,0201

SOC: FIXED

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 17 OF 21
OMIT_TABLE

FIXED

AP8	VDD_FIXED_S1
AV56	VDD_FIXED_S1
CA52	VDD_FIXED_S1
CE16	VDD_FIXED_S1
CG31	VDD_FIXED_S1
CG52	VDD_FIXED_MIPID_S1
CG56	VDD_FIXED_MIPIC_S1
CK55	VDD_FIXED_MIPID_PLL_S1
J20	VDD_FIXED_USB_S1
J52	VDD_FIXED_LPDP_TX_S1
J56	VDD_FIXED_LPDP_TX_S1
CE33	VDD_FIXED_LPDP_RX_S1
CE37	VDD_FIXED_LPDP_RX_S1
CE41	VDD_FIXED_LPDP_RX_S1
CE46	VDD_FIXED_LPDP_RX_S1
L16	VDD_FIXED_PCIE_S1
L20	VDD_FIXED_PCIE_S1
N16	VDD_FIXED_PCIE_S1
J12	VDD_FIXED_PCIE_REFBUF_S1
AP46	VDD_FIXED_PCPU_S1
AY39	VDD_FIXED_ECPU_S1
CF60	VDD_FIXED_MTR_S1
AE41	VDD_FIXED_PLL_GPU_S1
CE12	VDD_FIXED_PLL_DDR0_S1
BP60	VDD_FIXED_PLL_DDR1_S1
AC10	VDD_FIXED_PLL_DDR2_S1
P60	VDD_FIXED_PLL_DDR3_S1
BH27	VDD_FIXED_PLL_SOC_S1
CA35	VDD_FIXED_PLL_ANE_S1
F9	VDD_FIXED_XTAL_S1

PP0V78_SOC_FIXED_S1 — CPU内部微处理模块0.78V供电

C1901 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1907 220PF 5% 25V C0G 01005 ROOM=SOC_FILT
C1908 220PF 5% 25V C0G 01005 ROOM=SOC_FILT
C1909 220PF 5% 25V C0G 01005 ROOM=SOC_FILT
C1906 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1905 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1910 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

GND
(Not used for MLBs)

C1916 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1918 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1917 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1922 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1921 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1920 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

OMIT XW1940 SHORT-20L-0.05MM-SM 1 2 ROOM=SOC_FILT
C1940 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1941 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1942 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1902 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP0V78_VDD_FIXED_XTAL — VOLTAGE=0.8
R1970 20.0 5% 1/32W MF 01005 ROOM=SOC_FILT
C1970 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT [SS] MURATA

SOC: VDD12

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 18 OF 21
OMIT_TABLE

F22	VDD12_USB
F24	VDD12_USB_DEBUG_S2
AP44	VDD12_PLL_PCPU
AY37	VDD12_PLL_ECPU
AE39	VDD12_PLL_GPU
F7	VDD12_XTAL_S1
CL9	VDD12_AMUX_S2
CG54	VDD12_MIPIC
CK53	VDD12_MIPID_S1
AM41	VDD12_TSADC_CPU0
AT39	VDD12_TSADC_CPU1
AP35	VDD12_TSADC_SOC0
AC52	VDD12_TSADC_SOC1
R12	VDD12_TSADC_SOC2
J27	VDDIO12_AOP_S2
J31	VDDIO12_AOP_S2
J35	VDDIO12_AOP_S2
J39	VDDIO12_AOP_S2
J44	VDDIO12_AOP_S2
J48	VDDIO12_AOP_S2
BF27	VDD12_PLL_SOC_S1
BH29	VDD12_PLL_SOC_S1
CE14	VDDIO12_PLL_DDR0_S1
BM60	VDDIO12_PLL_DDR1_S1
AC8	VDDIO12_PLL_DDR2_S1
M60	VDDIO12_PLL_DDR3_S1
CC35	VDD12_PLL_ANE
CG12	VDDIO12_GRP1_S2
AY56	VDDIO12_GRP3
BD56	VDDIO12_GRP3
BL56	VDDIO12_GRP3
CG16	VDDIO12_GRP4
CG20	VDDIO12_GRP4
CG23	VDDIO12_GRP4
AH8	VDDIO12_GRP5
AM8	VDDIO12_GRP5
AT8	VDDIO12_GRP5
AY8	VDDIO12_GRP5
BD8	VDDIO12_GRP5
J14	VDD12_PCIE
J18	VDD12_PCIE
CH60	VDD12_MTR
L50	VDD12_LPDP_TX
L54	VDD12_LPDP_TX
CG35	VDD12_LPDP_RX
CG39	VDD12_LPDP_RX
CG44	VDD12_LPDP_RX
CG48	VDD12_LPDP_RX
CG37	VDD12_LPDP_RX
N50	VDD12_EFUSE1
W18	VDD12_EFUSE2
AM39	VDD12_EFUSE3
N48	VDD12_EFUSE4
AP37	VDD12_EFUSE5
R14	VDD12_FMON
L12	VDD12_PCIE_REFBUF
L33	VDD12_ULPPLL_S2
K60	VDD12_ADC_SOC_S1

PP1V2_IO 1.2V供电 — Place cap near pin
C1935 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S2 1.2V供电 — Place cap near pin
C1900 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

RADAR #: 54364908
PLACE NEAR SOC
OMIT XW1930 SHORT-20L-0.05MM-SM 1 2 ROOM=SOC_FILT

PP1V2_SOC 1.2V供电 — PP1V2_SOC_FILT — VOLTAGE=1.2
To ANE 14
Place 01005 caps near pins (incl. ANE)
C1926 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1927 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1928 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S1 1.2V供电
FL1950 240-OHM-25%-0.20A-1.0DCR 01005 ROOM=SOC_FILT 155S0755
PP1V2_S1_XTAL — VOLTAGE=1.2
C1946 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1903 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S2 1.2V供电
PP1V2_IO 1.2V供电
PP1V2_S1 1.2V供电
C1998 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1999 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1997 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1996 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_IO 1.2V供电
PP1V2_S2 1.2V供电 — Place cap near pins
C1923 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1924 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S1
C1963 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1964 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

PP1V2_S1 — Shares decap with other S1 rails

14 PP1V2_SOC_FILT — Share cap with VDD12_PLL_ECPU/_PCPU/_GPU

1.2V供电 PP1V2_S2 — [LAYOUT] VDDIO12_GRPx: Isolation >= 2.5nH from other nets on the same domain
C1904 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

PP1V2_IO_GRP3 — VOLTAGE=1.2
OMIT XW1901 SHORT-10L-0.1MM-SM 2 1 ROOM=SOC_FILT NO_XNET_CONNECTION
1.2V供电 PP1V2_IO
C1945 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

PP1V2_IO_GRP4 — VOLTAGE=1.2
OMIT XW1902 SHORT-10L-0.1MM-SM 2 1 ROOM=SOC_FILT NO_XNET_CONNECTION
1.2V供电 PP1V2_IO
C1947 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

1.2V供电 PP1V2_IO
C1948 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

1.2V供电 PP1V2_SOC
1.2V供电 PP1V2_SOC
C1937 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1955 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1950 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

GND

1.2V供电 PP1V2_IO
C1931 0.01UF 10% 6.3V X5R 01005 ROOM=SOC_FILT
C1932 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1933 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

Used for SoC fusing
GND on all systems

PP1V2_VDD12_FMON — VOLTAGE=1.2
49.9 R1960 1% MF 1/32W 01005 ROOM=SOC_FILT
1.2V供电 PP1V2_IO

PP1V2_VDD12_ULPPLL_S2 — VOLTAGE=1.2
49.9 R1961 1% MF 1/32W 01005 ROOM=SOC_FILT
PP1V2_SOC
PP1V2_S2
PP1V2_S1

C1938 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1995 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1936 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

[LAYOUT] VDD12_PCIE_REFBUF: Inductance from C1995.1 to PP1V2_SOC plane >1.5nH @ 100MHz

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Power (Fixed & 1V2)
DRAWING NUMBER	051-05170
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REVISION	10.0.0
BRANCH	crb-1
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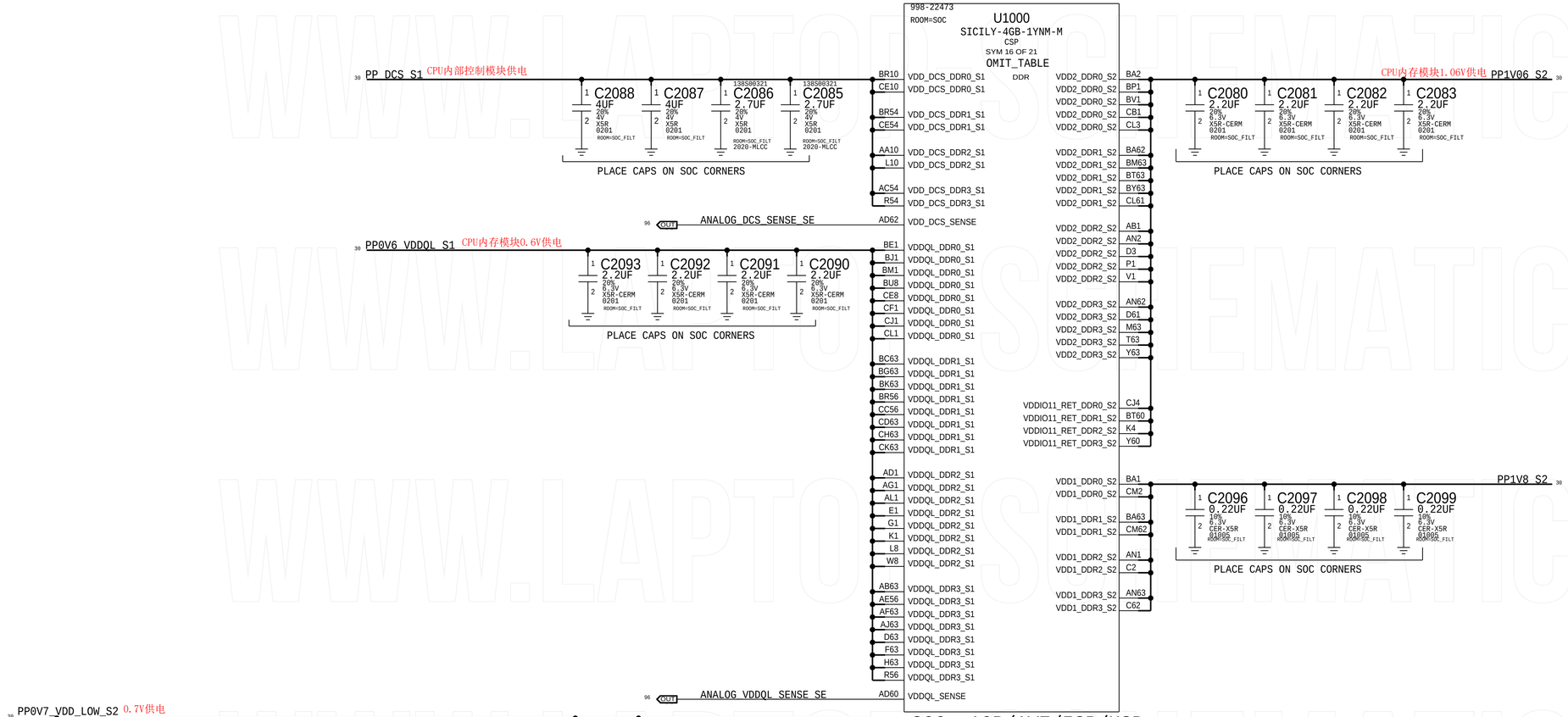
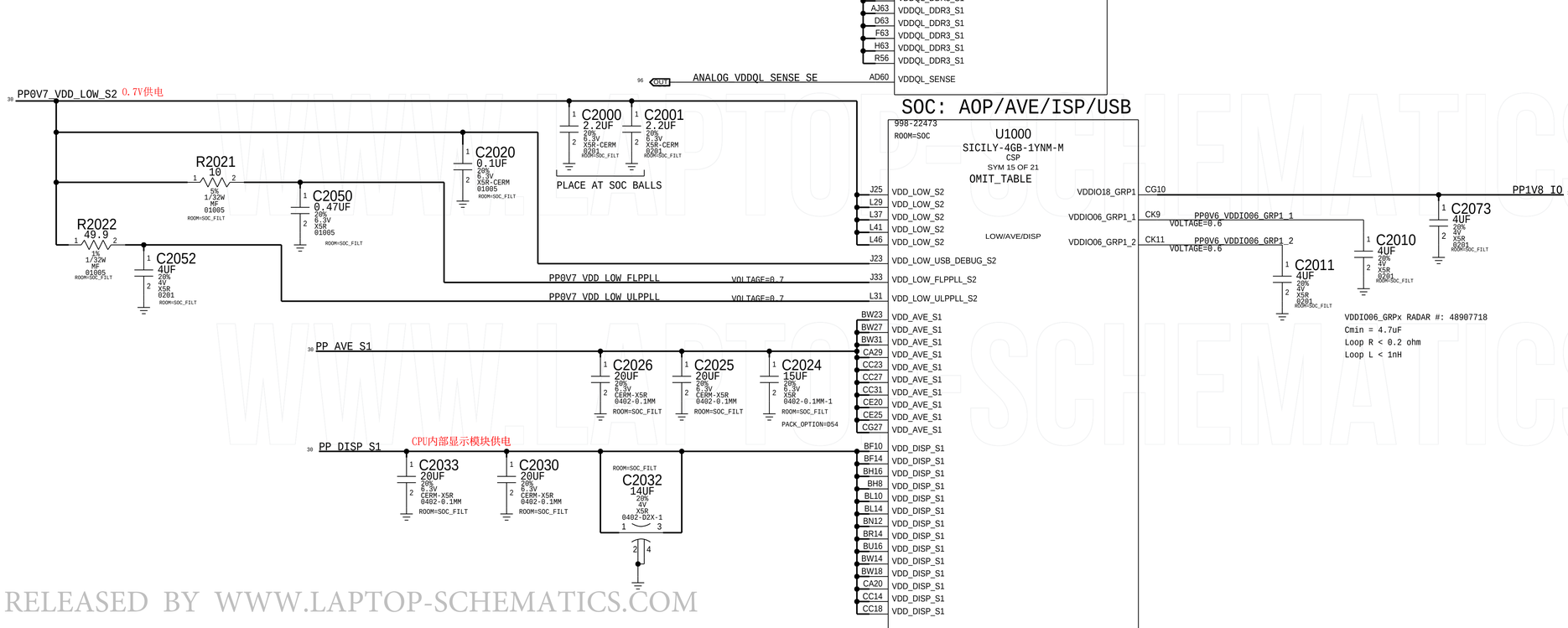
SOC: DDR



SOC: AOP/AVE/ISP/USB



SYNCING: D52, D53, D54, DEV

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PAGE TITLE	SOC: Power (DDR & AOP/AVE/ISP/USB)
DRAWING NUMBER	051-05170
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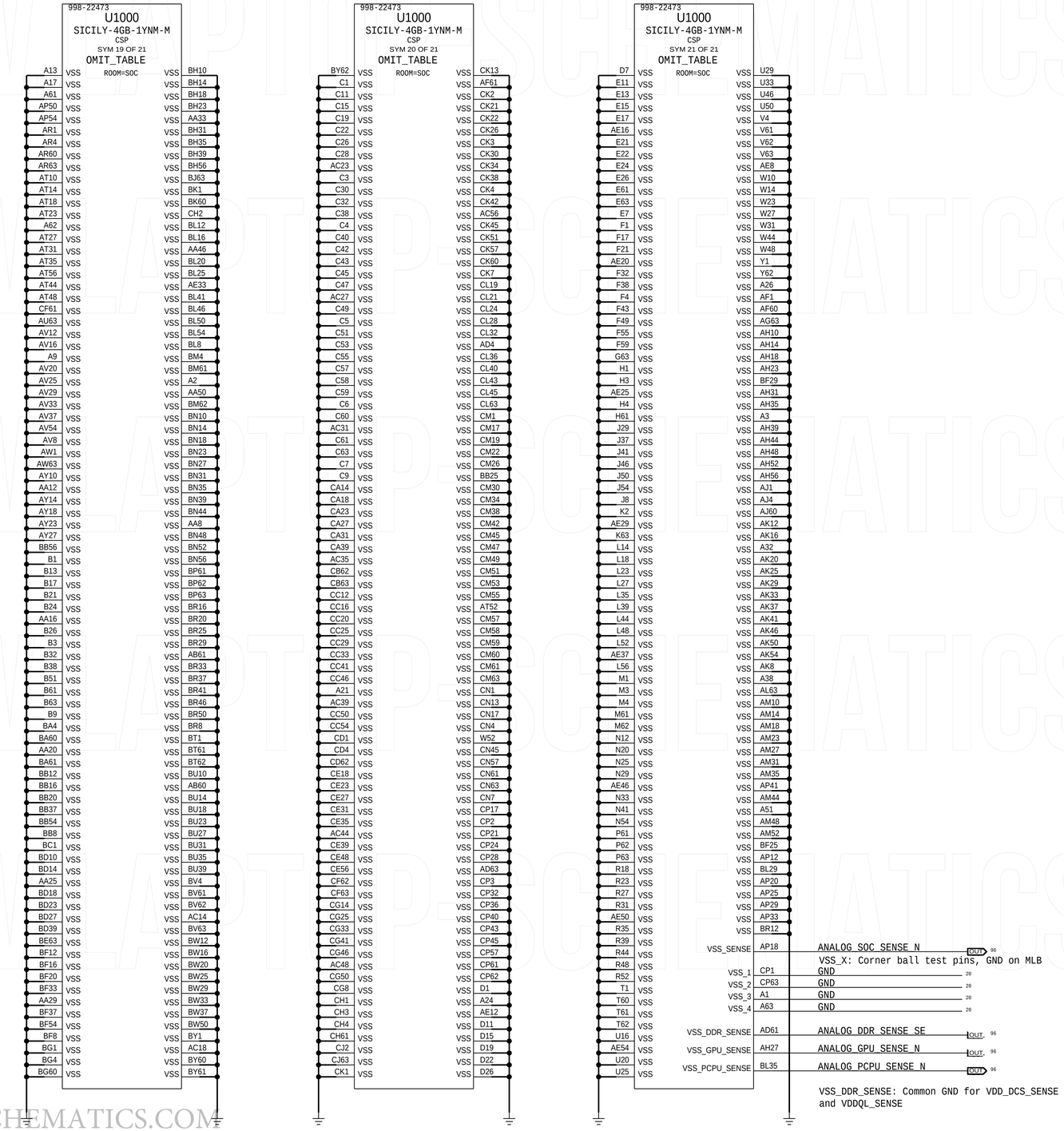
SOC: GND



SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Power (GND)
DRAWING NUMBER	051-05170
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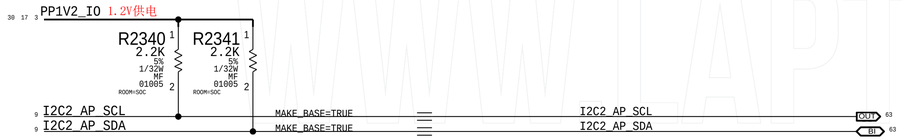
AP/ISP I2C

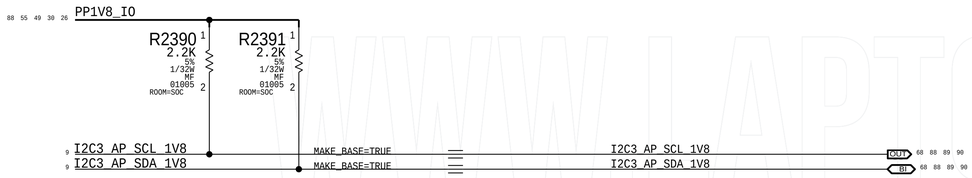
AP I2C0 (Unused)

AP I2C1 (Unused)

AP I2C2

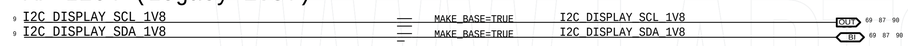


MASTER	AP	NUMBER	I2C2	DIAGS NUMBER	2	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Top Spk Amp	1.2V	0x40	0x80, 0x81	1MHz	MLB		



MASTER	AP	NUMBER	I2C3	DIAGS NUMBER	3	SPEED	400kHz	
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION			
Touch EEPROM	1.8V	0x51	0xA2, 0xA3	400kHz	Touch Flex			
Babbage (TFE)	1.8V	0x4B	0x96, 0x97	1MHz	Touch Flex	D52/D54 only		
NOTE: For D52/D54, bus can either be mastered by SoC or Ada								
Roswell	1.8V	0x10	0x20, 0x21	400kHz	Touch Flex	D53 only		
NOTE: Roswell is I2C for D53-only (AID for D52/D54)								

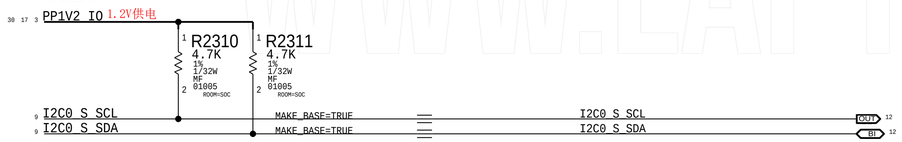
AP I2C4 (Legacy 1.8V)



MAKE_BASE for Display PMIC intentional, test feature only

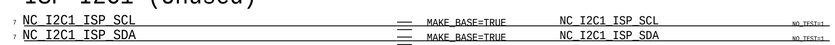
MASTER	AP	NUMBER	I2C4	DIAGS NUMBER	4	SPEED	400kHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Display PMIC	1.8V	0x50	0xA0, 0xA1	400kHz	MLB		
NOTE: SoC is master for FCT *ONLY*, DDIC is master for normal operation							

SI2C0



ISP I2C0

ISP I2C1 (Unused)



SYNCING: D52, D53, D54

PAGE TITLE
SOC: Aliases: I2C AP/ISP

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SIZE D
REVISION 10.0.0
BRANCH crb-1
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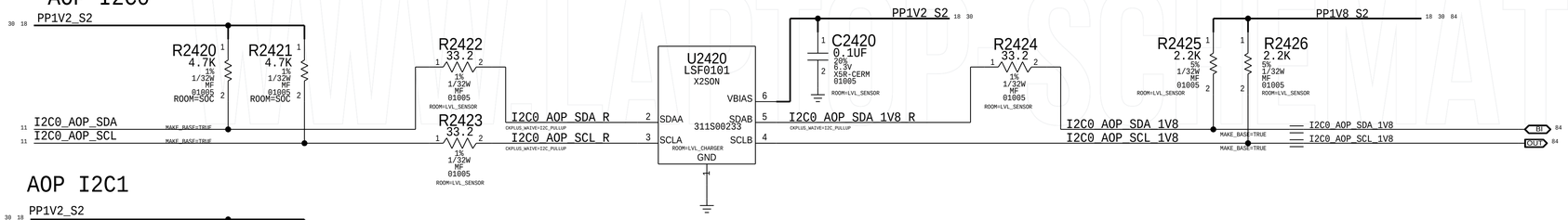
AOP/SMC I2C

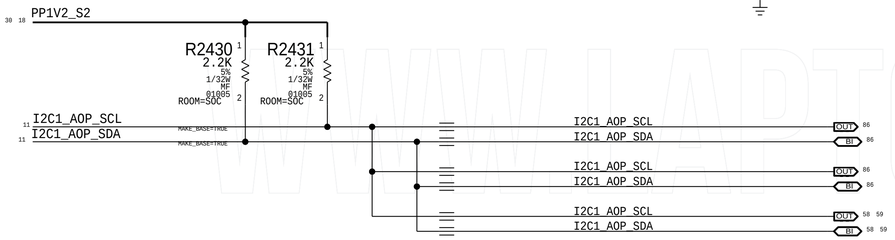
AOP I2C0



MASTER	AOP	NUMBER	I2C0	DIAGS NUMBER	5	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Prox	1.8V	0x58	0xB0, 0xB1	1MHz	Sensor Flex
ALS	1.8V	0x29	0x52, 0x53	1MHz	Sensor Flex
Grievous	1.8V	0x33	0x66, 0x67	1MHz	Sensor Flex
Compass	1.8V	0x0E	0x1C, 0x1D	1MHz	Sensor Flex

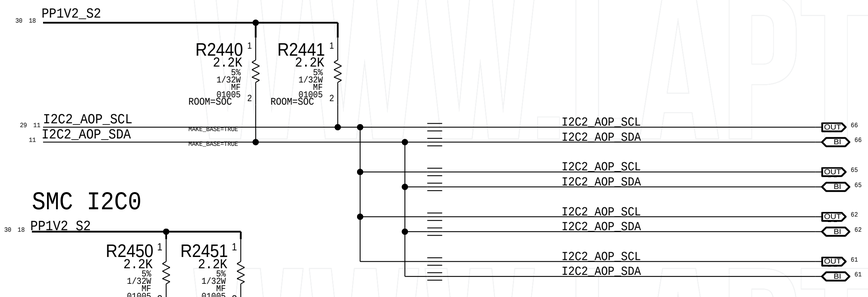
AOP I2C1



MASTER	AOP	NUMBER	I2C1	DIAGS NUMBER	6	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Eiger	1.2V	0x76	0xEC, 0xED	1MHz	Dock
Arc EEPROM	1.2V	0x50	0xA0, 0xA1	1MHz	Arc Flex
Jarvis	1.2V	0x0F	0x1E, 0x1F	1MHz	MLB

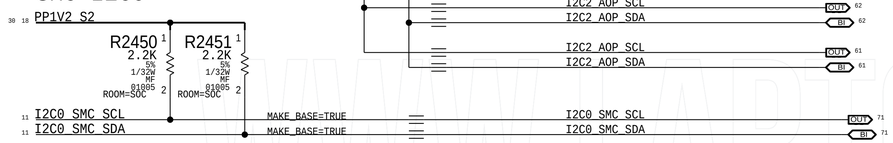
AOP I2C2



MASTER	AOP	NUMBER	I2C2	DIAGS NUMBER	7	SPEED	1MHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Sakonnet	1.2V	0x08	0x10, 0x11	1MHz	MLB
Codec	1.2V	0x4A	0x94, 0x95	1MHz	MLB
Arc Amp	1.2V	0x42	0x84, 0x85	1MHz	MLB
Bot Spk Amp	1.2V	0x40	0x80, 0x81	1MHz	MLB

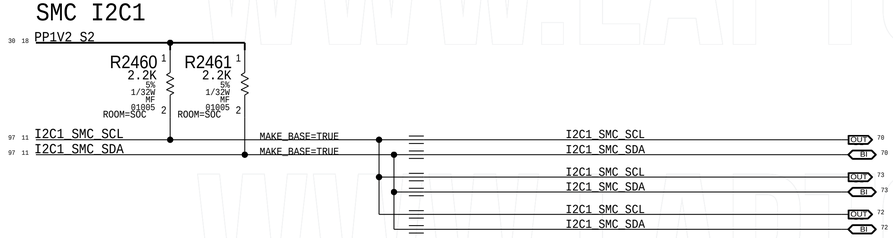
SMC I2C0



MASTER	SMC	NUMBER	I2C0	DIAGS NUMBER	8	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
CCG2B	1.2V	0x12	0x24, 0x25	1MHz	MLB

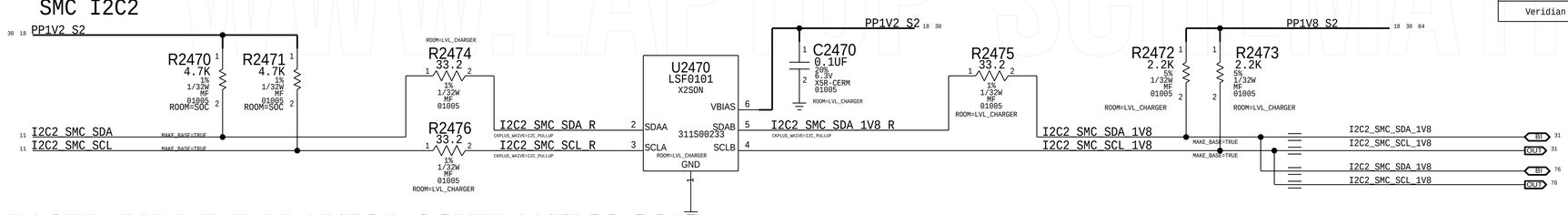
SMC I2C1



MASTER	SMC	NUMBER	I2C1	DIAGS NUMBER	9	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Kraken	1.2V	0x1A	0x34, 0x35	1MHz	MLB
Parrot	1.2V	0x21	0x42, 0x43	1MHz	MLB
Gecko2	1.2V	0x52	0xA4, 0xA5	1MHz	MLB

SMC I2C2



MASTER	SMC	NUMBER	I2C2	DIAGS NUMBER	10	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Yangtze	1.8V	0x71	0xE2, 0xE3	400kHz	MLB
Veridian	1.8V	0x0B	0x16, 0x17	400kHz	Battery Flex

SYNCING: D52, D53, D54

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BRANCH	crb-1
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AOP GPIOs

* All AOP GPIOs tie into SCM block

SPMI0	SPI	AOP_FUNC0
SPMI0	SPI	AOP_FUNC1
SPMI0	SPI	AOP_FUNC2
SPMI0	SPI	AOP_FUNC3
SPMI1	SPI	AOP_FUNC4
SPMI1	SPI	AOP_FUNC5
SPMI1	SPI	AOP_FUNC6
SPMI1	SPI	AOP_FUNC7
	SPI	AOP_FUNC8
	SPI	AOP_FUNC9
	SPI	AOP_FUNC10
	SPI	AOP_FUNC11
I2C0	SPI	AOP_FUNC12
I2C0	SPI	AOP_FUNC13
I2C0	SPI	AOP_FUNC14
I2C1, I2C0	SPI	AOP_FUNC15
I2C1	I2C0	AOP_FUNC16
I2C1	I2C0	AOP_FUNC17
I2C1	I2C0	AOP_FUNC18
	I2C1	AOP_FUNC19
	I2C1	AOP_FUNC20
	I2C1	AOP_FUNC21
	I2C1	AOP_FUNC22

11	GPIO_SCM_AOP_FROM_IMU_DATARDY	CPU到陀螺仪中断信号	=	GPIO_SCM_AOP_FROM_IMU_DATARDY	MAKE_BASE=TRUE IN 57
11	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	CPU到陀螺仪SPI总线片选信号	=	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	MAKE_BASE=TRUE OUT 57
11	GPIO_AOP_FROM_PEARL_B2B_DETECT	点阵到CPU的插入检测信号	=	GPIO_AOP_FROM_PEARL_B2B_DETECT	MAKE_BASE=TRUE IN 83
11	NC_DEV_AOP_FUNC3		=	NC_DEV_AOP_FUNC3	21
11	GPIO_SCM_AOP_FROM_R1_INT	CPU到U1超带宽芯片的中断信号	=	GPIO_SCM_AOP_FROM_R1_INT	MAKE_BASE=TRUE IN 101
11	GPIO_AOP_TO_R1_COREDUMP_TRIGGER		=	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	MAKE_BASE=TRUE OUT 101
11	GPIO_AOP_TO_R1_TIME_SYNC_L		=	GPIO_AOP_TO_R1_TIME_SYNC_L	MAKE_BASE=TRUE OUT 101
11	GPIO_AOP_TO_CODEC_RESET_L	CPU到音频芯片复位信号	=	GPIO_AOP_TO_CODEC_RESET_L	MAKE_BASE=TRUE OUT 61 96
11	GPIO_AOP_TO_BB_FORCE_PWM	CPU到基带强制调节信号	=	GPIO_AOP_TO_BB_FORCE_PWM	MAKE_BASE=TRUE OUT 99
11	GPIO_AOP_FROM_IRCAM_B2B_DETECT	红外相机到CPU插入检测信号	=	GPIO_AOP_FROM_IRCAM_B2B_DETECT	MAKE_BASE=TRUE IN 82
11	GPIO_SCM_AOP_TO_R1_SPI_CS_L		=	GPIO_SCM_AOP_TO_R1_SPI_CS_L	MAKE_BASE=TRUE OUT 101
11	NC_AOP_FUNC11		=	NC_AOP_FUNC11	20
11	GPIO_AOP_TO_ALS_COEX		=	GPIO_AOP_TO_ALS_COEX	MAKE_BASE=TRUE OUT 84
11	GPIO_AOP_TO_NFC_IRONMAN_EN	CPU到NFC的开启信号	=	GPIO_AOP_TO_NFC_IRONMAN_EN	MAKE_BASE=TRUE OUT 100
11	NC_GPIO_AOP_FROM_TOUCH_CTS		=	NC_GPIO_AOP_FROM_TOUCH_CTS	IN 21 88
11	GPIO_SCM_AOP_BI_PROX_INT_L	CPU到感距中断信号	=	GPIO_SCM_AOP_BI_PROX_INT_L	MAKE_BASE=TRUE IN 75
11	GPIO_SCM_AOP_FROM_ALS_INT_L	CPU到感光中断信号	=	GPIO_SCM_AOP_FROM_ALS_INT_L	MAKE_BASE=TRUE IN 84
11	GPIO_SCM_AOP_FROM_EIGER_INT_L		=	GPIO_SCM_AOP_FROM_EIGER_INT_L	MAKE_BASE=TRUE IN 86
11	GPIO_SCM_AOP_FROM_COMPASS_INT	CPU到指南针中断信号	=	GPIO_SCM_AOP_FROM_COMPASS_INT	MAKE_BASE=TRUE IN 75
11	GPIO_SCM_AOP_FROM_JARVIS_INT		=	GPIO_SCM_AOP_FROM_JARVIS_INT	MAKE_BASE=TRUE IN 58 59 96
11	GPIO_AOP_FROM_TOUCH_INT_L	CPU到触摸中断信号	=	GPIO_AOP_FROM_TOUCH_INT_L	MAKE_BASE=TRUE IN 68 88
11	NC_AOP_FUNC21		=	NC_AOP_FUNC21	20
11	NC_DEV_AOP_FUNC22		=	NC_DEV_AOP_FUNC22	21

AP GPIOs

AP_GPIO0	10	GPIO_BOARD_REV3	版本识别3	GPIO_BOARD_REV3	版本识别3 MAKE_BASE=TRUE IN 3
AP_GPIO1	10	GPIO_BOARD_REV2	版本识别2	GPIO_BOARD_REV2	版本识别2 MAKE_BASE=TRUE IN 3
AP_GPIO2	10	GPIO_BOARD_REV1		GPIO_BOARD_REV1	MAKE_BASE=TRUE IN 3
AP_GPIO3	10	GPIO_BOARD_REV0		GPIO_BOARD_REV0	MAKE_BASE=TRUE IN 3
AP_GPIO4	10	GPIO_AP_CANARY1		GPIO_AP_CANARY1	MAKE_BASE=TRUE IN 98
AP_GPIO5	10	GPIO_AP_CANARY2		GPIO_AP_CANARY2	MAKE_BASE=TRUE IN 98
AP_GPIO6	10	GPIO_AP_BI_CCG2B_SWDIO	CPU到快充芯片SWD总线数据	GPIO_AP_BI_CCG2B_SWDIO	MAKE_BASE=TRUE BI 71 96
AP_GPIO7	10	GPIO_AP_TO_CCG2B_SWCLK	CPU到快充芯片SWD总线时钟	GPIO_AP_TO_CCG2B_SWCLK	MAKE_BASE=TRUE OUT 71 96
AP_GPIO8	10	GPIO_AP_FROM_DISPLAY_PANEL_ID		GPIO_AP_FROM_DISPLAY_PANEL_ID	MAKE_BASE=TRUE IN 87 90
AP_GPIO9	10	GPIO_AP_FROM_WLAN_TIME_SYNC		GPIO_AP_FROM_WLAN_TIME_SYNC	MAKE_BASE=TRUE IN 98
AP_GPIO10	10	GPIO_AP_TO_BB_PEAK_PWR_IND		GPIO_AP_TO_BB_PEAK_PWR_IND	MAKE_BASE=TRUE OUT 99
AP_GPIO11	10	GPIO_AP_TO_BB_COREDUMP		GPIO_AP_TO_BB_COREDUMP	MAKE_BASE=TRUE OUT 99
AP_GPIO12	10	GPIO_AP_FROM_BB_RESET_DETECT_L		GPIO_AP_FROM_BB_RESET_DETECT_L	MAKE_BASE=TRUE IN 99
AP_GPIO13	10	GPIO_AP_FROM_CODEC_INT_L		GPIO_AP_FROM_CODEC_INT_L	MAKE_BASE=TRUE IN 61 96
AP_GPIO14	10	NC_AP_GPIO14		NC_AP_GPIO14	20
AP_GPIO15	10	GPIO_AP_TO_SPKRAMP_TOP_RESET_L		GPIO_AP_TO_SPKRAMP_TOP_RESET_L	MAKE_BASE=TRUE OUT 63
AP_GPIO16	10	GPIO_AP_FROM_BT_AUDIO_SYNC		GPIO_AP_FROM_BT_AUDIO_SYNC	MAKE_BASE=TRUE IN 98
AP_GPIO17	10	GPIO_AP_TO_AMUX_PMU_SYNC		GPIO_AP_TO_AMUX_PMU_SYNC	OUT 21
AP_GPIO18	10	NC_DEV_AP_GPIO18		NC_DEV_AP_GPIO18	21
AP_GPIO19	10	NC_DEV_AP_GPIO19		NC_DEV_AP_GPIO19	21
AP_GPIO20	10	NC_DEV_AP_GPIO20		NC_DEV_AP_GPIO20	21
AP_GPIO21	10	NC_DEV_AP_GPIO21		NC_DEV_AP_GPIO21	21
AP_GPIO22	10	NC_DEV_AP_GPIO22		NC_DEV_AP_GPIO22	21
AP_GPIO23	10	NC_DEV_AP_GPIO23		NC_DEV_AP_GPIO23	21
AP_GPIO24	10	NC_DEV_AP_GPIO24		NC_DEV_AP_GPIO24	21
AP_GPIO25	10	GPIO_AP_TO_BB_TIME_MARK		GPIO_AP_TO_BB_TIME_MARK	MAKE_BASE=TRUE OUT 99
AP_GPIO26	10	NC_DEV_AP_GPIO26		NC_DEV_AP_GPIO26	21

Great Dane

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SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Aliases: GPIOs
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Misc. SoC Aliases

NAND + USB & MISC

5	PP1V2_IO		1.2V供电	PP1V2_IO	20 26 30
5	PP1V2_IO				
94 5	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	MAKE_BASE=TRUE	强制DFU信号	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	27
				IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	70
5	NC_DEV_AP_TMR32_PWM0	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_AP_TMR32_PWM0	
5	NC_DEV_AP_TMR32_PWM1	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_AP_TMR32_PWM1	
5	NC_DEV_AP_TMR32_PWM2	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_AP_TMR32_PWM2	
5	NC_DEV_PAD_MTR_VREF_P	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_PAD_MTR_VREF_P	
5	NC_DEV_PAD_MTR_VREF_N	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_PAD_MTR_VREF_N	
5	PP1V2_IO			PP1V2_IO	20 26 30
94 27	IO_PMU_TO_SYSTEM_RESET_L	MAKE_BASE=TRUE	电源到CPU的主复位	IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	5
				IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	11
				IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	41
	NC_DEV_SOC_THROTTLE_TRIGGER0	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_SOC_THROTTLE_TRIGGER0	5
	NC_DEV_PMU_CPU_TRIGGER0	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_PMU_CPU_TRIGGER0	27
96	IO_AP_FROM_PMU_SW_SHDN_L	MAKE_BASE=TRUE	CPU到主电源节能开启信号	IO_AP_FROM_PMU_SW_SHDN_L CPU到主电源节能开启信号	
				IO_AP_FROM_PMU_SW_SHDN_L	27
96	IO_AP_FROM_PMU_PRE_UVLO_L	MAKE_BASE=TRUE		IO_AP_FROM_PMU_PRE_UVLO_L	5
				IO_AP_FROM_PMU_PRE_UVLO_L	27
	NC_DEV_SOC_THROTTLE_TRIGGER3	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_SOC_THROTTLE_TRIGGER3	5
	NC_DEV_PMU_GPU_TRIGGER0	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_PMU_GPU_TRIGGER0	27
	NC_DEV_SOC_THROTTLE_TRIGGER4	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_SOC_THROTTLE_TRIGGER4	5
	NC_DEV_PMU_GPU_TRIGGER1	MAKE_BASE=TRUE NO_TEST=1		NC_DEV_PMU_GPU_TRIGGER1	27
96 5	IO_SOC_TO_PMU_SOCHOT_RESET_L	MAKE_BASE=TRUE		IO_SOC_TO_PMU_SOCHOT_RESET_L	27
96 5	CLK_AP_TO_PMU_TST_CLKOUT	MAKE_BASE=TRUE	CPU到电源的测试时钟	CLK_AP_TO_PMU_TST_CLKOUT CPU到电源的测试时钟	27
5	AMUX_SOC_TO_PMU_AMUX_OUT	MAKE_BASE=TRUE	CPU到电源模拟信号	AMUX_SOC_TO_PMU_AMUX_OUT CPU到电源模拟信号	27
11	GND				
5	GND				
5	GND				
96 11	IO_AON_TO_AP_XTAL_CFSB	MAKE_BASE=TRUE CKPLUS_WAIVE=SINGLE_COMP_NET		IO_AON_TO_AP_XTAL_CFSB CPU内部端口休眠唤醒信号	5
96 73	90_EUSB_DBG_PARROT_BI_AP_N	MAKE_BASE=TRUE		90_EUSB_DBG_PARROT_BI_AP_N CPU到USB数据转换芯片测试数据N	
96 73	90_EUSB_DBG_PARROT_BI_AP_P	MAKE_BASE=TRUE		90_EUSB_DBG_PARROT_BI_AP_P CPU到USB数据转换芯片测试数据P	
9	NC_SOC_S_GPIO1	MAKE_BASE=TRUE NO_TEST=1		NC_SOC_S_GPIO1	

VSS CORNER BALLS

16	GND
16	GND
16	GND
16	GND

UART: KRAKEN

70	UART0_AP_TO_KRAKEN_DEBUG_TXD			UART0_AP_TO_KRAKEN_DEBUG_TXD	9 96
70	UART0_AP_FROM_KRAKEN_DEBUG_RXD			UART0_AP_FROM_KRAKEN_DEBUG_RXD	9 96
70	UART4_AP_TO_KRAKEN_ACC_TXD			UART4_AP_TO_KRAKEN_ACC_TXD	9 96
70	UART4_AP_FROM_KRAKEN_ACC_RXD			UART4_AP_FROM_KRAKEN_ACC_RXD	9 96

DISPLAY

8	NC_SOC_DWI_CLK			NC_SOC_DWI_CLK	
8	NC_SOC_DWI_DATA			NC_SOC_DWI_DATA	
8	NC_TOUCH_BSYNC1_DISP			NC_TOUCH_BSYNC1_DISP	
8	NC_EDP_HPD_DISP			NC_EDP_HPD_DISP	
8	NC_SOC_DISP_I2C_SCL			NC_SOC_DISP_I2C_SCL	
8	NC_SOC_DISP_I2C_SDA			NC_SOC_DISP_I2C_SDA	
8	NC_SOC_DISP_POL			NC_SOC_DISP_POL	
8	NC_SOC_DISP_AGPIO			NC_SOC_DISP_AGPIO	
8	NC_SOC_DISP_EXT_HPD			NC_SOC_DISP_EXT_HPD	
8	NC_SOC_DISP_TOUCH_EB			NC_SOC_DISP_TOUCH_EB	
8	NC_DEV_LPDP_AP_TX0P			NC_DEV_LPDP_AP_TX0P	
8	NC_DEV_LPDP_AP_TX0N			NC_DEV_LPDP_AP_TX0N	
8	NC_DEV_LPDP_AP_TX1P			NC_DEV_LPDP_AP_TX1P	
8	NC_DEV_LPDP_AP_TX1N			NC_DEV_LPDP_AP_TX1N	
8	NC_DEV_LPDP_AP_TX2P			NC_DEV_LPDP_AP_TX2P	
8	NC_DEV_LPDP_AP_TX2N			NC_DEV_LPDP_AP_TX2N	
8	NC_DEV_LPDP_AP_TX3P			NC_DEV_LPDP_AP_TX3P	
8	NC_DEV_LPDP_AP_TX3N			NC_DEV_LPDP_AP_TX3N	
8	NC_DEV_LPDP_AP_AUXP			NC_DEV_LPDP_AP_AUXP	
8	NC_DEV_LPDP_AP_AUXN			NC_DEV_LPDP_AP_AUXN	
8	NC_DEV_LPDP_AP_RCALP			NC_DEV_LPDP_AP_RCALP	
8	NC_DEV_LPDP_AP_RCALN			NC_DEV_LPDP_AP_RCALN	
8	NC_LPDP_EXT_AP_TX0_P			NC_LPDP_EXT_AP_TX0_P	
8	NC_LPDP_EXT_AP_TX0_N			NC_LPDP_EXT_AP_TX0_N	
8	NC_LPDP_EXT_AP_TX1_P			NC_LPDP_EXT_AP_TX1_P	
8	NC_LPDP_EXT_AP_TX1_N			NC_LPDP_EXT_AP_TX1_N	
8	NC_LPDP_EXT_AP_TX2_P			NC_LPDP_EXT_AP_TX2_P	
8	NC_LPDP_EXT_AP_TX2_N			NC_LPDP_EXT_AP_TX2_N	
8	NC_LPDP_EXT_AP_TX3_P			NC_LPDP_EXT_AP_TX3_P	
8	NC_LPDP_EXT_AP_TX3_N			NC_LPDP_EXT_AP_TX3_N	
8	NC_LPDP_EXT_AP_AUX_P			NC_LPDP_EXT_AP_AUX_P	
8	NC_LPDP_EXT_AP_AUX_N			NC_LPDP_EXT_AP_AUX_N	
8	NC_LPDP_EXT_AP_RCAL_P			NC_LPDP_EXT_AP_RCAL_P	
8	NC_LPDP_EXT_AP_RCAL_N			NC_LPDP_EXT_AP_RCAL_N	

ISP

7	NC_ISP_GPIO_1			NC_ISP_GPIO_1	
7	NC_ISP_GPIO_2			NC_ISP_GPIO_2	
7	NC_SENSOR2_CLK_AP			NC_SENSOR2_CLK_AP	
7	NC_SENSOR3_CLK_AP			NC_SENSOR3_CLK_AP	

SPI (AP)

9	SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2			SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2	3 22 96
9	SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1			SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1	3 22
9	SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0			SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0	3 22
9	SPI3_AP_FROM_CODEC_MISO			SPI3_AP_FROM_CODEC_MISO	61 96
9	SPI3_AP_TO_CODEC_MOSI			SPI3_AP_TO_CODEC_MOSI	61 96
9	SPI3_AP_TO_CODEC_SCLK			SPI3_AP_TO_CODEC_SCLK	61
9	SPI3_AP_TO_CODEC_CS_L			SPI3_AP_TO_CODEC_CS_L	61 96

SOC: PCIe

6	NC_DEV_PCIE_GP0_AP_CLKREQ_L			NC_DEV_PCIE_GP0_AP_CLKREQ_L	
6	NC_DEV_PCIE_GP0_AP_REFCLK_P			NC_DEV_PCIE_GP0_AP_REFCLK_P	
6	NC_DEV_PCIE_GP0_AP_REFCLK_N			NC_DEV_PCIE_GP0_AP_REFCLK_N	
6	NC_DEV_PCIE_GP0_AP_RX_P			NC_DEV_PCIE_GP0_AP_RX_P	
6	NC_DEV_PCIE_GP0_AP_RX_N			NC_DEV_PCIE_GP0_AP_RX_N	
6	NC_DEV_PCIE_GP0_AP_TX_P			NC_DEV_PCIE_GP0_AP_TX_P	
6	NC_DEV_PCIE_GP0_AP_TX_N			NC_DEV_PCIE_GP0_AP_TX_N	
6	NC_DEV_PCIE_GP0_AP_RESET_L			NC_DEV_PCIE_GP0_AP_RESET_L	

SOC: Serial

9	NC_UART1_AP_CTS_L			NC_UART1_AP_CTS_L	
9	NC_UART1_AP_RTS_L			NC_UART1_AP_RTS_L	
9	NC_UART1_AP_RXD			NC_UART1_AP_RXD	
9	NC_UART1_AP_TXD			NC_UART1_AP_TXD	
9	NC_UART2_AP_CTS_L			NC_UART2_AP_CTS_L	
9	NC_UART2_AP_RTS_L			NC_UART2_AP_RTS_L	
9	NC_UART2_AP_RXD			NC_UART2_AP_RXD	
9	NC_UART2_AP_TXD			NC_UART2_AP_TXD	
9	NC_UART3_AP_CTS_L			NC_UART3_AP_CTS_L	
9	NC_UART3_AP_RXD			NC_UART3_AP_RXD	
9	NC_I2S1_AP_MCLK			NC_I2S1_AP_MCLK	
10	NC_AP_GPIO14			NC_AP_GPIO14	
9	NC_I2S2_AP_MCLK			NC_I2S2_AP_MCLK	
9	NC_SSPI0_MISO_AP			NC_SSPI0_MISO_AP	
9	NC_SSPI0_SCLK_AP			NC_SSPI0_SCLK_AP	
9	NC_SSPI0_MOSI_AP			NC_SSPI0_MOSI_AP	
9	NC_UART6_AP_RXD_1V8			NC_UART6_AP_RXD_1V8	

SOC: AOP

11	GPIO_AOP_TO_WLAN_CONTEXT_A			GPIO_AOP_TO_WLAN_CONTEXT_A	98
11	GPIO_AOP_TO_WLAN_CONTEXT_B			GPIO_AOP_TO_WLAN_CONTEXT_B	98
19	NC_AOP_FUNC11			NC_AOP_FUNC11	
19	NC_AOP_FUNC21			NC_AOP_FUNC21	

NUB

11	NC_NUB_GPIO5			NC_NUB_GPIO5	
11	GND				
11	NC_DEV_JTAG_TDI			NC_DEV_JTAG_TDI	
11	NC_DEV_JTAG_TDO			NC_DEV_JTAG_TDO	
11	NC_DEV_JTAG_TRST_L			NC_DEV_JTAG_TRST_L	
11	PP1V2_S2			PP1V2_S2	26 30 57 72 82 83 87 88 90 99 100
96 68 11	SWD_NUB_TO_PMU_TOUCH_SWCLK	MAKE_BASE=TRUE		SWD_NUB_TO_PMU_TOUCH_SWCLK CPU到电源和触摸电源的SPMI总线时钟	27

SYNCING: D52, D53, D54

PAGE TITLE	SOC: Aliases: Misc
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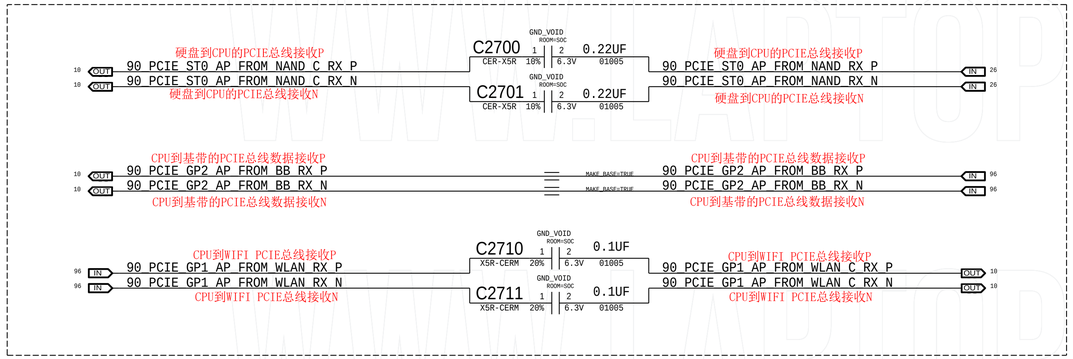
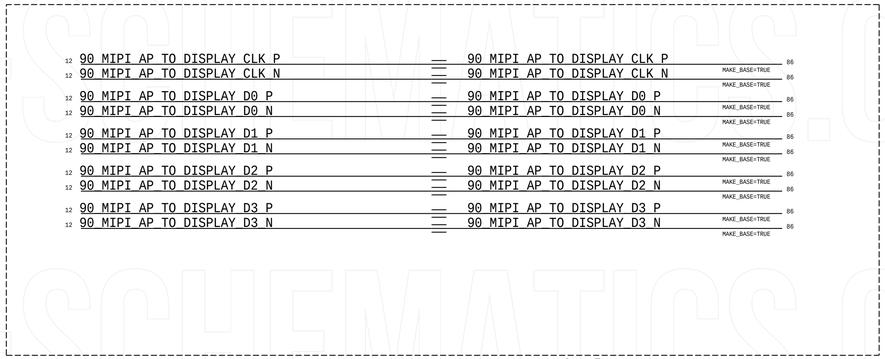
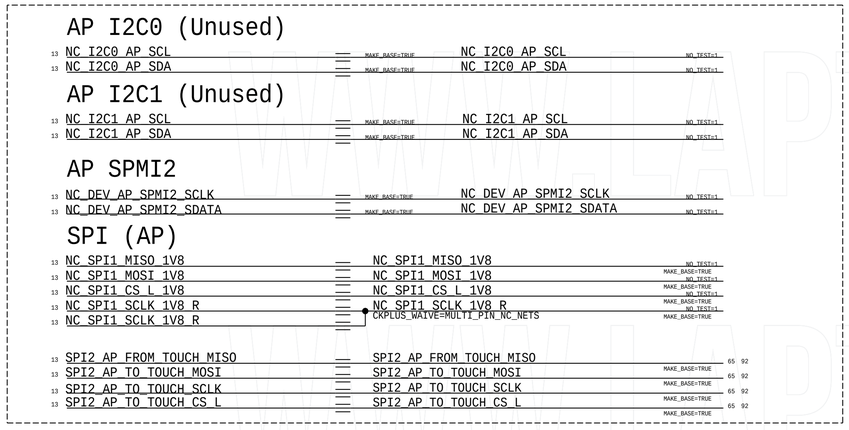
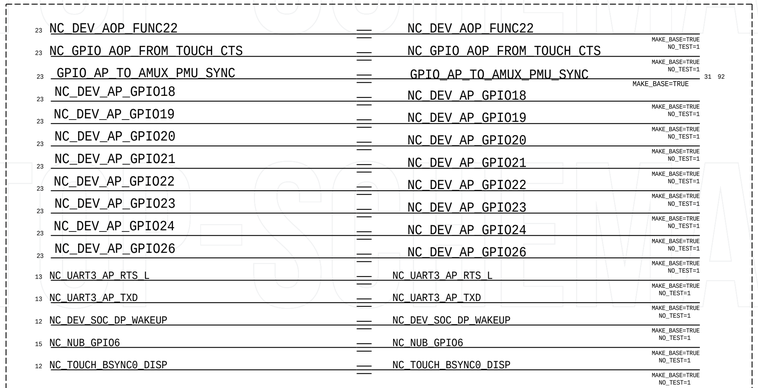
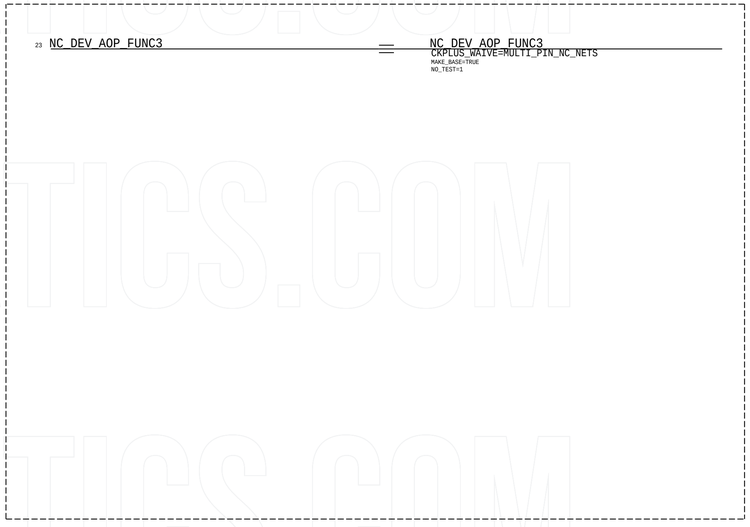




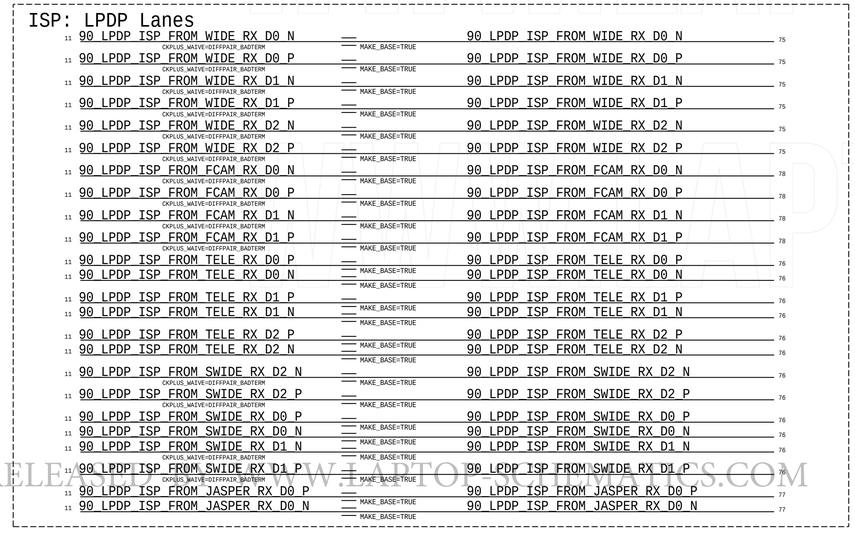




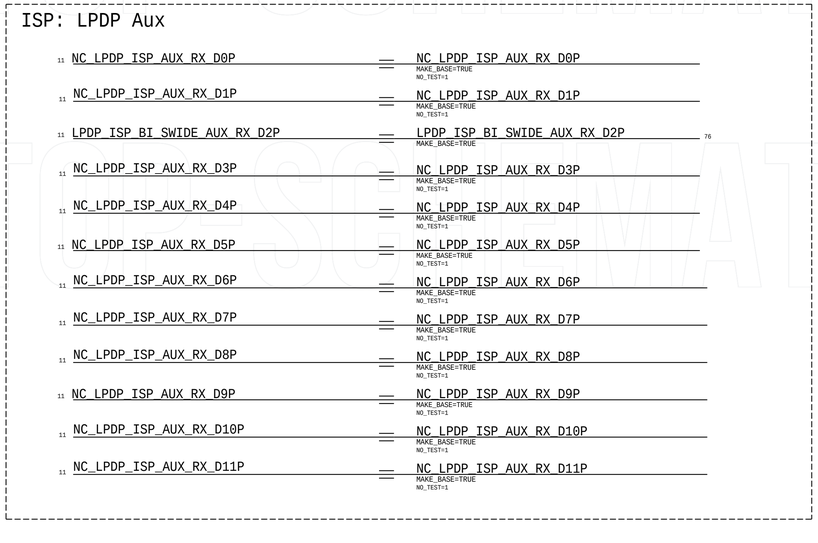
Kobol



LPDP



LPDP



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PAGE TITLE
SOC: Aliases: FF-Specific

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SIZE D
REVISION 10.0.0
BRANCH crb-1
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S5E NAND

I_VCC = 1150mA MAX (1us PEAK POWER)
PP2V625_NAND
硬盘2.625V供电

C2913 15UF 20% 6.3V X5R 0402-0.1MM-1
C2916 15UF 20% 6.3V X5R 0402-0.1MM-1
C2919 15UF 20% 6.3V X5R 0402-0.1MM-1
C2921 15UF 20% 6.3V X5R 0402-0.1MM-1
C2949 2.2UF 20% 6.3V X5R-CERM 0201
C2950 2.2UF 20% 6.3V X5R-CERM 0201
C2951 2.2UF 20% 6.3V X5R-CERM 0201
C2952 2.2UF 20% 6.3V X5R-CERM 0201
C2953 330PF 10% 16V CER-X7R 01005
C2954 330PF 10% 16V CER-X7R 01005
C2936 220PF 5% 25V C0G 01005
C2937 220PF 5% 25V C0G 01005
C2934 47PF 5% 16V NP0-C0G 01005
C2938 47PF 5% 16V NP0-C0G 01005
C2935 22PF 5% 16V C0G 01005
C2939 22PF 5% 16V C0G 01005
ROOM=NAND

U2900
H23BFG8127AEQ-BC
LGA
SYM 2 OF 2
335S00436
ROOM=NAND
OMIT_TABLE

D3 E12 G4 L12 R2 — VCC
J2 K9 T5 — VDDIO_1
E10 E2 N2 P9 — (VCCQ_ANI)
G6 G8 L6 L8 R6 R8 — VDD
(VDD)
J8 M9 N6 N8 — PCIE_VDD
PCIE_AVDD_H
(VCCQ_IO)
VSS
AVDD1X_PLL
VDDIO_2
VSS_R
VPP
VQPS
VDD_PLL

I_VDDIO1 (@ 1.2V) = 72mA MAX
PP1V2_IO
1.2V供电

C2941 2.2UF 20% 6.3V X5R-CERM 0201
C2924 2.2UF 20% 6.3V X5R-CERM 0201
C2926 2.2UF 20% 6.3V X5R-CERM 0201
C2910 0.1UF 20% 6.3V X5R-CERM 01005
C2911 220PF 5% 25V C0G 01005
C2955 220PF 5% 25V C0G 01005
C2956 330PF 10% 16V CER-X7R 01005
C2957 47PF 5% 16V NP0-C0G 01005
C2958 22PF 5% 16V C0G 01005
ROOM=NAND

FL2925 10-OHM-1.1A 01005 ROOM=NAND 155S0876
PP_NAND_VDDIO1_F VOLTAGE=1.8
C2925 2.2UF 20% 6.3V X5R-CERM 0201
R2963 2.0 5% 1/32W MF 01005 ROOM=NAND
PP_NAND_VDDIO1_R VOLTAGE=1.8
C2963 2.2UF 20% 6.3V X5R-CERM 0201

I_VDDIO2 (@ 1.2V) = 384mA MAX
PP1V2_IO
1.2V供电

C2931 15UF 20% 6.3V X5R 0402-0.1MM-1
C2929 15UF 20% 6.3V X5R 0402-0.1MM-1
C2943 2.2UF 20% 6.3V X5R-CERM 0201
C2945 2.2UF 20% 6.3V X5R-CERM 0201
C2947 2.2UF 20% 6.3V X5R-CERM 0201
C2959 330PF 10% 16V CER-X7R 01005
C2960 330PF 10% 16V CER-X7R 01005
C2912 220PF 5% 25V C0G 01005
C2915 47PF 5% 16V NP0-C0G 01005
C2917 22PF 5% 16V C0G 01005
C2961 220PF 5% 25V C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2918 47PF 5% 16V NP0-C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2914 22PF 5% 16V C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2962 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2

I_VDD = 820mA MAX
PP0V83_NAND
硬盘0.83V供电

C2948 15UF 20% 6.3V X5R 0402-0.1MM-1
C2902 15UF 20% 6.3V X5R 0402-0.1MM-1
C2905 15UF 20% 6.3V X5R 0402-0.1MM-1
FL2923 10-OHM-1.1A 01005 ROOM=NAND 155S0876
PP0V83_NAND_PLL VOLTAGE=0.83
C2923 2.2UF 20% 6.3V X5R-CERM 0201
C2900 2.2UF 20% 6.3V X5R-CERM 0201
C2901 2.2UF 20% 6.3V X5R-CERM 0201
C2922 2.2UF 20% 6.3V X5R-CERM 0201
C2927 2.2UF 20% 6.3V X5R-CERM 0201
C2940 2.2UF 20% 6.3V X5R-CERM 0201
C2942 2.2UF 20% 6.3V X5R-CERM 0201
C2944 2.2UF 20% 6.3V X5R-CERM 0201
C2946 2.2UF 20% 6.3V X5R-CERM 0201
C2907 330PF 10% 16V CER-X7R 01005
C2903 220PF 5% 25V C0G 01005
C2908 47PF 5% 16V NP0-C0G 01005
C2904 22PF 5% 16V C0G 01005
C2909 330PF 10% 16V CER-X7R 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2906 220PF 5% 25V C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3

NC_DEV_NAND_VPP
GND
VQPS used for fuse programming, GND in system

NOTES:
INT PU = internal pull up to VDDIO_1
INT PD = internal pull down to VSS
Internal pulls are 40kOhm (min), 80kOhm (typ), 165kOhm (max)

U2900
H23BFG8127AEQ-BC
LGA
SYM 1 OF 2
335S00436
ROOM=NAND
OMIT_TABLE

CLK_AP_TO_NAND_24M — M3 CLK_IN
IO_AP_TO_NAND_RESET_L — L4 RESET*
GND — G10 TRST* (INT PD)
90_PCIE_ST0_AP_TO_NAND_REFCLK_P — K11 PCIE_REFCLK_P
90_PCIE_ST0_AP_TO_NAND_REFCLK_N — J12 PCIE_REFCLK_N
PCIE_ST0_AP_BI_NAND_CLKREQ_L — P5 PCIE_CLKREQ*
90_PCIE_ST0_AP_TO_NAND_TX_P — M11 PCIE_RX0_P
90_PCIE_ST0_AP_TO_NAND_TX_N — N12 PCIE_RX0_N
90_PCIE_ST0_AP_FROM_NAND_RX_P — R12 PCIE_TX0_P
90_PCIE_ST0_AP_FROM_NAND_RX_N — T11 PCIE_TX0_N
PCIE_ST0_AP_TO_NAND_PERST_L — E8 EXT_NCE/PERST*
ANALOG_NAND_PCIE_RESREF (for dev) — H7 PCIE_RESREF
C2920 10PF 5% 16V NP0/C0G 01005 ROOM=NAND
R2904 200 0.5% 1/32W TK 01005 ROOM=NAND
Keep ZQ trace DCR < 200mOhm
ANALOG_NAND_ZQ_0 — C10 ZQ_0
ANALOG_NAND_ZQ_1 — K3 ZQ_1
(for dev)
R2900 300 1% 1/32W MF 01005-1 ROOM=NAND
R2901 300 1% 1/32W MF 01005-1 ROOM=NAND
OMIT_TABLE

(INT PU) EXT_D0/BOOT0 — B3 GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L
(INT PD) EXT_D1/BOOT1 — C4 IO_AP_TO_NAND_FW_STRAP
EXT_D2/BOOT2/SPINAND_SCLK/SPI_SCLK — B5 SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0
EXT_D3/SPINAND_MISO/SPI_MISO/SWD_UID — C6 SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2
EXT_D4/SPI_CS — B7 GND
EXT_D5/SPINAND_MOSI/SPI_MOSI/SWD_UID1 — C8 SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1
EXT_D6/BOOT3 — B9 GND
EXT_D7/SPF_N — B11 IO_PMU_TO_NAND_SYSTEM_ALIVE
(INT PU) EXT_DQS/BCM_N — D11 NC_DEV_NAND_BCM_L
(INT PU) EXT_NRE/JTAG_TMS — D7 SWD_AP_BI_NAND_SWDIO
(INT PU) EXT_NWE/JTAG_TCK — E6 SWD_AP_TO_MANY_SWCLK
EXT_RNB/JTAG_TDO — E4 GND
(INT PU) EXT_CLE/JTAG_TDI — D5 NC_DEV_NAND_JTAG_TDI
(INT PU) EXT_ALE/JTAG_SEL — D9 GND
DROOP* — T3
WP* — G2 PP1V2_IO
ANI0_VREF — G12 ANALOG_NAND_ANI0_VREF
ANI1_VREF — J4 ANALOG_NAND_ANI1_VREF

SUBSYSTEM SPECIFIC BOM TABLES

ZQ Resistor

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0784	1	RES,3000HM,1%,1/32W,01005	R2901	CRITICAL	S5E

Note: Dev Board adds an S4E option

NAND Capacities

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00436	1	HYNIX,3Dv5,64Gb,Ultimate	U2900	CRITICAL	NAND:ULTIMATE
335S00437	1	HYNIX,3Dv5,128Gb,Supreme	U2900	CRITICAL	NAND:SUPREME
335S00438	1	HYNIX,3Dv5,256Gb,Extreme	U2900	CRITICAL	NAND:EXTREME
335S00439	1	HYNIX,3Dv5,512Gb,Max	U2900	CRITICAL	NAND:MAX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00461	335S00436	NAND:ULTIMATE	U2900	KIOXIA,BiCS4.5,64Gb,Ultimate
335S00469	335S00436	NAND:ULTIMATE	U2900	WD,BiCS4.5,64Gb,Ultimate
335S00462	335S00437	NAND:SUPREME	U2900	KIOXIA,BiCS4.5,128Gb,Supreme
335S00470	335S00437	NAND:SUPREME	U2900	WD,BiCS4.5,128Gb,Supreme
335S00464	335S00438	NAND:EXTREME	U2900	KIOXIA,BiCS4.5,256Gb,Extreme
335S00472	335S00438	NAND:EXTREME	U2900	WD,BiCS4.5,256Gb,Extreme
335S00467	335S00439	NAND:MAX	U2900	KIOXIA,BiCS4.5,512Gb,Max
335S00475	335S00439	NAND:MAX	U2900	WD,BiCS4.5,512Gb,Max

SYNCING: D52, D53, D54

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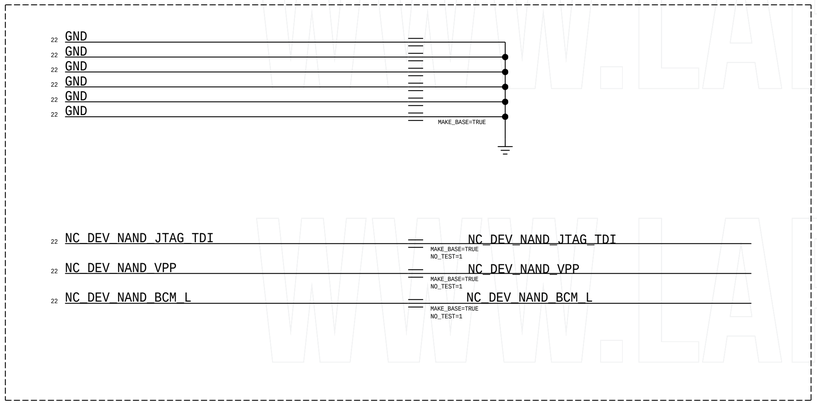
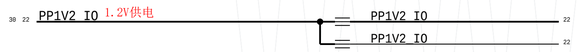
DEV BOARD COMPATIBILITY



VDDIO2



SYNCING: D52, D53, D54

PAGE TITLE	NAND: Aliases
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BUCK4 — 2.2A MAX

VOLTAGE=1.0625 (DEFAULT, DVC = 0.98V - 1.11V)
PP1V06_S2
CPU内存模块1.06V供电

C3343 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3342 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3341 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3340 220PF 5% 25V C0G 01005 ROOM=PMU

L3340 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984
LX_BUCK4 → A10 BUCK4_LX, B10 BUCK4_LX

OMIT XW3340 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
ANALOG_FB_BUCK4 → D10 BUCK4_FB, C10 BUCK4_VSS_FB
LOCAL FEEDBACK

BUCK5 — 2.0A MAX

VOLTAGE=0.763 (0.614V - 0.763V)
PP_AVE_S1
I_LOAD = 1.7A (MAX)

C3351 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D54
C3350 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D54
C3354 220PF 5% 25V C0G 01005 ROOM=PMU
C3351 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C3350 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV

L3350 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984
LX_BUCK5 → A12 BUCK5_LX, B12 BUCK5_LX

OMIT XW3350 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
ANALOG_FB_BUCK5 → D12 BUCK5_FB, C12 BUCK5_VSS_FB
MID-PLANE FEEDBACK

BUCK6 — 2.1A MAX

VOLTAGE=1.2 (DEFAULT)
PP1V2_S4

C3364 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3363 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3362 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3361 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C3360 220PF 5% 25V C0G 01005 ROOM=PMU

L3360 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984
LX_BUCK6 → A2 BUCK6_LX, B2 BUCK6_LX

OMIT XW3360 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
ANALOG_FB_BUCK6 → D2 BUCK6_FB, C2 BUCK6_VSS_FB
LOCAL FEEDBACK

BUCK7 — 2.2A MAX

VOLTAGE=0.769 (DEFAULT)
PP_SRAM_S1
暂存供电

C3371 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C3371 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D54
C3370 220PF 5% 25V C0G 01005 ROOM=PMU

L3370 0.47UH-20%-4.0A-0.05OHM PIJD2012-SM ROOM=PMU 152S00985
LX_BUCK7 → T17 BUCK7_LX, T18 BUCK7_LX

OMIT XW3370 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
ANALOG_FB_BUCK7 → T15 BUCK7_FB, T16 BUCK7_VSS_FB
MID-PLANE FEEDBACK

BUCK8 — 2.2A MAX

VOLTAGE=0.75 (0.585V - 0.75V)
PP_DISP_S1
CPU内部显示模块供电

C3382 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C3381 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3380 220PF 5% 25V C0G 01005 ROOM=PMU

L3380 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU 152S00982
LX_BUCK8 → A14 BUCK8_LX, B14 BUCK8_LX

OMIT XW3380 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
ANALOG_FB_BUCK8 → D14 BUCK8_FB, C14 BUCK8_VSS_FB
MID-PLANE FEEDBACK

BUCK9 — 0.6A MAX

VOLTAGE=1.1
PP1VX_DISPLAY_S2 显示屏1V供电
I_LOAD = 0.2A (MAX)

C3392 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3391 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C3390 220PF 5% 25V C0G 01005 ROOM=PMU

L3390 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU 152S00821
LX_BUCK9 → Y5 BUCK9_LX

OMIT XW3390 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
ANALOG_FB_BUCK9 → V5 BUCK9_FB, W5 BUCK9_VSS_FB
LOCAL FEEDBACK

BUCK9 NOTES:
1. Output is default OFF
2. Voltage adjusts dynamically based on display vendor and mode (~1.0V to ~1.15V)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C3391)	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

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U3300 TML69A0 WLCSP SYM 2 OF 5

998-19244 CRITICAL ROOM=PMU

BUCK4_LX, BUCK4_LX, BUCK4_FB, BUCK4_VSS_FB (BUCK4)
BUCK5_LX, BUCK5_LX, BUCK5_FB, BUCK5_VSS_FB (BUCK5)
BUCK6_LX, BUCK6_LX, BUCK6_FB, BUCK6_VSS_FB (BUCK6)
BUCK7_LX, BUCK7_LX, BUCK7_FB, BUCK7_VSS_FB (BUCK7)
BUCK8_LX, BUCK8_LX, BUCK8_FB, BUCK8_VSS_FB (BUCK8)
BUCK9_LX, BUCK9_FB, BUCK9_VSS_FB (BUCK9)

BUCK0_LX0, BUCK0_LX1, BUCK0_LX1, BUCK0_LX3, BUCK0_LX3, BUCK0_LX2, BUCK0_LX2, BUCK0_LX4, BUCK0_LX4, BUCK0_FB, BUCK0_VSS_FB (BUCK0)
BUCK1_LX0, BUCK1_LX1, BUCK1_LX1, BUCK1_LX2, BUCK1_LX2, BUCK1_FB, BUCK1_VSS_FB (BUCK1)
BUCK2_LX0, BUCK2_LX1, BUCK2_LX1, BUCK2_FB, BUCK2_VSS_FB (BUCK2)
BUCK3_LX, BUCK3_LX, BUCK3_LX, BUCK3_FB, BUCK3_VSS_FB (BUCK3)

BUCK0 — 13.8A MAX

L3300 1UH-20%-3.6A-0.0620HM PIWE20160H-SM ROOM=PMU 152S00876
LX_BUCK0_P0 → F18 BUCK0_LX0

L3301 0.1UH-20%-6.1A-0.019OHM ROOM=PMU MTFE2016-2SM 152S00897
LX_BUCK0_P1 → B17, B18 (UPPER_COIL_IN)
LX_BUCK0_P3 → D17, D18 (LOWER_COIL_IN)
UPPER_COIL_OUT → 3; LOWER_COIL_OUT → 4

L3302 0.1UH-20%-6.1A-0.019OHM ROOM=PMU MTFE2016-2SM 152S00897
LX_BUCK0_P2 → H17, H18 (UPPER_COIL_IN)
LX_BUCK0_P4 → K17, K18 (LOWER_COIL_IN)
UPPER_COIL_OUT → 3; LOWER_COIL_OUT → 4

(0.528V - 1.061V) VOLTAGE=1.061 PP_CPU_PCORE

C3300 220PF 5% 25V C0G 01005 ROOM=PMU
C3301 16UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU 2020-MLCC (138S00313)
C3302 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

OMIT XW3301 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION
<--- ANALOG_FB_BUCK0_R
R3300 499 1% 1/32W MF 0100 (110S00026) ROOM=PMU
OMIT XW3300 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION

BUCK0_FB, BUCK0_VSS_FB: ANALOG_FB_BUCK0 → IN ANALOG_PCPU_SENSE_P
DIE SENSE; PLACE XW NEAR U1000.BL37

BUCK1 — 10.0A MAX

L3310 1UH-20%-3.6A-0.0620HM PIWE20160H-SM ROOM=PMU 152S00876
LX_BUCK1_P0 → Y13 BUCK1_LX0

L3311 0.1UH-20%-6.1A-0.019OHM ROOM=PMU MTFE2016-2SM 152S00897
LX_BUCK1_P1 → Y17, Y17 (UPPER_COIL_IN)
LX_BUCK1_P2 → W15, Y15 (LOWER_COIL_IN)
UPPER_COIL_OUT → 3; LOWER_COIL_OUT → 4

(0.542V - 1.044V) VOLTAGE=1.044 PP_GPU
CPU集显供电

C3310 220PF 5% 25V C0G 01005 ROOM=PMU
C3311 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3312 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

OMIT XW3310 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
BUCK1_FB, BUCK1_VSS_FB: ANALOG_FB_BUCK1 → U13, V13
REMOTE FEEDBACK; PLACE NEAR SOC

BUCK2 — 4.9A MAX

L3320 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU 152S00821
LX_BUCK2_P0 → Y9 BUCK2_LX0

L3321 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
LX_BUCK2_P1 → W11, Y11 BUCK2_LX1

(0.612V - 0.79V) VOLTAGE=0.79 PP_SOC_S1
CPU内部微处理模块供电

C3320 220PF 5% 25V C0G 01005 ROOM=PMU
C3321 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU

OMIT XW3320 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
BUCK2_FB, BUCK2_VSS_FB: ANALOG_FB_BUCK2 → U9, V9
MID-PLANE FEEDBACK

BUCK3 — 1.2A MAX

L3330 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU 152S00821
LX_BUCK3 → V3, W3, Y3 BUCK3_LX

VOLTAGE=1.8 PP1V8_S4

C3330 220PF 5% 25V C0G 01005 ROOM=PMU
C3331 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3332 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3333 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3334 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

OMIT XW3330 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
BUCK3_FB, BUCK3_VSS_FB: ANALOG_FB_BUCK3 → W1, V1
LOCAL FEEDBACK

SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: PMU: Bucks (1/5)
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BRANCH	crb-1
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PMU DOCUMENTS RADAR #: 62945546

PP_VDD_MAIN

PLACE IN VICINITY OF PMU FOR BULK CAP

C3404 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU
C3405 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU
C3406 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU
C3407 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU
C3408 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU

PLACE ON PMU CORNERS TO FILL 01005 RING AROUND PMU

C3480 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3481 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3482 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3483 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU

Buck0 Buck1 Buck11

C3490 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C3491 138S00325 2.7UF 20% 6.3V X5R 0201 ROOM=PMU 2020-MLCC
C3492 138S00325 2.7UF 20% 6.3V X5R 0201 ROOM=PMU 2020-MLCC
C3493 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

998-19244
CRITICAL
U3300
TMLL69A0
WLCSP
SYM 3 OF 5
ROOM=PMU

C3450 0.22UF	A1	VDD_BUCK13_10_6_4
	B1	VDD_BUCK13_10_6_4
C3451 0.22UF	A3	VSS_BUCK13_6
	B3	VSS_BUCK13_6
C3452 0.22UF	A5	VDD_BUCK13_10_6_4
	B5	VDD_BUCK13_10_6_4
C3459 0.22UF	A7	VSS_BUCK10
	B7	VSS_BUCK10
C3453 0.22UF	A9	VDD_BUCK13_10_6_4
	B9	VDD_BUCK13_10_6_4
C3454 0.22UF	A11	VSS_BUCK5_4
	B11	VSS_BUCK5_4
C3455 0.22UF	A13	VDD_BUCK8_5
	B13	VDD_BUCK8_5
C3456 0.22UF	A15	VSS_BUCK8
	B15	VSS_BUCK8
	A16	VSS_BUCK0
	A17	VSS_BUCK0
	A18	VSS_BUCK0
C3457 0.22UF	C17	VDD_BUCK11_7_0
	C18	VDD_BUCK11_7_0
C3469 0.22UF	E17	VSS_BUCK0
	E18	VSS_BUCK0
C3458 0.22UF	G17	VDD_BUCK11_7_0
	G18	VDD_BUCK11_7_0
C3460 0.22UF	J17	VSS_BUCK0
	J18	VSS_BUCK0
C3470 0.22UF	L17	VDD_BUCK11_7_0
	L18	VDD_BUCK11_7_0
C3461 0.22UF	N17	VSS_BUCK11
	N18	VSS_BUCK11
C3462 0.22UF	R17	VDD_BUCK11_7_0
	R18	VDD_BUCK11_7_0
C3463 0.22UF	U17	VSS_BUCK7
	U18	VSS_BUCK7
	V18	VSS_BUCK1
	W18	VSS_BUCK1
	Y18	VSS_BUCK1
C3464 0.22UF	W16	VDD_BUCK12_2_1
	Y16	VDD_BUCK12_2_1
C3471 0.22UF	W14	VSS_BUCK1
	Y14	VSS_BUCK1
C3465 0.22UF	W12	VDD_BUCK12_2_1
	Y12	VDD_BUCK12_2_1
C3472 0.22UF	W10	VSS_BUCK2
	Y10	VSS_BUCK2
C3466 0.22UF	W8	VDD_BUCK12_2_1
	Y8	VDD_BUCK12_2_1
C3467 0.22UF	W6	VSS_BUCK12_9
	Y6	VSS_BUCK12_9
C3468 0.22UF	W4	VDD_BUCK9_3
	Y4	VDD_BUCK9_3
	V4	VDD_BUCK9_3
	V2	VSS_BUCK3
	W2	VSS_BUCK3
	Y1	VSS_BUCK3
	Y2	VSS_BUCK3

BUCK INPUT

BUCK10_LX0 A8 LX_BUCK10_P0
BUCK10_LX1 A6 LX_BUCK10_P1 B6
BUCK10_FB D8 ANALOG_FB_BUCK10
BUCK10_VSS_FB C8

L3400 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU 152S00021
L3401 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
OMIT XW3400 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
MID-PLANE FEEDBACK

(0.765V - 1.099V) VOLTAGE=1.099 PP_CPU_SRAM
C3401 220PF 5% 25V C0G 01005 ROOM=PMU
C3402 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3403 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK10 4.2A MAX

BUCK11_LX0 M18 LX_BUCK11_P0
BUCK11_LX1 P17 P18 LX_BUCK11_P1
BUCK11_FB M15 ANALOG_FB_BUCK11
BUCK11_VSS_FB M16

L3410 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU 152S00821
L3411 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
OMIT XW3410 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
REMOTE FEEDBACK

(0.519V - 0.828V) VOLTAGE=0.828 PP_CPU_ECORE
C3410 220PF 5% 25V C0G 01005 ROOM=PMU
C3411 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3412 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_OPTION=D54
C3412 15UF 20% 6.3V X6S 0402-0.1MM-1 ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV

BUCK11 3.8A MAX

BUCK12_LX W7 V7 LX_BUCK12
BUCK12_FB U7 ANALOG_FB_BUCK12
BUCK12_VSS_FB V7

L3420 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984
OMIT XW3420 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LOCAL FEEDBACK; PLACE NEAR U3300.N1

(DEFAULT) VOLTAGE=0.88 PP0V9_S1
C3420 220PF 5% 25V C0G 01005 ROOM=PMU
C3421 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3422 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3423 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK12 2.1A MAX

BUCK13_LX A4 LX_BUCK13
BUCK13_FB C4 ANALOG_FB_BUCK13
BUCK13_VSS_FB B4

L3430 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU 152S00982
OMIT XW3430 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
MID-PLANE FEEDBACK

(0.615V - 0.842V) VOLTAGE=0.842 PP_DCS_S1
C3432 220PF 5% 25V C0G 01005 ROOM=PMU
C3430 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3431 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK13 1.0A MAX

SYNCING: D52, D53, D54

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PMU:LDOs

PMU DOCUMENTS RADAR #: 62945546

SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	(C3515)	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	(C3515)	CAP,X5R,4UF,0201,0.55MM,KYOCERA

15uF 0402 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	[SEE BELOW]	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

(C3509,C3510,C3520,C3530,C3540,C3545,C3555,C3566,C3570)

NOTES:
1. PP1V2_SOC is low noise SOC rail, PP1V2_IO is its noisy cousin
2. PPVAR_EIGER_S2 typical output is 1.8V, max 3.275V during calibration
3. LDO3 and LDO8 are operating near-dropout by design (1.24Vin, 1.2Vout)
4. Max system load currents provided in power tree, radar # 43311246
5. OTP will disable LDO13 and LDO14 for all programs. Software must enable them for D52 and D54.
6. LDO6 is OTP programmed to be a load switch

998-19244 CRITICAL — U3300 TMLL69A0 WLCSP SYM 1 OF 5 — ROOM=PMU

PP_VDD_BOOST	F5 H4 J2 J4 J5 K1 K2 K3	VDD_BOOST_LDO	LDO GROUP 1
PP_VDD_MAIN	K5	VDD_MAIN_LDO	LDO GROUP 2 & INTERNAL POWER
PP_VDD_BOOST / PP_VDD_MAIN	H5 / G5	VDD_LDO2 / VDD_LDO15	LDO GROUP 3
PP1V2_S4	L5	VDD_LDO14_3	LDO GROUP 4
PP1V06_S2 / PP1V2_S4 / PP1V2_S4 / PP0V9_S1 / PP0V9_S1	H2 / F3 / F2 / G2 / G3	VDD_LDO4 / VDD_LDO6 / VDD_LDO8 / VDD_LDO11 / VDD_LDO12	LDO GROUP 5
PP1V8_S4	N4 N5 P4 P5	VIN_SW2_1_0	BUCK3 SWITCHES
PP1V2_S4	N3 P1 P2 P3	VIN_SW5_4_3	BUCK6 SWITCHES
PP0V9_S1	N1 N2	VIN_SW6	BUCK12 SWITCHES

VLDO1	J6	PP3V3_USB_S2	VOLTAGE=3.3
VLDO5	L1	PP2V625_NAND 硬盘2.625V供电	VOLTAGE=2.625
VLDO5	L2		
VLDO5	L3		
VLDO7	H3	PP3V0_S2	VOLTAGE=3.0
VLDO10	J1	PP3V0_DISPLAY_S2 显示屏3V供电	VOLTAGE=3.0
VLDO13	J3	PP3V1_TOUCH_S2 触摸3.1V供电	VOLTAGE=3.15
VLDO9	K6	PP1V8_ALWAYS 1.8V待机供电	VOLTAGE=1.8
VLDOINT	K4	PP1V5_VLDOINT	VOLTAGE=1.5
VMBX	L9	PMU_VMBX	
VCP_OUT	N6	PMU_VPUMP	
VLDO2	H6	PP1V8_AUDIO_VA_S2 音频1.8V供电	VOLTAGE=1.8
VLDO15	G6	PPVAR_EIGER_S2	VOLTAGE=3.0
VLDO3	L4	PP1V2_SOC	VOLTAGE=1.2
VLDO14	L6	PP1V2_TOUCH_S2	VOLTAGE=1.22
VLDO4	H1	PP0V7_VDD_LOW_S2 0.7V供电	VOLTAGE=0.7
VLDO6	F4	PP1V2_NFC_S2 NFC1.2V供电	VOLTAGE=1.2
VLDO8	F1	PP1V0_S4	VOLTAGE=1V
VLDO11	G1	PP0V6_VDDQL_S1 CPU内存模块0.6V供电	VOLTAGE=0.6
VLDO12	G4	PP0V78_SOC_FIXED_S1 CPU内部微处理模块0.78V供电	VOLTAGE=0.78
BUCK3_SW0	R4 R5	PP1V8_S2	VOLTAGE=1.8
BUCK3_SW1	M4	PP1V8_IO	VOLTAGE=1.8
BUCK3_SW2	M5	PP1V8_TOUCH_S2 触摸1.2V供电	VOLTAGE=1.8
BUCK6_SW0	R1	PP1V2_S2 1.2V供电	VOLTAGE=1.2
BUCK6_SW1	R2 R3	PP1V2_IO 1.2V供电	VOLTAGE=1.2
BUCK6_SW2	M3	PP1V2_S1 1.2V供电	VOLTAGE=1.2
BUCK12_SW0	M1 M2	PP0V83_NAND 硬盘0.83V供电	VOLTAGE=0.83

PMU LDO Capability:

LDO1	200 mA MAX
LDO5	1200 mA MAX
LDO7	250 mA MAX
LDO10	50 mA MAX
LDO13	150 mA MAX
LDO9	10 mA MAX
LDO2	50 mA MAX
LDO15	100 mA MAX
LDO3	400 mA MAX
LDO14	150 mA MAX
LDO4	300 mA MAX
LDO6	250 mA MAX
LDO8	600 mA MAX
LDO11	700 mA MAX
LDO12	580 mA MAX

BUCK_SW0: 700 mA MAX, 50mOhm MAX
BUCK_SW1: 350 mA MAX, 50mOhm MAX
BUCK_SW2: 200 mA MAX, 125mOhm MAX
BUCK_SW3: 200 mA MAX, 125mOhm MAX
BUCK_SW4: 890 mA MAX, 25mOhm MAX
BUCK_SW5: 50 mA MAX, 125mOhm MAX
BUCK_SW6: 820 mA MAX, 50mOhm MAX

Place XW3580 near U3300.F1 (star route from PMU to Arrow)

SYNCING: D52, D53, D54, DEV

DCR Requirement: <50mOhm MAX (30mOhm NOM) for Rin + Rout
Rin = DCR from XW3420 (PP0V9_S1 feedback) to U3300.N1 (SW6 input)
Rout = DCR from U3300.M1 (SW6 output) to U2900.G6 (NAND VDD)

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PMU DOCUMENTS RADAR #: 62945546

PMU - GPIOs + DIOs

See 50000123 for IO settings

AMUX CAPS

AMUX_RCAM_PVDD (27 50 51)
- C3673 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

AMUX_PMU_FROM_CAM_PMU (27 43 46 50)
- C3671 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

30 PP1V2_S2

R3661 20.0K 5% 1/32W MF 01005 ROOM=PMU

998-19244 CRITICAL

U3300 PMLL03A0 WLCSP SYM 4 OF 5 ROOM=PMU

RESET_IN1
RESET_IN2
RESET_IN3
SHDN
CRASH*
FAULT_OUT*
RESET*
ACTIVE_READY
SYS_ALIVE
VBUS_DETECT
REQUEST_DFU
FORCE_DFU
SLEEP_32K
OUT_32K
FORCE_SYNC
LDO1_EN
LDO13_EN
AMUX_A0
AMUX_A1
AMUX_A2
AMUX_A3
AMUX_A4
AMUX_A5
AMUX_A6
AMUX_A7
AMUX_AY
AMUX_B0
AMUX_B1
AMUX_B2
AMUX_B3
AMUX_B4
AMUX_B5
AMUX_B6
AMUX_B7
AMUX_BY
DFT_CTRL0
DFT_CTRL1
VSS_DFT_2
VPP
SPMI_SCLK
SPMI_SDATA
XIN
XOUT
VSS
NXTAL_MEMS
1V2 LOGIC INPUT POWER
VDDIO1V2

SYSTEM INTERFACE

96 11	IN	IO_SOC_TO_PMU_WDOG_RESET CPU到电源的看门狗信号	L12
96 70	IN	IO_PMU_FROM_KRAKEN_RESET USB到电源的复位	M11
20	IN	IO_SOC_TO_PMU_SOCHOT_RESET_L	L11
		RESET_IN3: Enabled only in PMU awake state	
30		NC_DEV_PMU_SHDN_1V8	L10
30		NC_DEV_PMU_CRASH_L_1V8	M10
70 35 29	OUT	IO_PMU_TO_DOTARA_RESET_L_1V8 电源和USB到无线充电芯片的复位	L7
94 20	OUT	IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	N9
30 29	OUT	IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY 电源输出的准备就绪信号	L8
96 22	OUT	IO_PMU_TO_NAND_SYSTEM_ALIVE 电源到硬盘激活信号	M9
30	IN	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8 充电芯片到主电源的中断信号	R14
30		NC_DEV_PMU_REQUEST_DFU	K13
20	OUT	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 强制DFU信号	N15
29 11	OUT	CLK_PMU_TO_AOP_32K 电源到CPU的32K时钟	T5
89 88	OUT	CLK_PMU_TO_TOUCH_32K_1V8 电源到触摸的32K时钟	R7
		FORCE_SYNC: SCAN_ACTIVE can tap into 1.2V or 1,8V side, whichever is easier	
33	IN	IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8 触摸输出的强制同步信号	T13
		LDO13_EN: Wired to Ada (D52/D54) LDO13_EN: GND (D53)	
96 73 70	IN	IO_KRAKEN_TO_PARROT_PMU_USB_EN USB输出的开启信号	N13
68	IN	GPIO_PMU_FROM_TOUCH_LDO_EN	P6
20	IN	AMUX_SOC_TO_PMU_AMUX_OUT CPU到电源模拟信号	F9
20	IN	IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8 显示屏到显示电源7.3V开启信号	E11
27	IN	AMUX_PMU_TO_ADC_IN	E10
72	IN	AMUX_PMU_FROM_GECKO 附件供电芯片到电源的模拟检测信号	F12
51 50 27	IN	AMUX_RCAM_PVDD 电源的检测相机PVDD供电信号	E8
		C3660: PMU Buck Noise	
27	IN	IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA USB芯片到电源的数据线ID识别输入	F13
30		GND	E9
30	IN	GND	E12
		AMUX_A7 tied to GND for AMUX calibration	
94	OUT	AMUX_PMU_AY	G13
96 21	IN	GPIO_AP_TO_AMUX_PMU_SYNC CPU到电源数模转换同步信号	E7
69	IN	AMUX_PMU_FROM_DISPLAY 主电源到显示电源的监测信号	F10
96 35	IN	DOTARA_SUPER_GPIO_1V8	F8
50 46 43 27	IN	AMUX_PMU_FROM_CAM_PMU 主电源到相机电源的监测信号	G11
29	IN	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8 点阵到相机电源和电源的中断信号	G8
29	IN	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	G9
20	IN	CLK_AP_TO_PMU_TST_CLKOUT CPU到电源的测试时钟	H9
69	IN	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K 电源到WIFI 超带宽芯片的时钟	H8
94	OUT	AMUX_PMU_BY	G12
30		GND	M7
30	IN	SWD_NUB_TO_PMU_TOUCH_SWCLK CPU到电源和触摸电源的SPMI总线时钟	M6
30		GND	T2
30		GND	E5
35 11	IN	SPMI0_NUB_TO_PMU_DOTARA_CLK CPU到电源 无线充芯片的SPMI总线时钟	P14
35 11	BI	SPMI0_NUB_BI_PMU_DOTARA_DATA CPU到电源 无线充芯片的SPMI总线数据	N14
		CLK_PMU_XTAL1_XIN_32K	T1
		CLK_PMU_XTAL2_XOUT_32K	U1
		VSS_PMU_XTAL	U3
		GND	T3
30		PP1V2_S4	P13

32KHZ OSCILLATOR

THROTTLERS

K9		PMU_VDD_MAIN_SNS
P8	OUT	IO_AP_FROM_PMU_PRE_UVLO_L
T7		NC_DEV_PMU_VDD_BOOST_UVLO_L
U15	OUT	NC_DEV_PMU_CPU_TRIGGER0
T14	OUT	IO_AP_FROM_PMU_SW_SHDN_L CPU到主电源节能开启信号
R13	OUT	NC_DEV_PMU_GPU_TRIGGER0
U14	OUT	NC_DEV_PMU_GPU_TRIGGER1

ADC

J9		PMU_VDD_MAIN_SENSE_N
J10		PMU_VDD_MAIN_SENSE_P
F11	IN	IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA USB芯片到电源的数据线ID识别信号
G14		ANALOG_PMU_VDD_MAIN_SENSE_FILT
H10		AMUX_PMU_TO_ADC_IN CKPLUS_WAIVE=SINGLE_COMP_NET

BUTTONS

K15	IN	IO_BUTTON_VOL_DOWN_L_1V8 音量减
M13	IN	IO_BUTTON_SIDE_L_1V8 开关信号
N12	IN	IO_BUTTON_VOL_UP_L_1V8 音量上
M12	IN	IO_BUTTON_RINGER_A_1V8 静音信号
L14		NC_DEV_PMU_DOWN_BUTTONO_L
L13		NC_DEV_PMU_SIDE_BUTTONO_L
M14	OUT	GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L 电源到CPU的检测信号

GPIO

P7		NC_DEV_PMU_GPIO_1
R12		GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L 电源到喇叭功放的复位
P12		SWD_NUB_BI_PMU_SWDIO CPU到电源的SPMI总线数据
P11		GPIO_S4_PMU_TO_R1_RESET_L 电源到超带宽芯片的复位
U12		GPIO_S4_PMU_TO_WLAN_REG_ON 电源到WIFI的开启信号
T12		CLK_GPIO_S4_PMU_TO_WLAN_R1_32K 电源到WIFI 超带宽芯片的时钟
R11		NC_DEV_PMU_GPIO_7
N11		GPIO_PMU_FROM_WLAN_HOST_WAKE 电源到WIFI的唤醒信号
N10		GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L 电源到基带的PCIE总线唤醒信号
T11		GPIO_PMU_TO_CCG2B_RESET_L 电源到快充芯片的复位信号
U11		GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8 充电芯片到主电源的中断信号
U10		GPIO_PMU_FROM_CODEC_WAKE_L 电源到音频的唤醒信号
T10		GPIO_PMU_TO_AMUX_PMU_SUPER_TP
R10		GPIO_PMU_NFC_TO_ARCAMP_RESET_L 电源到振动芯片复位信号
N8		GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L 电源到硬盘低电量启动信号
M8		GPIO_PMU_NFC_TO_ARCAMP_TRIG
P10		I2C2_AOP_SCL
T9		CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8 电源到显示屏32K时钟信号
R9		GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8 电源到显示屏复位信号
R8		GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8 电源到点阵芯片的开启信号
P9		GPIO_SEQ_PMU_TO_BBPMU_RESET_L 电源到基带电源的复位信号
T8		GPIO_SEQ_PMU_TO_NFC_EN 电源到NFC芯片开启信号
U5		GPIO_SEQ_PMU_TO_BOOST_EN_1V8 电源到BOOST升压芯片开启信号
T6		GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8 电源到显示屏异常识别信号
R6		GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8 电源到升压芯片旁路信号

HV,HLD (S4) = GPIO1
HLD (S4) = GPIO2
SWDIO = GPIO3
HLD (S4) = GPIO4–GPIO8
HLD (S4) = Hold Capable
HV = High Voltage
SEQ = Sequenced
SEQ = GPIO9–GPIO16
HV,SEQ = GPIO17–GPIO25

GPIO01 requires 200k PD if used (glitch mitigation)
GPIO25 requires 200k PD if used (glitch mitigation)

NTC

H13		NTC_FOREHEAD_P 顶部温度检测
H12		NTC_RADIO_BB_SE 基带温度检测
J13		NTC_RADIO_PA_SE 功放温度检测
J12		NTC_AP_P CPU温度检测
H11		NTC_BATTERY_P 电池温度检测
G10		ANALOG_PMU_TCAL

REFERENCES

J8		ANALOG_PMU_VREF_ADC
K10		ANALOG_PMU_VREF
J11		ANALOG_PMU_VSS_REF
K11		ANALOG_PMU_VSS_REF

VDD_MAIN_SNS: Drop single via to VDD_MAIN plane, place XW3650 directly at the via to the plane

NO_XNET_CONNECTION ROOM=PMU
OMIT XW3650 SHORT-20L-0.05MM-SM
PP_VDD_MAIN (25 30)

BATTERY CURRENT SENSE FILTER

- R3671 1.00K 1% 1/32W MF 01005 ROOM=PMU — PMU_VDD_MAIN_SENSE_R_N (IN 32)
- C3670 0.22UF 10% 6.3V X5R 01005 ROOM=PMU
- R3670 1.00K 1% 1/32W MF 01005 ROOM=PMU — PMU_VDD_MAIN_SENSE_R_P (IN 32)

BATTERY VOLTAGE SENSE FILTER

CRITICAL
R3603 9.53K 1% 1/32W MF 01005 ROOM=PMU — ANALOG_PMU_VDD_MAIN_SENSE (IN 76)
C3603 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU
48731558

PMU GPIO Pulls

30 PP1V8_ALWAYS 1.8V待机供电
- R3610 100K 5% 1/32W MF 01005 ROOM=PMU — GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8 (96 31 30 29) 充电芯片到主电源的中断信号
- GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8 (33 29) 电源到升压芯片旁路信号
- R3600 200K 1% 1/32W MF 01005 ROOM=PMU

REFERENCE PIN LAYOUT NOTES

1. Surface route IREF (U3300.J11) to VSS_REF (U3300.K11)
2. Drop via under VSS_REF (U3300.K11) to XW3646
3. Tie XW3646 directly from via to GND plane
4. Place XW3647 near U3300.J7

TCAL RESISTOR MUST BE 0.1%
- R3620 3.92K 0.1% 1/32W TK 01005 ROOM=PMU

0V
997mV

- C3610 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
- C3699 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU — ANALOG_PMU_VSS_VREF_ADC
- MAKE_BASE=TRUE
- OMIT XW3646 SHORT-20L-0.05MM-SM ROOM=PMU
- OMIT XW3647 SHORT-20L-0.05MM-SM ROOM=PMU

SYNCING: D52, D53, D54, DEV

Al tener en corto tenemos 900mv en el encendido.

oscilladores de sistemas electromecanicos.

MEMS Oscillator #1 (Active)

1.8V待机供电 PP1V8_ALWAYS (26 27 30 77)
- C3653 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU
- Y3601 32.768KHZ-50PPM CSP (VDD, NC, CLKOUT, GND)
- 197S00228
- PACK_IGNORE=TRUE PACK_OPTION=D53_DEV BOMOPTION=32K:MEMS1
- PACK_IGNORE=TRUE PACK_OPTION=D53_DEV BOMOPTION=32K:MEMS1

MEMS Oscillator #2 (Active)

1.8V待机供电 PP1V8_ALWAYS (26 27 30 77)
- C3654 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU
- Y3602 32.768KHZ-50PPM CSP (VDD, NC, CLKOUT, GND)
- 197S00228
- CLK_PMU_XTAL2_XOUT_32K_R
- R3652 200 1% 1/32W MF 01005 ROOM=SOC
- PACK_IGNORE=TRUE PACK_OPTION=D53 BOMOPTION=32K:MEMS2
- PACK_IGNORE=TRUE PACK_OPTION=D53 BOMOPTION=32K:MEMS2

XTAL Oscillator (Passive)

- OMIT_TABLE Y3600 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM CRITICAL ROOM=PMU
- OMIT_TABLE C3651 22PF 5% 16V C0G 01005 ROOM=PMU
- OMIT_TABLE C3652 22PF 5% 16V C0G 01005 ROOM=PMU
- OMIT XW3600 SHORT-20L-0.05MM-SM ROOM=PMU — NO_XNET_CONNECTION

RADAR #: 50214461

Note: only 1 32K option may be stuffed at once

XTAL LAYOUT NOTES

1. Flood plane of VSS_PMU_XTAL on the layer beneath the XTAL (Y3600)
2. Drop via for VSS42 (U3300.U3) directly to the VSS_PMU_XTAL plane
3. Drop 2nd via under U3300.U3 from VSS_PMU_XTAL to XW3600
4. Tie XW3600 directly from via to GND plane

- C3640 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

MEMS vs XTAL Select

30 26 PP1V5_VLDOINT

XTAL Select:
1V5 = MEMS (Active)
GND = XTAL (Passive)

- R3650 0.00 0% 1/32W MF 01005 ROOM=SOC — PACK_IGNORE=TRUE PACK_OPTION=D53,DEV BOMOPTION=32K:MEMS1&32K:MEMS2
- R3651 0.00 0% 1/32W MF 01005 ROOM=SOC — PACK_IGNORE=TRUE PACK_OPTION=D53,DEV BOMOPTION=32K:XTAL&32K:XTAL_NEWFLOW

PACK_OPTION=D52,D54

32K Sub-BOMs & XTAL new KDS flow

Population of sub-BOMs (685s) is done in d53/mlb_top bomtool

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
685-00409	1	SUBBOM,32K,XTAL,Y3600,D53	SUBBOM_32K	CRITICAL	32K:ALL
197S00013	1	XTAL,32.768KHZ,20PPM,12.5PF,1610	Y3600	CRITICAL	32K:XTAL
197S00291	1	XTAL,32.768KHZ,20PPM,12.5PF,1610	Y3600	CRITICAL	32K:XTAL_NEWFLOW
131S00378	2	CAP,C0G,22PF,2%,16V,01005	C3651, C3652	CRITICAL	32K:XTAL&32K:XTAL_NEWFLOW
117S0161	1	RES,MF,0 OHM,1/32W,01005	C3651	CRITICAL	32K:MEMS1&32K:MEMS2
131S00342	1	CAP,CER,NP0/C0G,1PF,+/-0.1PF,16V,01005	C3652	CRITICAL	32K:MEMS1&32K:MEMS2

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00410	685-00409	32K:ALL	ALL	SUBBOM,32K,MEMS1,Y3601,D53
685-00411	685-00409	32K:ALL	ALL	SUBBOM,32K,MEMS2,Y3602,D53
132S00185	132S0316	32K:MEMS1&32K:MEMS2	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005

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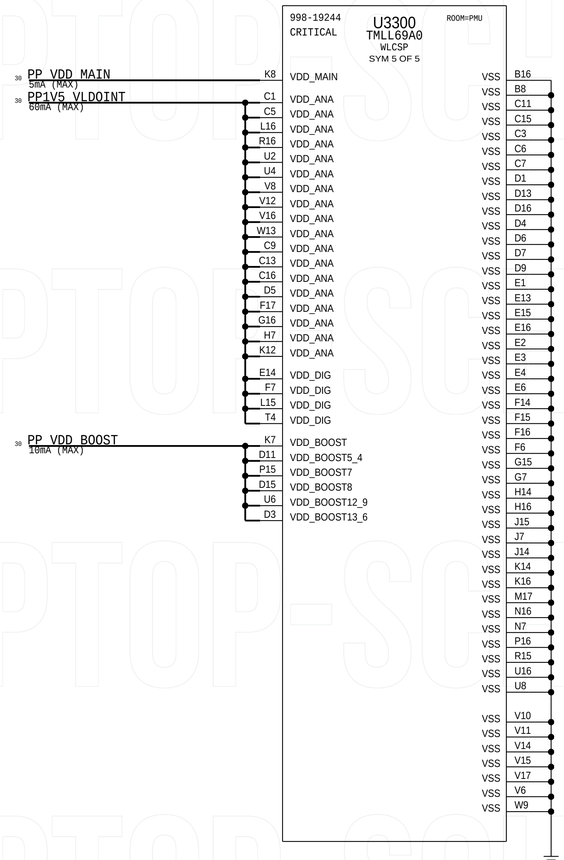

SYNCING: D52, D53, D54, DEV

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PMU GPIOs

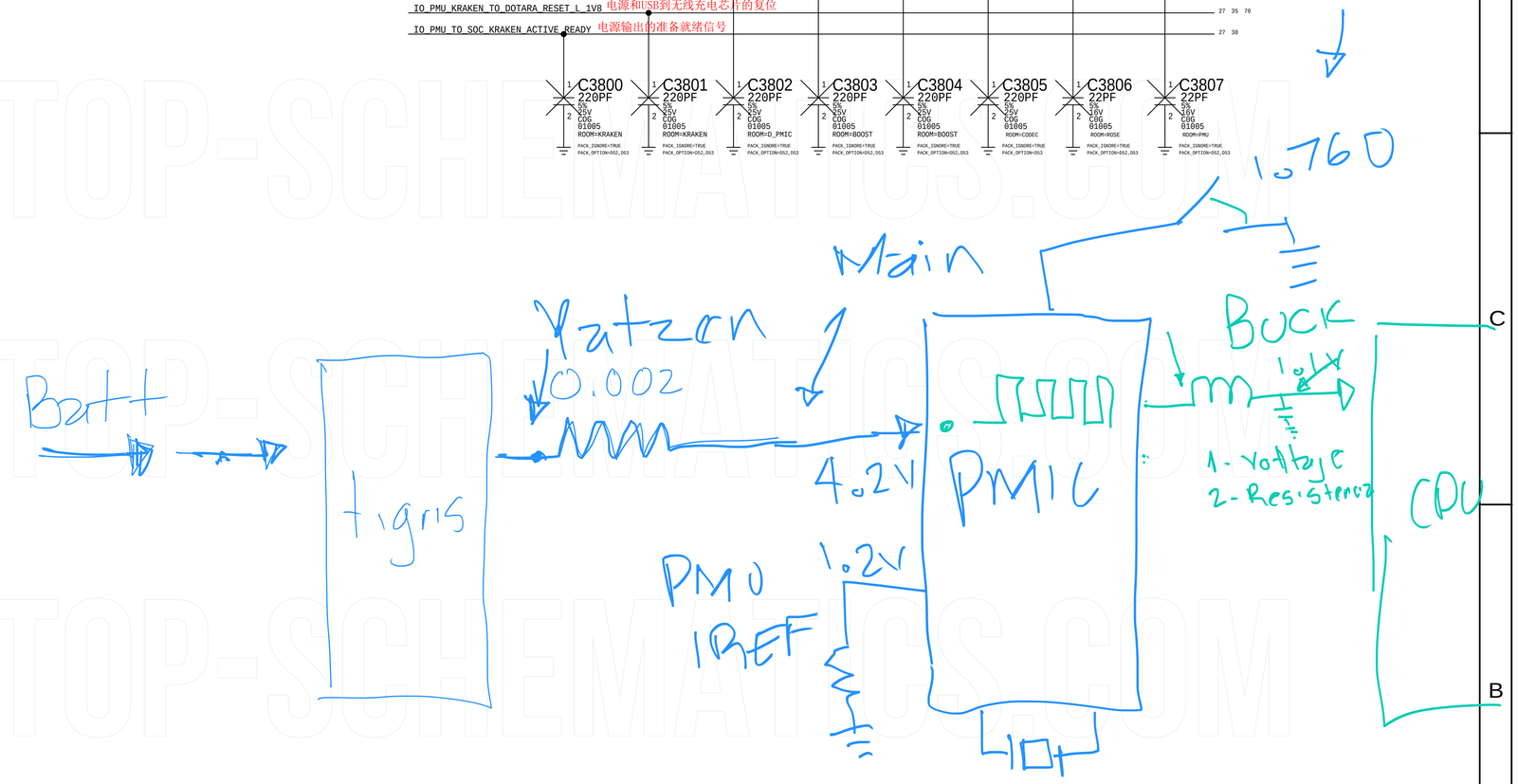
PMU_GPIO1	27	NC_DEV_PMU_GPIO_1	NC_DEV_PMU_GPIO_1			30
PMU_GPIO2	27	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L MAKE_BASE=TRUE	OUT		62 96
PMU_GPIO3	27	SWD_NUB_BI_PMU_SWDIO	SWD_NUB_BI_PMU_SWDIO	OUT		30
PMU_GPIO4	27	GPIO_S4_PMU_TO_R1_RESET_L	GPIO_S4_PMU_TO_R1_RESET_L MAKE_BASE=TRUE	OUT		101
PMU_GPIO5	27	GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO_S4_PMU_TO_WLAN_REG_ON MAKE_BASE=TRUE	OUT		98
PMU_GPIO6	27	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K CXPLUS_WAIVE=SINGLE_COMP_NET MAKE_BASE=TRUE	OUT		27 29 96 98 101
PMU_GPIO7	27	NC_DEV_PMU_GPIO_7	NC_DEV_PMU_GPIO_7			30
PMU_GPIO8	27	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE MAKE_BASE=TRUE	IN		98
PMU_GPIO9	27	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L MAKE_BASE=TRUE	IN		99
PMU_GPIO10	27	GPIO_PMU_TO_CCG2B_RESET_L	GPIO_PMU_TO_CCG2B_RESET_L MAKE_BASE=TRUE	OUT		71 96
PMU_GPIO11	27	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8 MAKE_BASE=TRUE	IN		27 30 31 96
PMU_GPIO12	27	GPIO_PMU_FROM_CODEC_WAKE_L	GPIO_PMU_FROM_CODEC_WAKE_L MAKE_BASE=TRUE	IN		29 61
PMU_GPIO13	27	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	GPIO_PMU_TO_AMUX_PMU_SUPER_TP CXPLUS_WAIVE=SINGLE_COMP_NET MAKE_BASE=TRUE	OUT		27
PMU_GPIO14	27	GPIO_PMU_NFC_TO_ARCAMP_RESET_L	GPIO_PMU_NFC_TO_ARCAMP_RESET_L MAKE_BASE=TRUE	OUT		65
PMU_GPIO15	27	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L MAKE_BASE=TRUE	OUT		22 96
PMU_GPIO16	27	GPIO_PMU_NFC_TO_ARCAMP_TRIG	GPIO_PMU_NFC_TO_ARCAMP_TRIG MAKE_BASE=TRUE	OUT		65
PMU_GPIO17	27	I2C2_AOP_SCL	I2C2_AOP_SCL MAKE_BASE=TRUE	IN		11 18
PMU_GPIO18	27	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8 MAKE_BASE=TRUE	OUT		87 90
PMU_GPIO19	27	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8 MAKE_BASE=TRUE	OUT		69 87 90
PMU_GPIO20	27	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8 MAKE_BASE=TRUE	OUT		35 96
PMU_GPIO21	27	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	GPIO_SEQ_PMU_TO_BBPMU_RESET_L MAKE_BASE=TRUE	OUT		99
PMU_GPIO22	27	GPIO_SEQ_PMU_TO_NFC_EN	GPIO_SEQ_PMU_TO_NFC_EN MAKE_BASE=TRUE	OUT		100
PMU_GPIO23	27	GPIO_SEQ_PMU_TO_BOOST_EN_1V8	GPIO_SEQ_PMU_TO_BOOST_EN_1V8 MAKE_BASE=TRUE	OUT		29 33
PMU_GPIO24	27	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8 MAKE_BASE=TRUE	OUT		29 69
PMU_GPIO25	27	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8 MAKE_BASE=TRUE	OUT		27 29 33

Buck Noise Mitigation

CLK_PMU_TO_AOP_32K	电源到CPU的32K时钟	11 27
CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	电源到WIFI 超带宽芯片的时钟	27 29 96 98 101
61 29 GPIO_PMU_FROM_CODEC_WAKE_L	电源到音频的唤醒信号	
33 29 27 GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8	电源到升压芯片旁路信号	
33 29 GPIO_SEQ_PMU_TO_BOOST_EN_1V8	电源到BOOST升压芯片开启信号	
GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	电源到显示屏异常识别信号	29 69
IO_PMU_KRAKEN_TO_DOTARA_RESET_L_1V8	电源和USB到无线充电芯片的复位	27 35 70
IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY	电源输出的准备就绪信号	27 30

C3800	220PF	5%	25V	C0G
C3801	220PF	5%	25V	C0G
C3802	220PF	5%	25V	C0G
C3803	220PF	5%	25V	C0G
C3804	220PF	5%	25V	C0G
C3805	220PF	5%	25V	C0G
C3806	22PF	5%	16V	C0G
C3807	22PF	5%	16V	C0G

	01005	
C3800	ROOM=KRAKEN	PACK_IGNORE=TRUE PACK_OPTION=D52,D53
C3801	ROOM=KRAKEN	PACK_IGNORE=TRUE PACK_OPTION=D52,D53
C3802	ROOM=D_PMIC	PACK_IGNORE=TRUE PACK_OPTION=D52,D53
C3803	ROOM=BOOST	PACK_IGNORE=TRUE PACK_OPTION=D52,D53
C3804	ROOM=BOOST	PACK_IGNORE=TRUE PACK_OPTION=D52,D53
C3805	ROOM=CODEC	PACK_IGNORE=TRUE PACK_OPTION=D53
C3806	ROOM=ROSE	PACK_IGNORE=TRUE PACK_OPTION=D52,D53
C3807	ROOM=PMU	PACK_IGNORE=TRUE PACK_OPTION=D52,D53



SYNCING: D52, D53, D54, DEV

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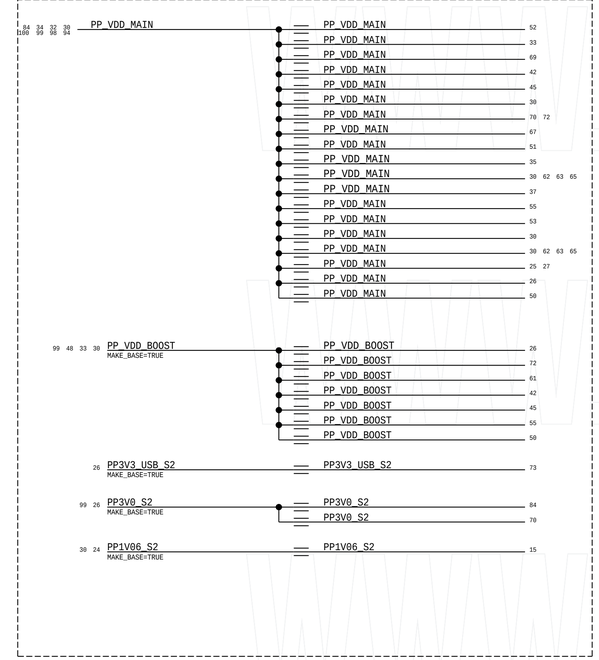
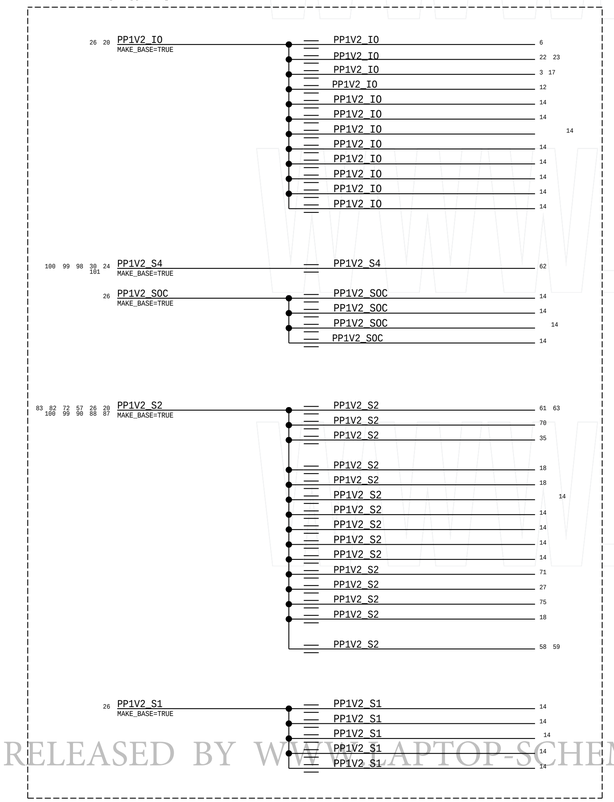
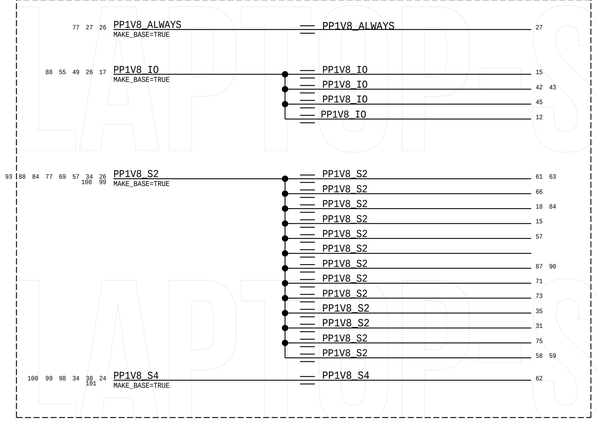
PP Misc Domains



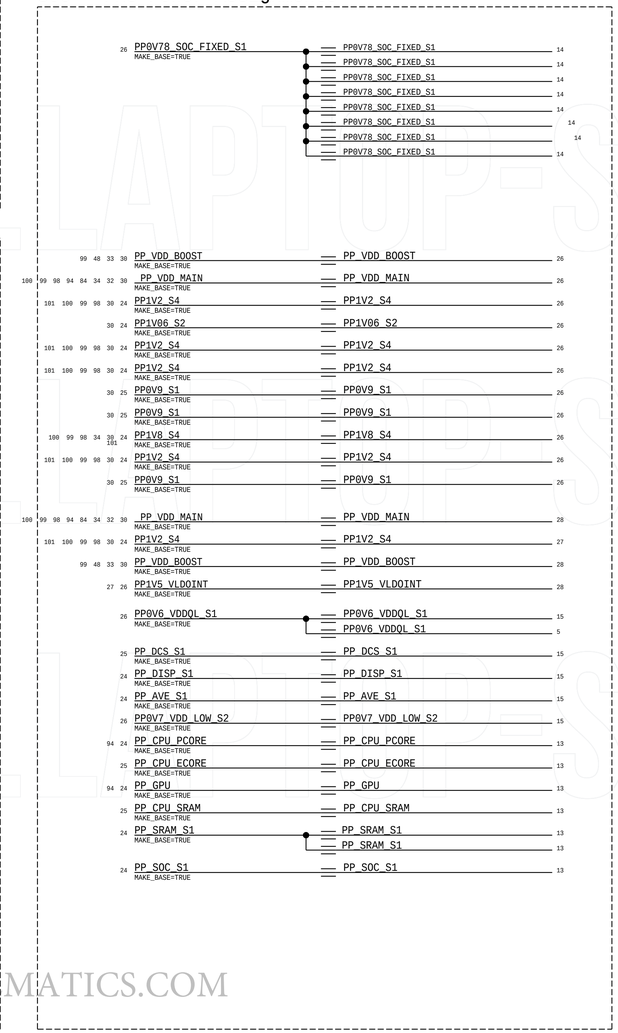
PP1V2 Domains



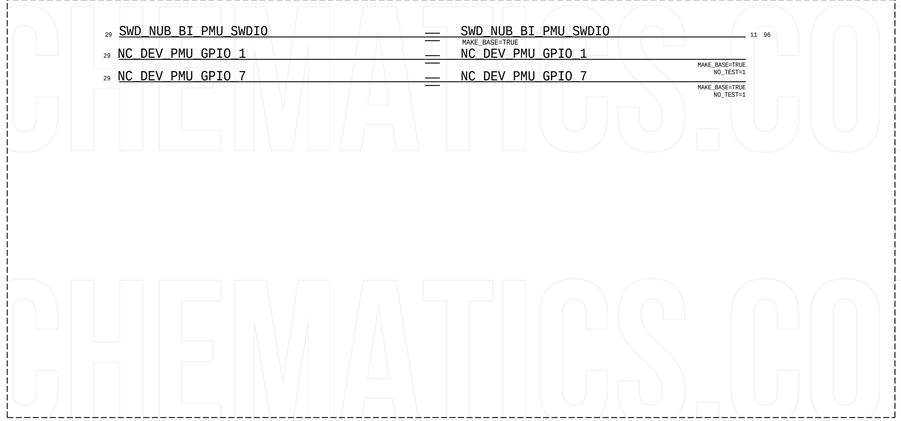
PP1V8 Domains



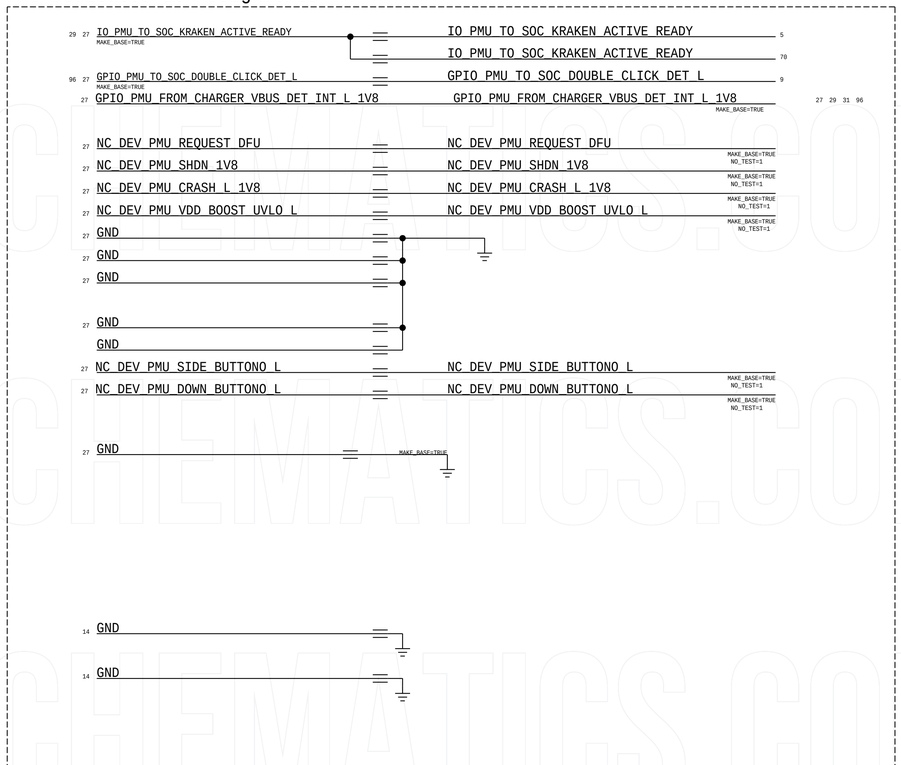
SOC + PMU Power Assignments



DEV Board Compatability



PMU Dedicated IO Assignments



SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: PMU: Aliases: Misc.
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YANGTZE CHARGER
(Veridian Charger Control)

SUBSYSTEM SPECIFIC BOM TABLES

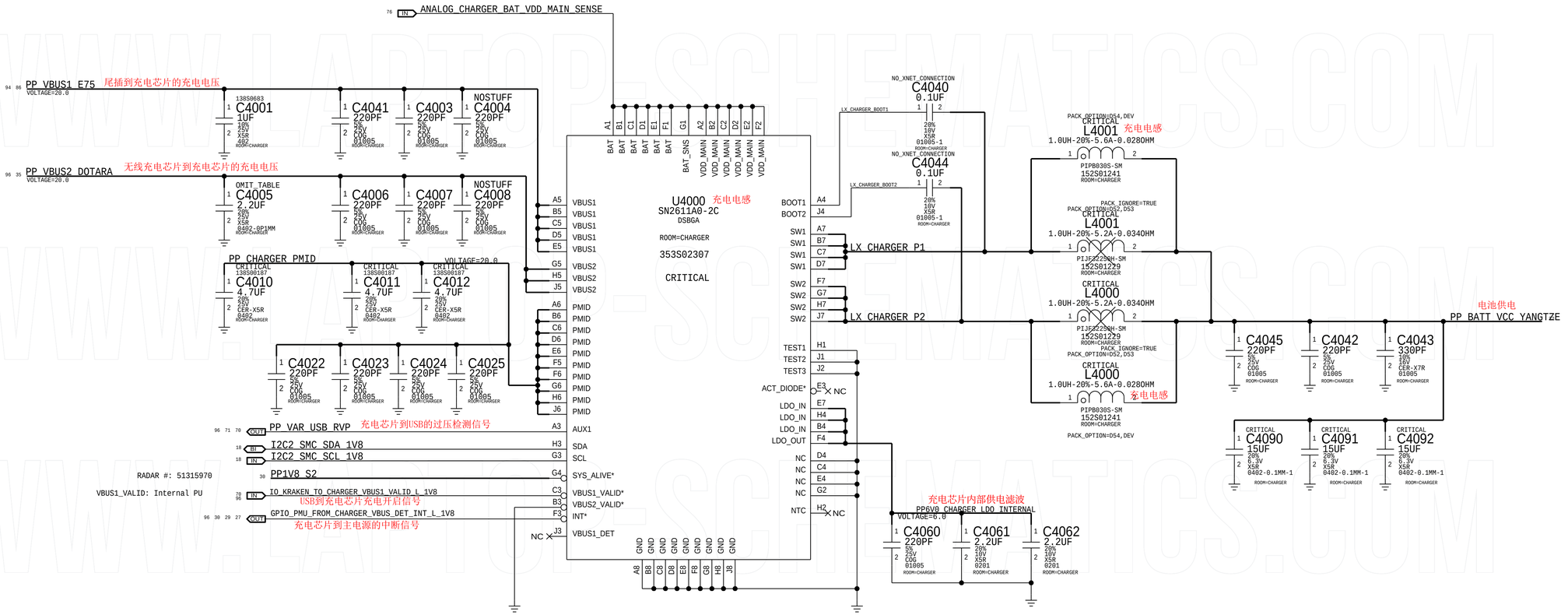
Inductors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S01341	152S01241	BOARD_ID:D54	L4000,L4001	IND,1.0UH,20%,5.6A,28MO,W=0.90,3030	[D54 ALT]
152S01292	152S01229		L4000,L4001	IND,1.0UH,20%,5.2A,34MO,W=0.89,3225	[D52/D53 ALT]

Low Noise Cap

All RefDes in ( ) do not include Murata ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	BOARD_ID:D54	(C4005)	CAP,X5R,2.2UF,20%,25V,0402



SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: Charger
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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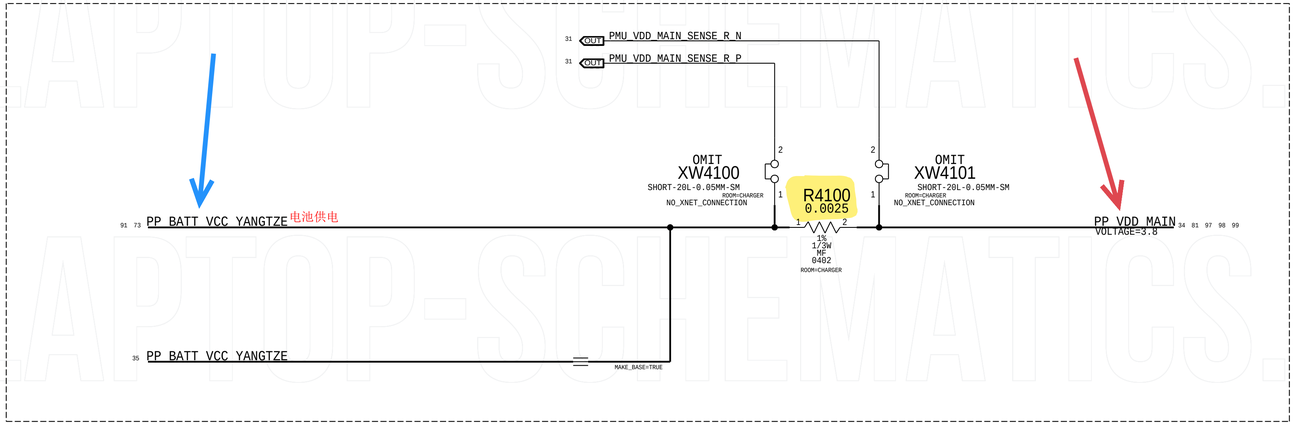
CHARGER SENSE RESISTOR



SYNCING: D52, D53

PAGE TITLE	SYS PWR: Charger/Boost: Aliases
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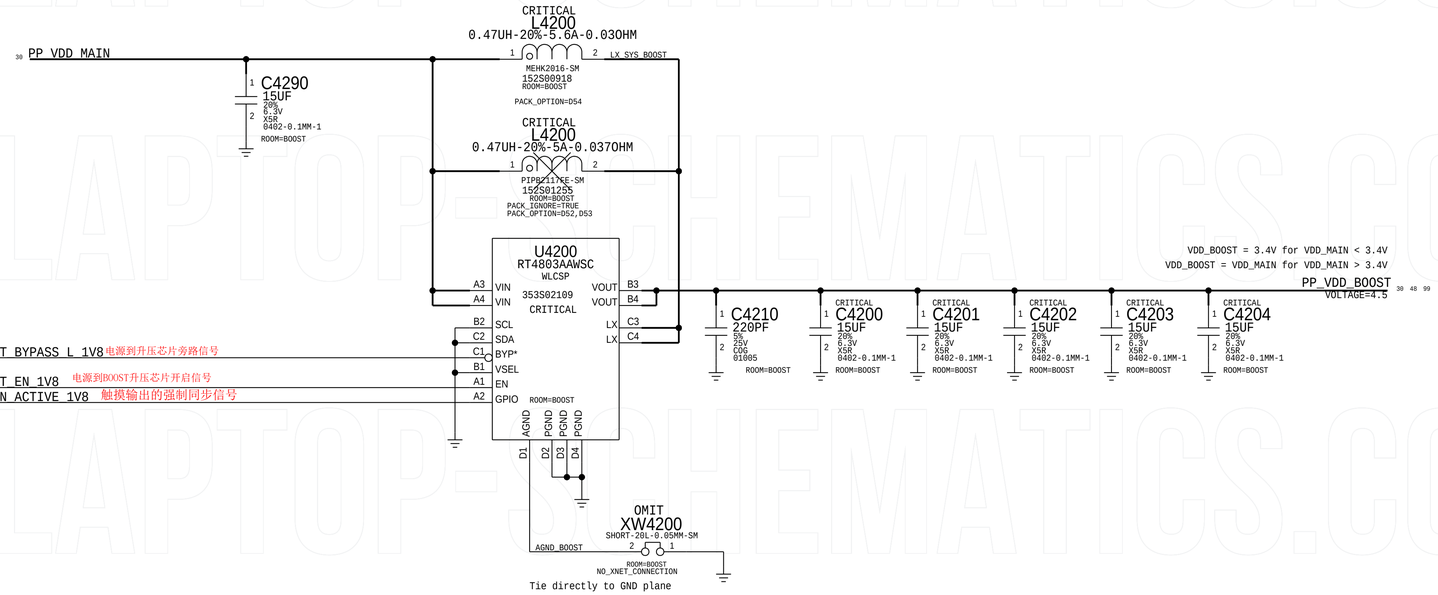
BOOST

SUBSYSTEM SPECIFIC BOM TABLES

Boost

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01124	353S02109	?	U4200	IC,SN61280E,BOOST,3.6V,4.5A,CSP16



SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: Boost
DRAWING NUMBER	051-05170
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REVISION	10.0.0
BRANCH	crb-1
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Dotara

SUBSYSTEM SPECIFIC BOM TABLES

Dotara FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00362	376S00295	?	Q4400	NFET,120V,OnSemi

Dotara CRB OTP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00678	1	DotaraLV, MTP V2.0.9	U4400	CRITICAL	?

SUBSYSTEM SPECIFIC BOM TABLES

Low Noise Cap

OMIT Table changes primary to SEMCO because Murata has desired footprint, but some locations require single-source on SEMCO

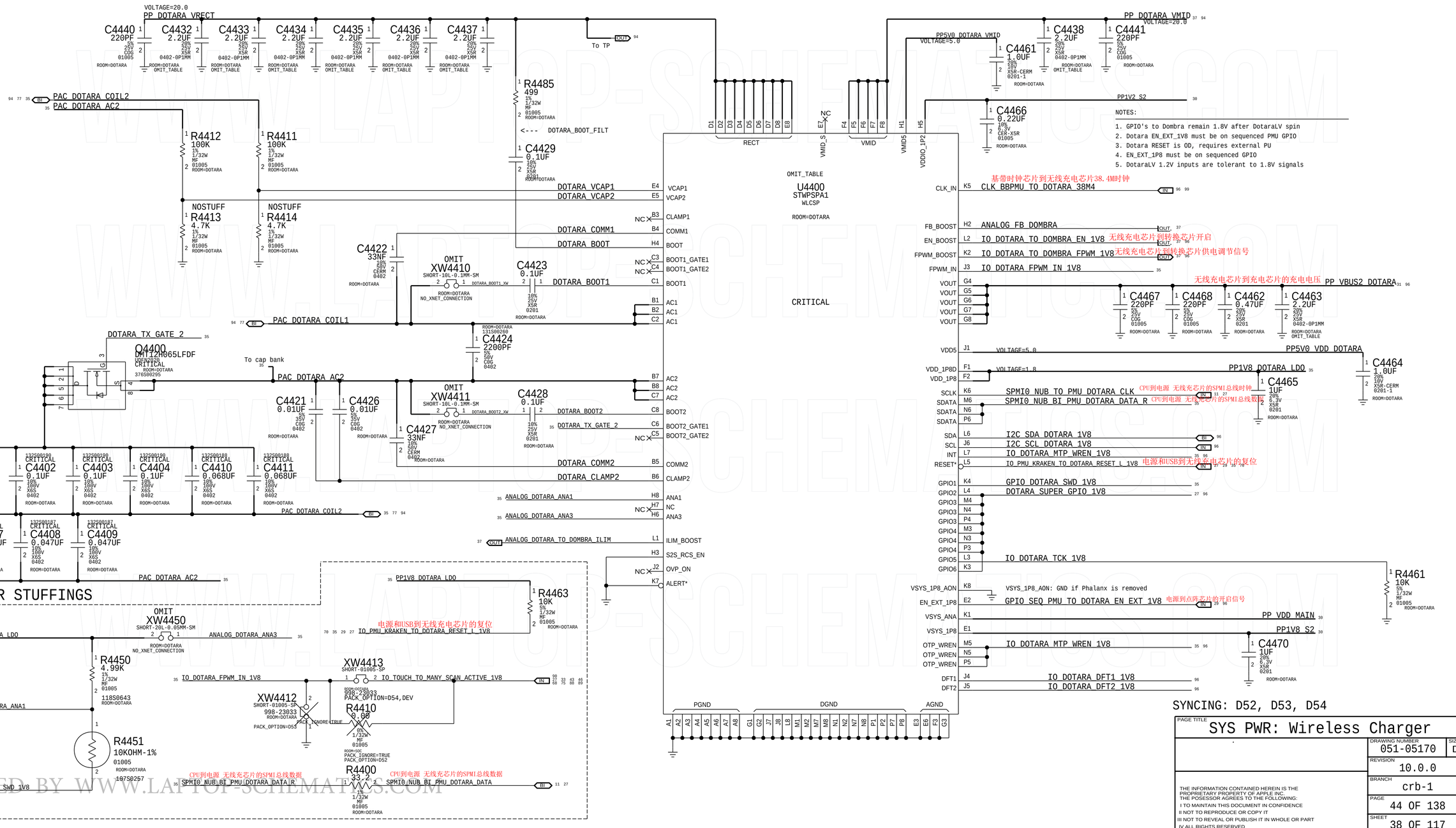
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S00246	10	CAP,X5R,2.2UF,20%,25V,0402	C4400,C4402,C4403,C4404,C4405,C4406,C4407,C4410,C4461,C4463	CRITICAL	?

All RefDes in ( ) do not include Murata ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	BOARD_ID:0X36&BOARD_ID:0X3F	[SEE BELOW]	CAP,X5R,2.2UF,20%,25V,0402
138S00185	138S00246	BOARD_ID:0X4	[SEE BELOW]	CAP,X5R,2.2UF,20%,25V,0402

DS3 Single-Source: (C4433,C4434,C4435,C4436,C4438,C4463)

DS4 Single-Source: (C4433,C4434,C4436)



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PAGE TITLE: SYS PWR: Wireless Charger

DRAWING NUMBER: 051-05170 SIZE: D

REVISION: 10.0.0

BRANCH: crb-1

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DOTARA ALIASES

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SYNCING: D52, D53, D54, DEV

PAGE TITLE	SYS PWR: Wireless Charger: Level Shifters
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SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

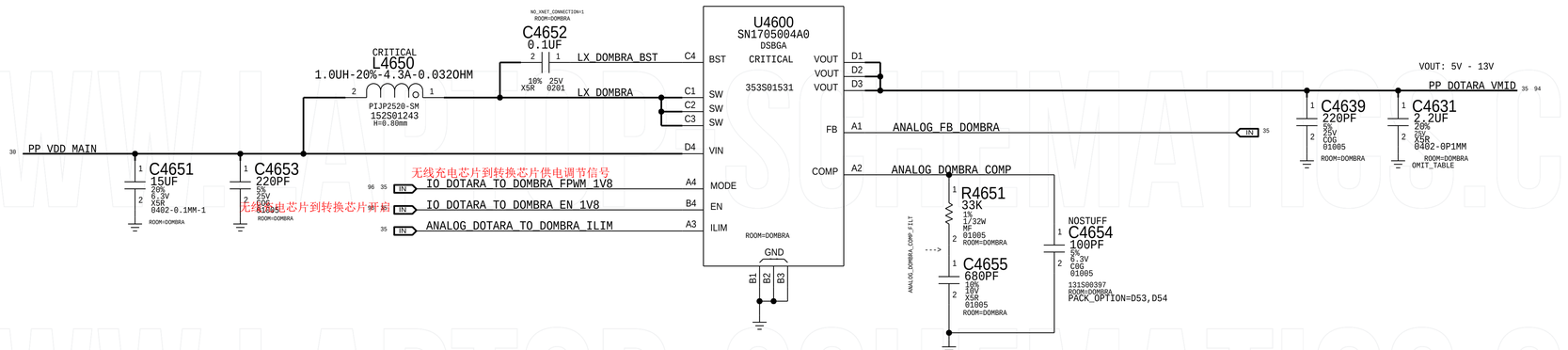
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

Low Noise Cap

All RefDes in ( ) do not include Murata ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	BOARD_ID:D54	(C4631)	CAP,X5R,2.2UF,20%,25V,0402

Dombra



SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: Wireless Charger: Boost
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SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: Wireless Charger: Aliases
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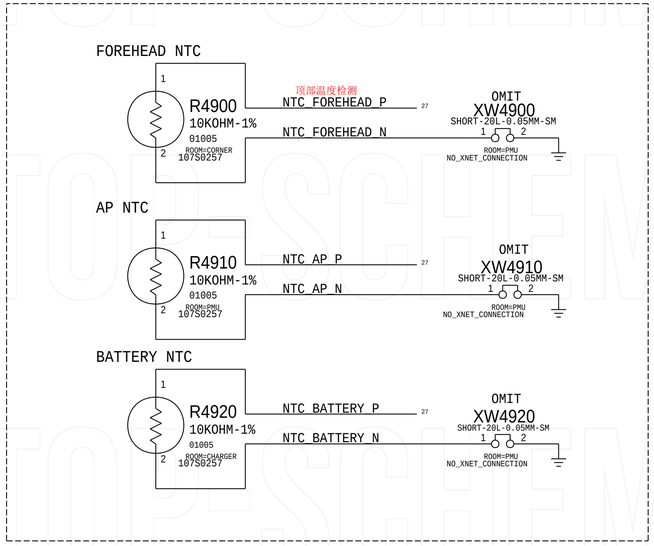
Top MLB NTCs

Place NTC XWs near PMU, route P/N differentially



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PAGE TITLE: SYS PWR: NTCs (Top)

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REVISION: 10.0.0
BRANCH: crb-1
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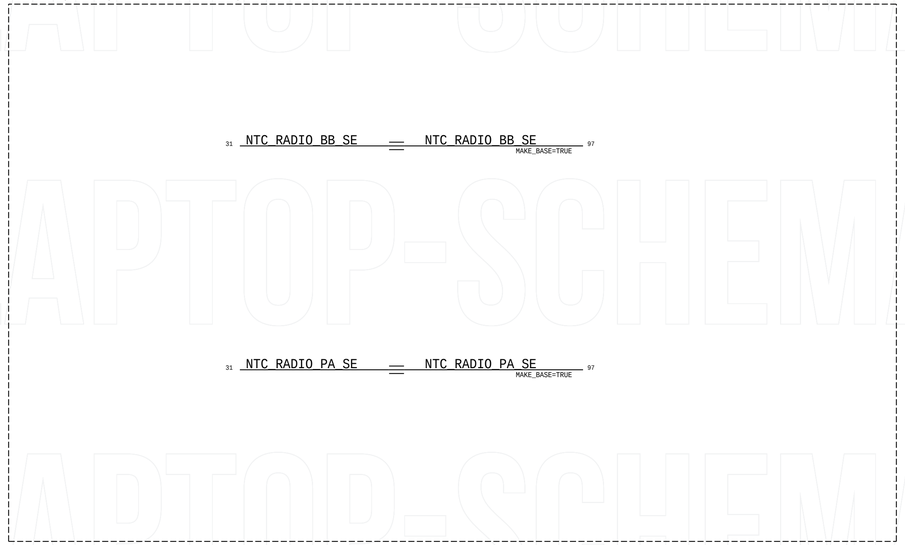
Bottom MLB NTCs

Routing single-ended on top MLB



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PAGE TITLE

SYS PWR: NTCs (Bottom)

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BRANCH crb-1

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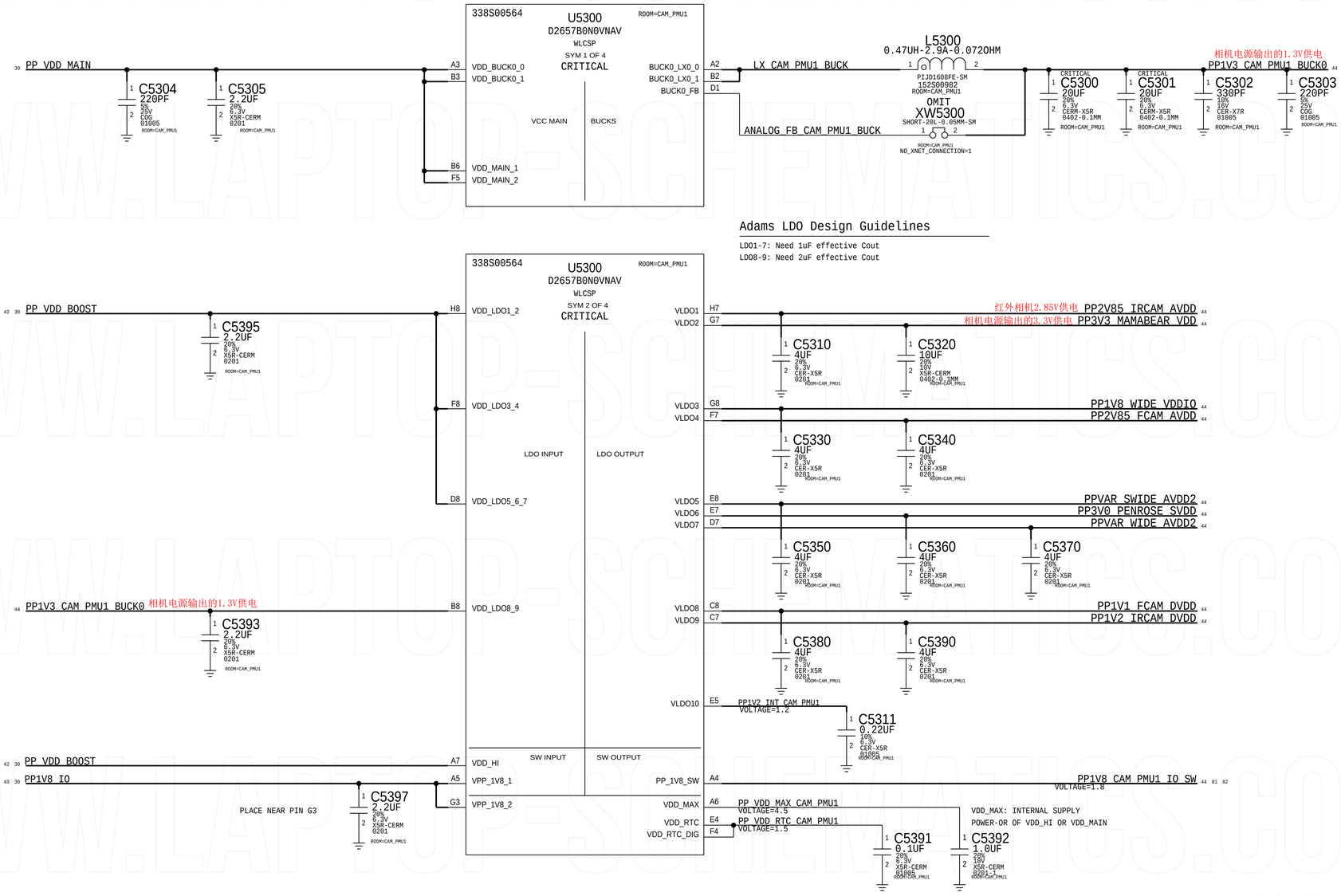
SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C5310,C5330,C5340,C5350,C5360,C5370,C5380,C5390)
(C5310,C5330,C5340,C5350,C5360,C5370,C5380,C5390)

CAMERA PMU1



SYNCING: D52, D53, D54

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PAGE TITLE
CAMERA: PMU 1: Power (1/2)

DRAWING NUMBER 051-05170 | SIZE D
REVISION 10.0.0
BRANCH crb-1
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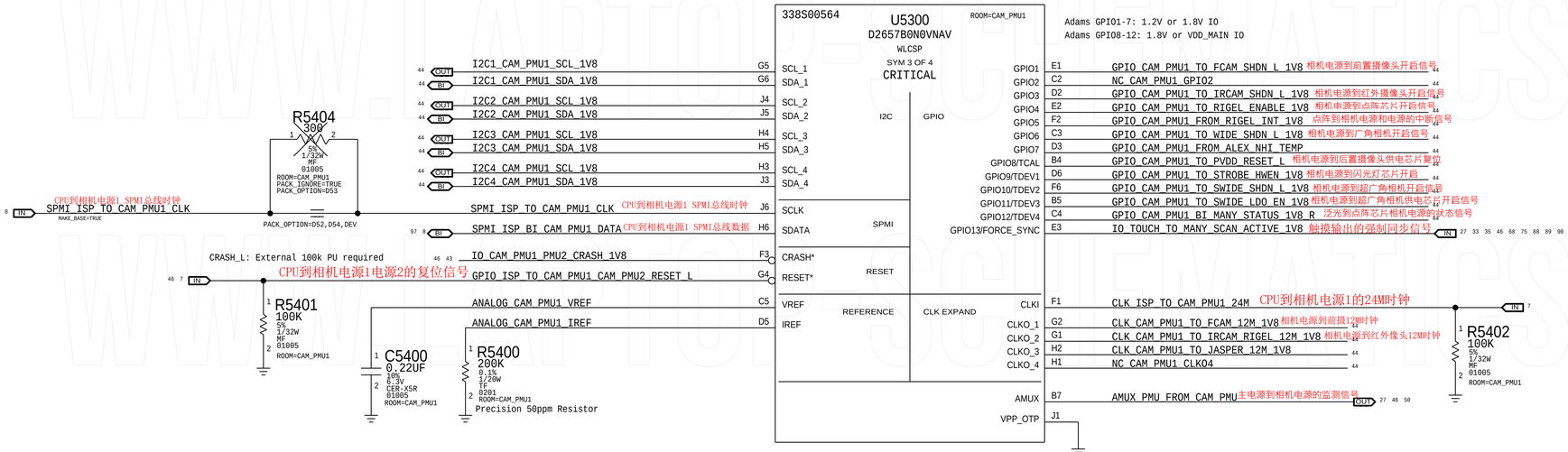
CAMERA PMU1



SYNCING: D52, D53, D54

PAGE TITLE	CAMERA: PMU 1: I/O (2/2)
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
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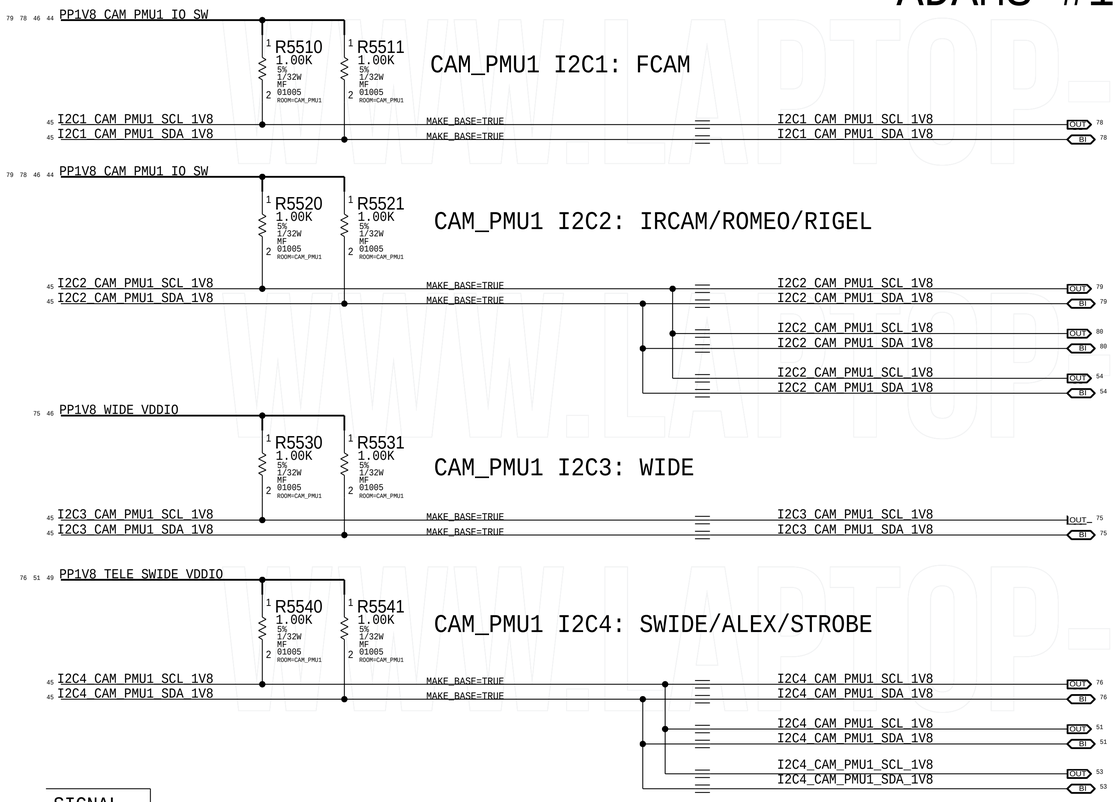
ADAMS #1 ALIASES



MASTER	CAM PMU1	NUMBER	I2C1	DIAGS NUMBER	4	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
FCAM	1.8V		0x10	0x20,0x21	1MHz	FCAM MD Flex	

MASTER	CAM PMU1	NUMBER	I2C2	DIAGS NUMBER	5	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
IRCAM	1.8V		0x18	0x30,0x31	1MHz	Juliet Flex	
Romeo	1.8V		0x66	0xCC,0xCD	1MHz	Romeo Flex	
Rigel	1.8V		0x55	0xAA,0xAB	1MHz	Top MLB	

MASTER	CAM PMU1	NUMBER	I2C3	DIAGS NUMBER	6	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
Wide	1.8V		0x10	0x20,0x21	1MHz	RCAM WI Flex	
Lorentz	1.8V		0x74	0xE8,0xE9	1MHz	RCAM WI Flex	

MASTER	CAM PMU1	NUMBER	I2C4	DIAGS NUMBER	7	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
Super Wide	1.8V		0x20	0x40,0x41	1MHz	RCAM Superflex	
Alex	1.8V		0x76	0xEC,0xED	1MHz	Top MLB	
Strobe	1.8V		0x65	0xCA,0xCB	1MHz	Top MLB	

SIGNAL

GPIO_1	45 GPIO_CAM_PMU1_TO_FCAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_FCAM_SHDN_L_1V8	MAKE_BASE=TRUE OUT 78
GPIO_2	45 NC_CAM_PMU1_GPIO2	NC_CAM_PMU1_GPIO2	NO_TEST=1 MAKE_BASE=TRUE
GPIO_3	45 GPIO_CAM_PMU1_TO_IRCAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_IRCAM_SHDN_L_1V8	MAKE_BASE=TRUE OUT 79
GPIO_4	45 GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	MAKE_BASE=TRUE OUT 54 92
GPIO_5	45 GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	MAKE_BASE=TRUE IN 31 54 92
GPIO_6	45 GPIO_CAM_PMU1_TO_WIDE_SHDN_L_1V8	GPIO_CAM_PMU1_TO_WIDE_SHDN_L_1V8	MAKE_BASE=TRUE OUT 75
GPIO_7	45 GPIO_CAM_PMU1_FROM_ALEX_NHI_TEMP	GPIO_CAM_PMU1_FROM_ALEX_NHI_TEMP	MAKE_BASE=TRUE IN 55
GPIO_8	45 GPIO_CAM_PMU1_TO_PVDD_RESET_L	GPIO_CAM_PMU1_TO_PVDD_RESET_L	MAKE_BASE=TRUE OUT 51
GPIO_9	45 GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	MAKE_BASE=TRUE OUT 53 92
GPIO_10	45 GPIO_CAM_PMU1_TO_SWIDE_SHDN_L_1V8	GPIO_CAM_PMU1_TO_SWIDE_SHDN_L_1V8	MAKE_BASE=TRUE OUT 76
GPIO_11	45 GPIO_CAM_PMU1_TO_SWIDE_LDO_EN_1V8	GPIO_CAM_PMU1_TO_SWIDE_LDO_EN_1V8	MAKE_BASE=TRUE OUT 50 92
GPIO_12	45 GPIO_CAM_PMU1_BI_MANY_STATUS_1V8_R	GPIO_CAM_PMU1_BI_MANY_STATUS_1V8_R	MAKE_BASE=TRUE
GPIO_13	Camera PMU1 GPIO13 intentionally not aliased		
CLKO_1	45 CLK_CAM_PMU1_TO_FCAM_12M_1V8	CLK_CAM_PMU1_TO_FCAM_12M_1V8	MAKE_BASE=TRUE OUT 78
CLKO_2	45 CLK_CAM_PMU1_TO_IRCAM_RIGEL_12M_1V8	CLK_CAM_PMU1_TO_IRCAM_RIGEL_12M_1V8	MAKE_BASE=TRUE OUT 54 79
CLKO_3	45 CLK_CAM_PMU1_TO_JASPER_12M_1V8	CLK_CAM_PMU1_TO_JASPER_12M_1V8	MAKE_BASE=TRUE OUT 77
CLKO_4	45 NC_CAM_PMU1_CLKO4	NC_CAM_PMU1_CLKO4	NO_TEST=1 MAKE_BASE=TRUE

POWER

VLDO1	44 PP2V85_IRCAM_AVDD	PP2V85_IRCAM_AVDD	VOLTAGE=2.9 MAKE_BASE=TRUE 79
VLDO2	44 PP3V3_MAMABEAR_VDD	PP3V3_MAMABEAR_VDD	VOLTAGE=3.3 MAKE_BASE=TRUE 80
VLDO3	44 PP1V8_WIDE_VDDIO	PP1V8_WIDE_VDDIO	VOLTAGE=1.8 MAKE_BASE=TRUE 46 75
VLDO4	44 PP2V85_FCAM_AVDD	PP2V85_FCAM_AVDD	VOLTAGE=2.9 MAKE_BASE=TRUE 78
VLDO5	44 PPVAR_SWIDE_AVDD2	PPVAR_SWIDE_AVDD2	VOLTAGE=3.0 MAKE_BASE=TRUE 76
VLDO6	44 PP3V0_PENROSE_SVDD	PP3V0_PENROSE_SVDD	VOLTAGE=3.0 MAKE_BASE=TRUE 50 82
VLDO7	44 PPVAR_WIDE_AVDD2	PPVAR_WIDE_AVDD2	VOLTAGE=3.0 MAKE_BASE=TRUE 75
VLDO8	44 PP1V1_FCAM_DVDD	PP1V1_FCAM_DVDD	VOLTAGE=1.1 MAKE_BASE=TRUE 78
VLDO9	44 PP1V2_IRCAM_DVDD	PP1V2_IRCAM_DVDD	VOLTAGE=1.2 MAKE_BASE=TRUE 79
VLDO10	Camera PMU1 LDO10 used as internal VREF		
BUCK0	44 PP1V3_CAM_PMU1_BUCK0	PP1V3_CAM_PMU1_BUCK0	VOLTAGE=1.3 MAKE_BASE=TRUE 50
(PMU1) VDD_LDO8_9	44 PP1V3_CAM_PMU1_BUCK0		
(PMU2) VDD_LDO8_9	47 PP1V3_CAM_PMU1_BUCK0		

D52/D53: PVDD Reset -> Lex
D54: PVDD Reset -> Alex

R5505 10K 5% 1/32W MF 01005 ROOM=CAM_PMU1
泛光到点阵芯片相机电源的状态信号
IO_RIGEL_BI_GRIEVOUS_STATUS_1V8 BI 54 81

R5506 10K 5% 1/32W MF 01005 ROOM=CAM_PMU1
IO_RIGEL_BI_MAMABEAR_STATUS_1V8 BI 54 80

SYNCING: D52, D53, D54

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SYNC_MASTER=0.143.0 SYNC_DATE=05/14/2019

PAGE TITLE
CAMERA: PMU 1: Aliases

DRAWING NUMBER 051-05170 SIZE D
REVISION 10.0.0
BRANCH crb-1
PAGE 55 OF 138
SHEET 46 OF 117

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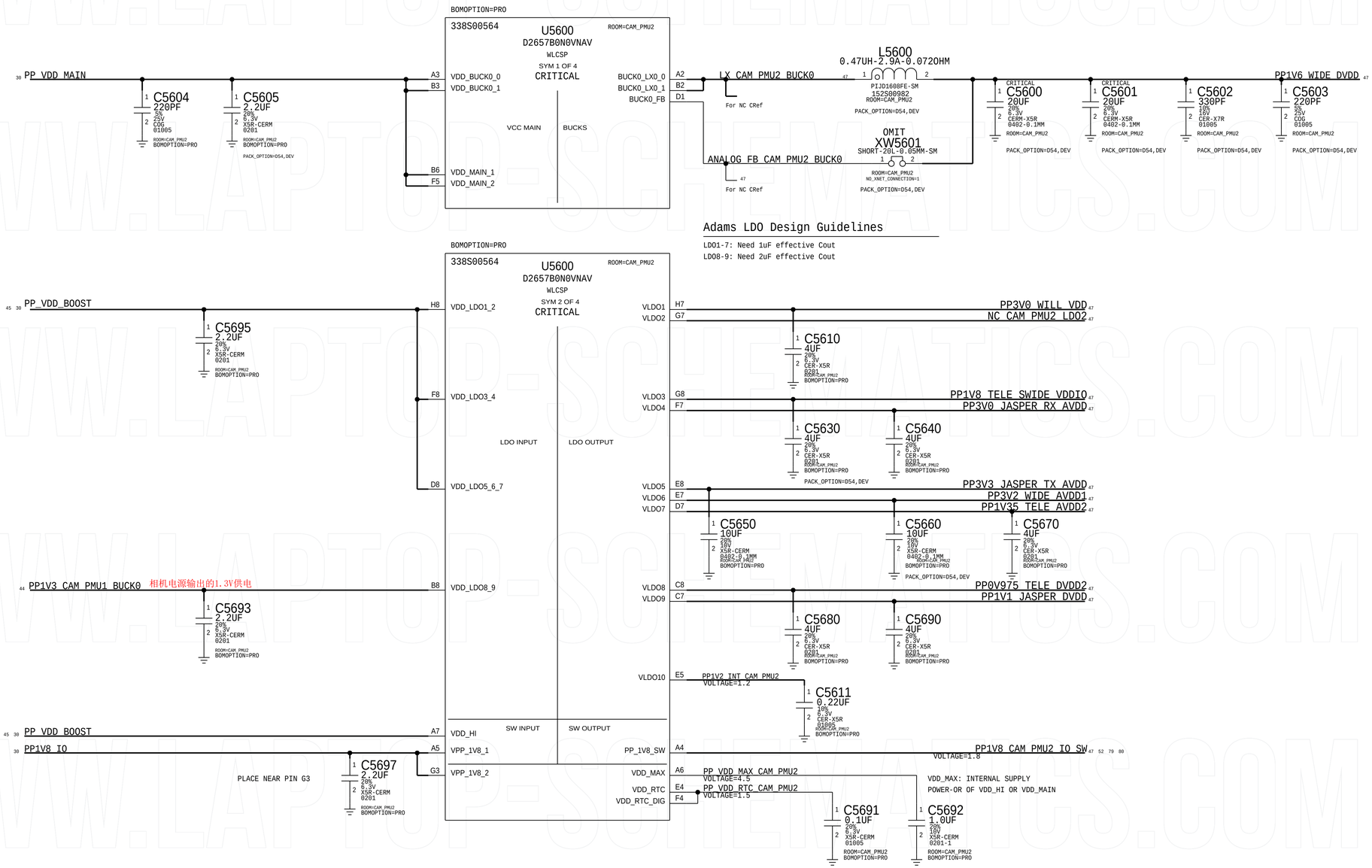
SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C5610,C5630,C5640,C5660,C5670,C5680,C5690)
(C5610,C5630,C5640,C5660,C5670,C5680,C5690)

CAMERA PMU2



SYNCING: D53, D54

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PAGE TITLE
CAMERA: PMU 2: Power (1/2)

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH crb-1
PAGE 56 OF 138
SHEET 47 OF 117

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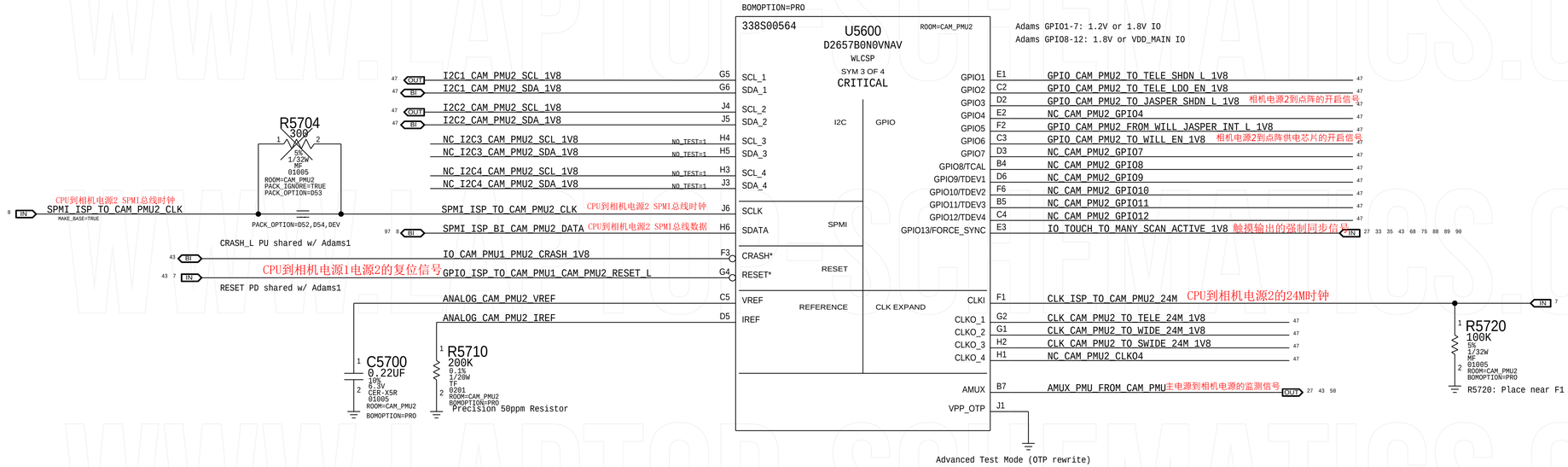
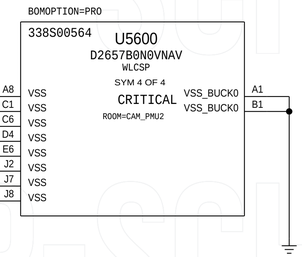
CAMERA PMU2





SYNCING: D53, D54

PAGE TITLE	CAMERA: PMU 2: I/O (2/2)
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	57 OF 138
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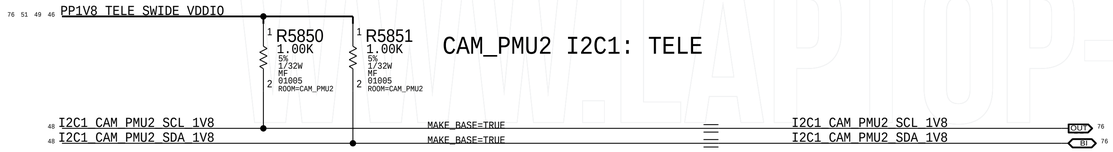
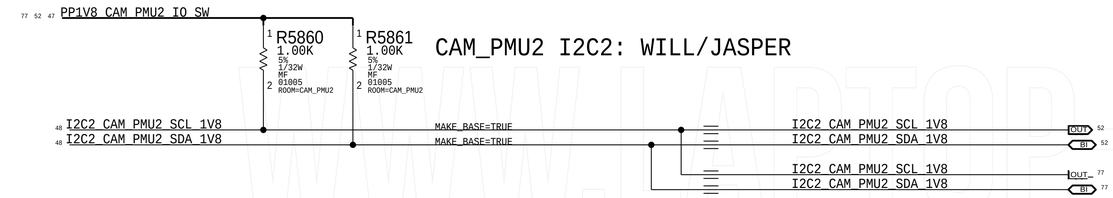
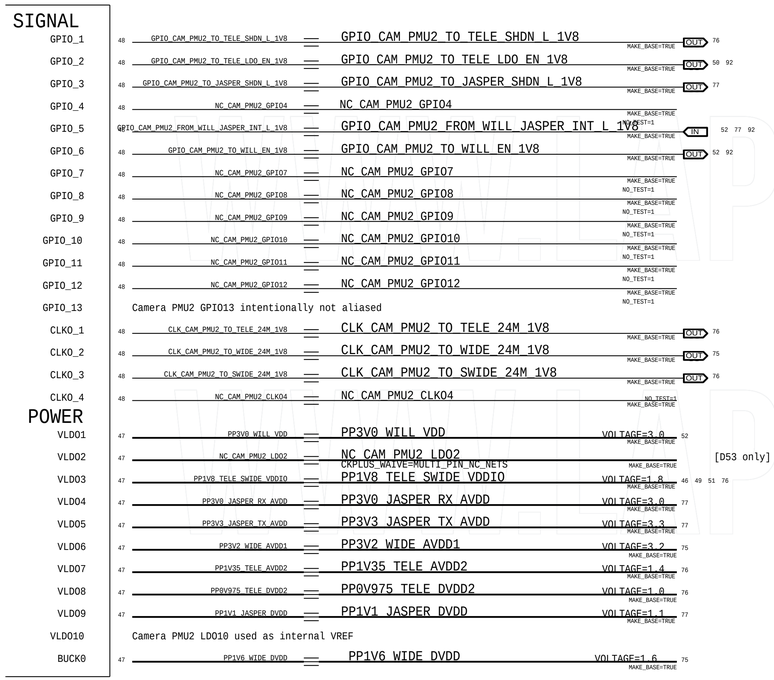
ADAMS #2 ALIASES



MASTER	CAM PMU2	NUMBER	I2C1	DIAGS NUMBER	8	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Tele	1.8V	0x10	0x20,0x21	1MHz	RCAM Superflex		
Lorentz	1.8V	0x74	0xE8,0xE9	1MHz	RCAM Superflex		



MASTER	CAM PMU2	NUMBER	I2C2	DIAGS NUMBER	9	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Will	1.8V	0x40	0x80,0x81	1MHz	Top MLB		
Periscope	1.8V	0x10	0x20,0x21	1MHz	Jasper Flex		
Riker (Main Core)	1.8V	0x33	0x66,0x67	1MHz	Jasper Flex		
Riker (OVP Core)	1.8V	0x34	0x68,0x69	1MHz	Jasper Flex		
Jasper (EEPROM)	1.8V	0x51	0xA2,0xA3	1MHz	Jasper Flex		



SYNCING: D53, D54

SYNC_MASTER=0.143.0 SYNC_DATE=05/14/2019

PAGE TITLE
CAMERA: PMU 2: Aliases

DRAWING NUMBER 051-05170 SIZE D
REVISION 10.0.0
BRANCH crb-1
PAGE 58 OF 138
SHEET 49 OF 117

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SUBSYSTEM SPECIFIC BOM TABLES

2.925V LDO

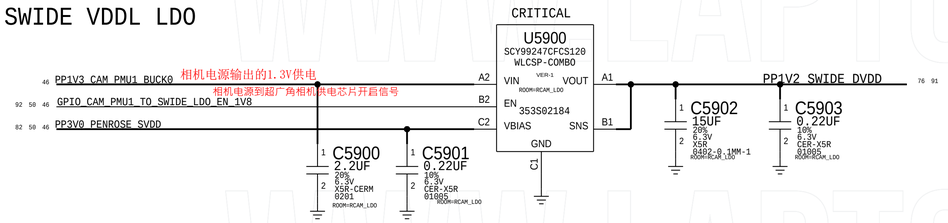
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02185	353S00015	?	ALL	IC,LDO,REG,2.925V,250MA,ONSEMI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02185	1	IC,LDO,REG,2.925V,250MA,ONSEMI	U5950	CRITICAL	?

1.2V LDO

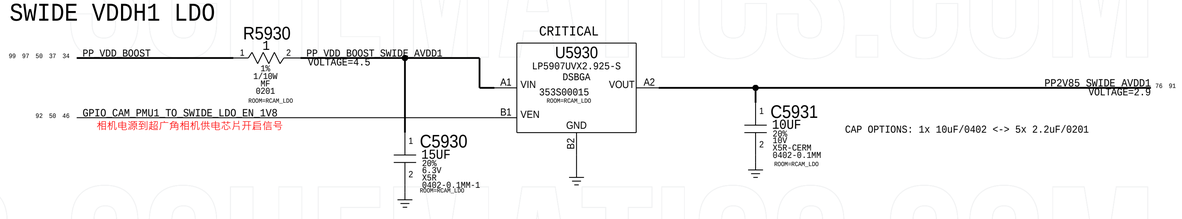
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02127	353S02184	?	ALL	IC,LDO,REG,1.20V,1000MA,RICHTEK

SWIDE VDDL LDO

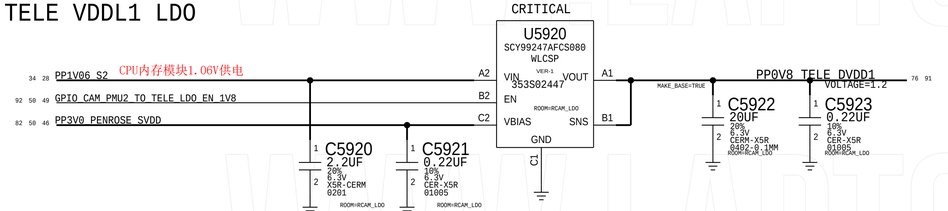


Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

SWIDE VDDH1 LDO

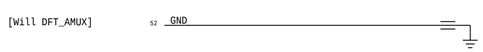


TELE VDDL1 LDO

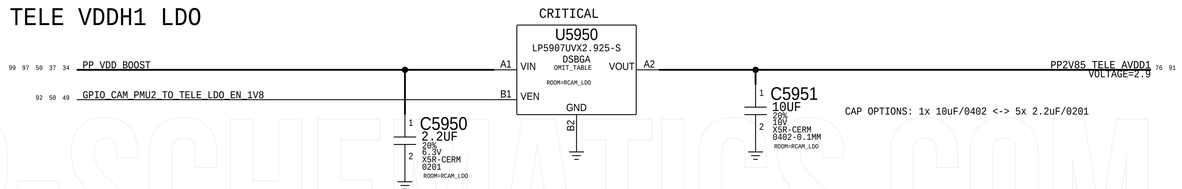


Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

Misc Aliases



TELE VDDH1 LDO



SYNCING: D52, D53, D54

SYNC_MASTER=0.143.0 SYNC_DATE=05/14/2019

PAGE TITLE

CAMERA: Discrete LDOs + Misc

DRAWING NUMBER 051-05170 SIZE D

REVISION 10.0.0

BRANCH crb-1

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SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00965	152S00640	?	ALL	Taiyo

15uF 0402 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	[SEE BELOW]	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

(C6251,C6252,C6253,C6254,C6256)

Alex

30 PP_VDD_MAIN
30 PP_VDD_BOOST

C6272 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX — VDDMAIN
C6250 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=RCAM_ALEX — VDD_SW
C6249 220PF 5% 25V C0G 01005 ROOM=RCAM_ALEX — VDD_SW
C6270 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=RCAM_ALEX — VDDMAIN
C6271 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=RCAM_ALEX — VDDHI

RESET*: Req external PD, VDD_MAIN logic level
51 44 IN GPIO_CAM_PMU1_TO_PVDD_RESET_L 相机电源到后置摄像头供电芯片复位
49 PP1V8_TELE_SWIDE_VDDIO
R6251 100K 5% 1/32W MF 01005 ROOM=RCAM_ALEX
R6250 100K 5% 1/32W MF 01005 ROOM=RCAM_ALEX
49 OUT GPIO_CAM_PMU1_FROM_ALEX_NHI_TEMP
51 44 IN I2C4_CAM_PMU1_SCL_1V8
51 44 BI I2C4_CAM_PMU1_SDA_1V8

U6250 D2748 CSP-1 338S00616 CRITICAL
B1 VDDHI, A5 VDD_SW, C4 VDDMAIN
B4 RESET*, C5 NHI_TEMP, C1 SCL, C2 SDA
BUCK_LX A4, BOOST_LX A2, VOUT A1, VOUT_FB B3, VBOOT B2, IOUT_SNS B5
ROOM=RCAM_ALEX
C3 VSS, A3 VSS_SW

A4 LX_BUCK_ALEX
CRITICAL L6250 0.47UH-20%-4A-0.048OHM PIWA2012H-SM 152S00640 ROOM=RCAM_ALEX
132S00283 C6260 6800PF 10% 16V X5R 01005 ROOM=RCAM_ALEX NO_XNET_CONNECTION
ALEX_BOOT 50
A2 LX_BOOST_ALEX
B2 ALEX_BOOT 50
B5 ALEX_IOUT_SNS
[LAYOUT] IOUT_SNS: <14pF max parasitic cap

XW6250 SHORT-20L-0.05MM-SM OMIT ROOM=RCAM_ALEX
PPVAR_RCAM_PVDD: I_Load = 900mA (MAX)
VOLTAGE=3.3
PPVAR_RCAM_PVDD 51 78 79
C6255 330PF 10% 16V C0G-X7R 01005 ROOM=RCAM_ALEX
C6251 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6252 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6253 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6254 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6256 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
XW6251 SHORT-20L-0.05MM-SM OMIT ROOM=RCAM_ALEX
电源的检测相机PVDD供电信号
AMUX_RCAM_PVDD OUT 27 51
XW6200 SHORT-01005-SP ROOM=RCAM_ALEX 998-22933
主电源到相机电源的监测信号
AMUX_PMU_FROM_CAM_PMU OUT 27 43 46
PACK_OPTION=D52,D54

SYNCING: D54

PAGE TITLE	CAMERA: Actuator Supply (Alex)
-	
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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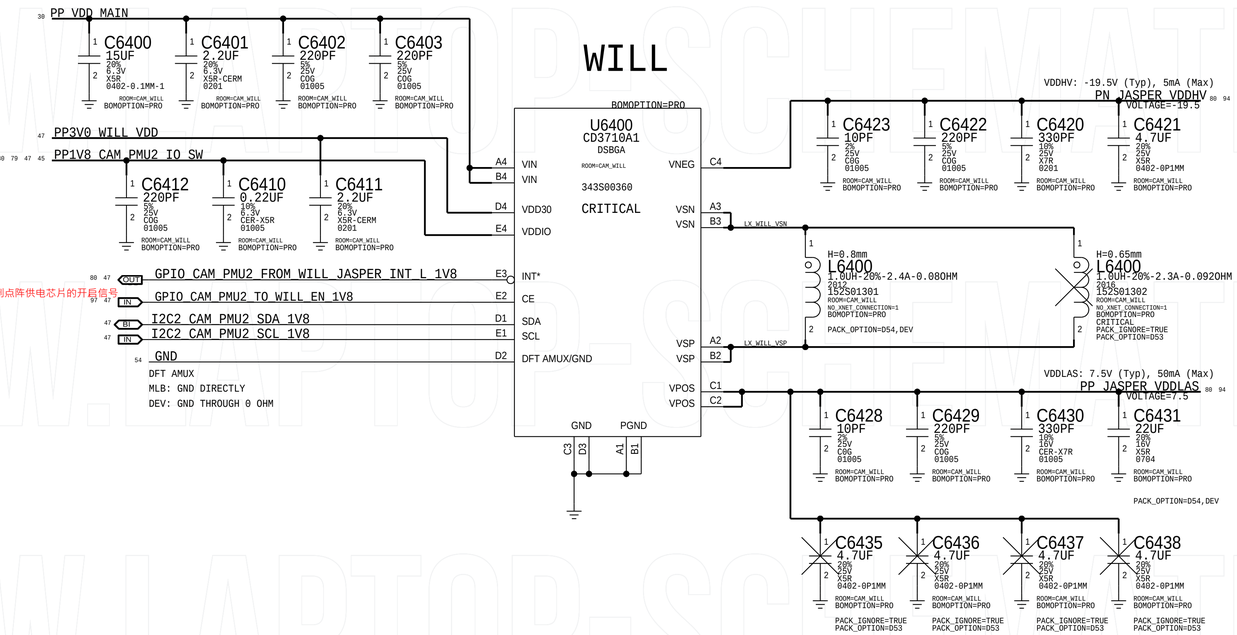
SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01343	152S01301	?	ALL	IND,MLG,1.0UH,20%,2.3A,52MOHM,H=0.8,2012

CRITICAL PART#	COMMENT
152S01301	IND,MLD,1.0UH,20%,2.3A,52MOHM,H=0.8,2012



SYNCING: D53, D54

PAGE TITLE	CAMERA: Will
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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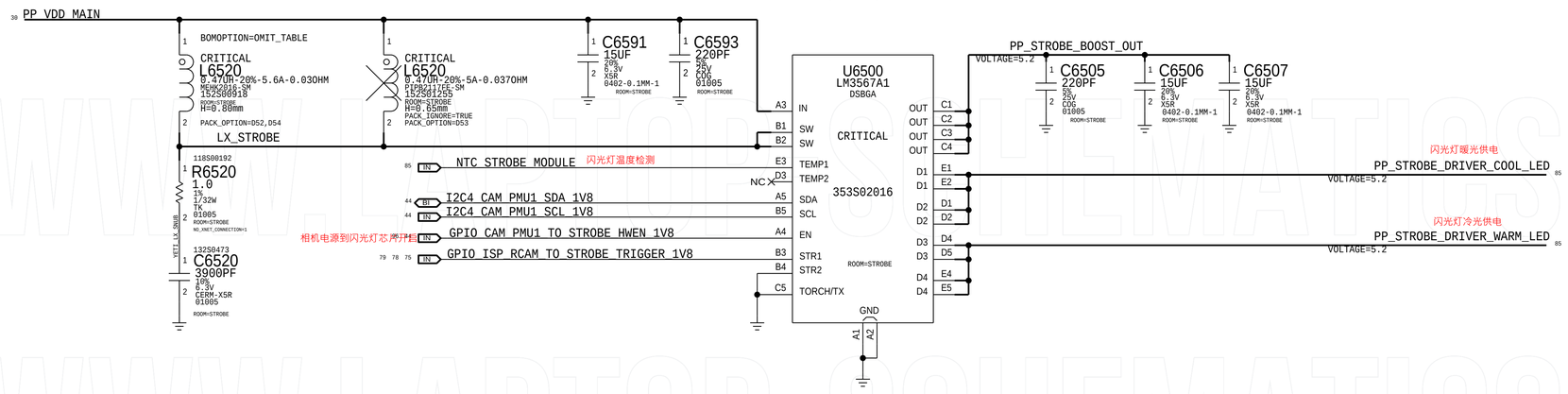
Yeti Inductor

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00872	152S00847	BOARD_ID:D54	L6520	IND,0.47UH,20%,5.6A,30MO,H=0.80,2016,TDK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S00918	1	IND,MLD,0.47UH,20%,5.6A,30MO,H=0.80,2016,TAIYO	L6520	CRITICAL	BOARD_ID:D52
152S00847	1	IND,MLD,0.47UH,20%,5.6A,26MO,H=0.80,2016,CYNTEC	L6520	CRITICAL	BOARD_ID:D54

LED STROBE DRIVER (YETI)

I2C Address (7-bit): 0x65



SYNCING: D52, D53, D54

PAGE TITLE	CAMERA: Strobe Driver
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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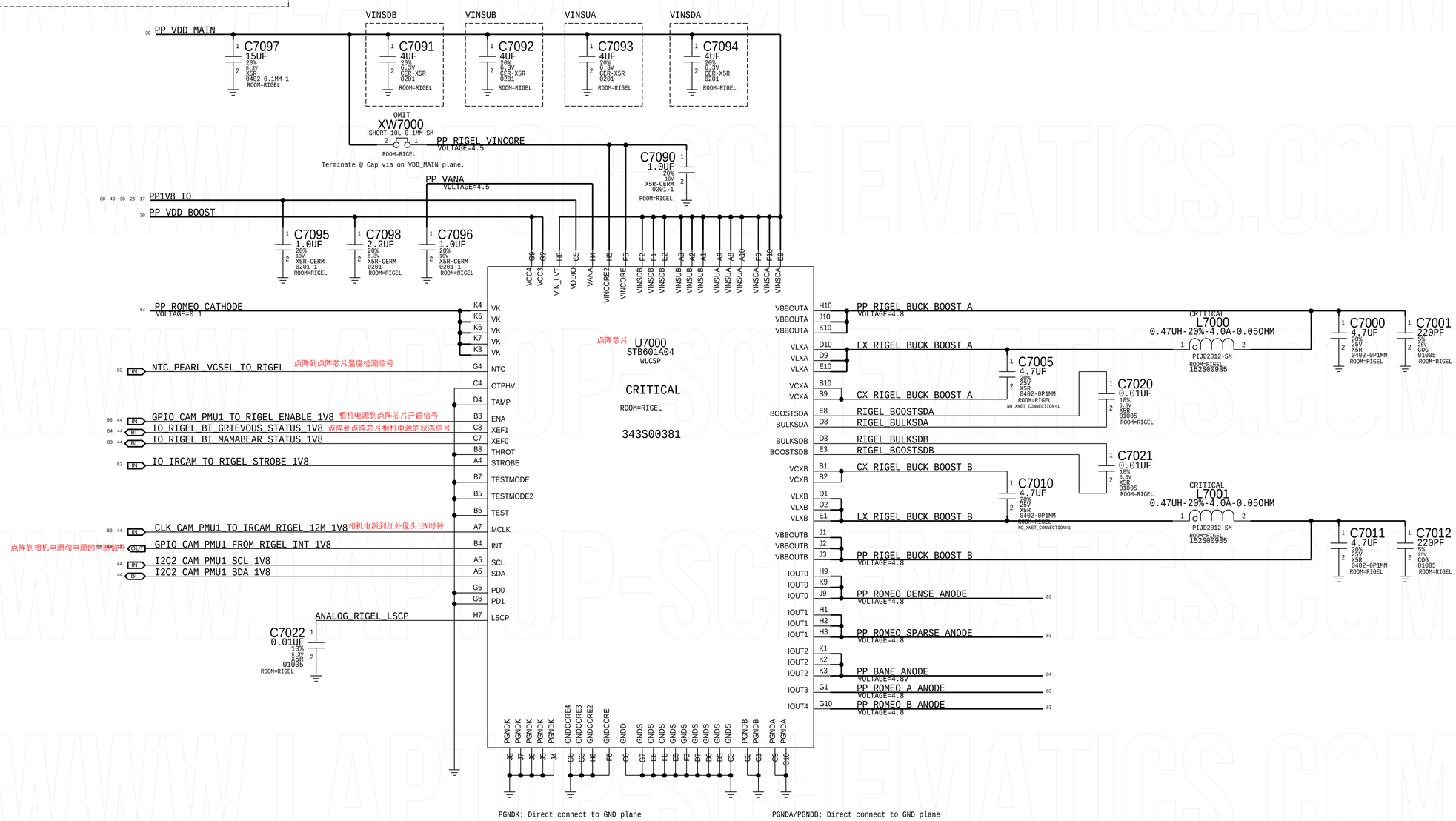
VCSEL DRIVER

RIGEL

SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR: Alt covered with PMU inductor BOM table



SYNCING: D52, D53, D54

PAGE TITLE	PEARL: VCSEL Driver
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	70 OF 138
SHEET	54 OF 117

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SYNCING: D52, D53, D54

PAGE TITLE
PEARL: Aliases

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH crb-1
PAGE 71 OF 138
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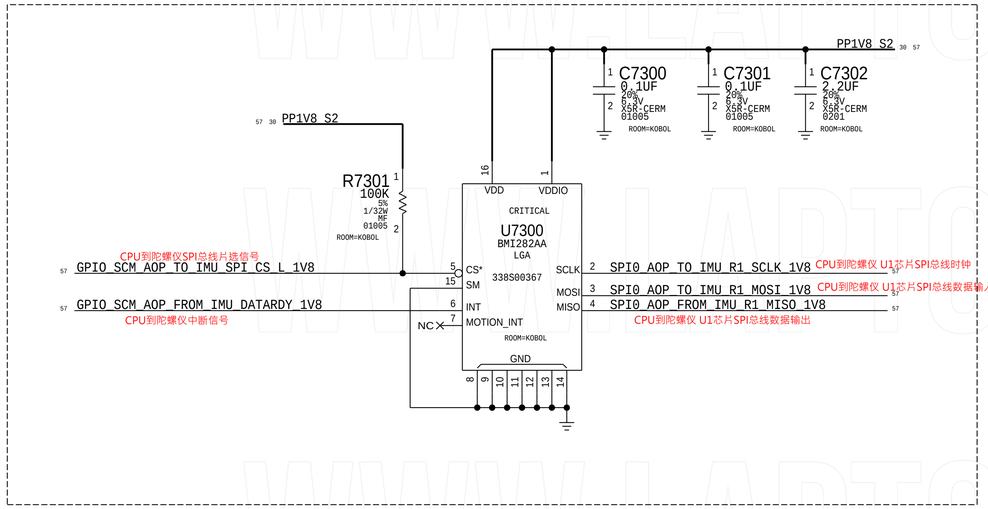
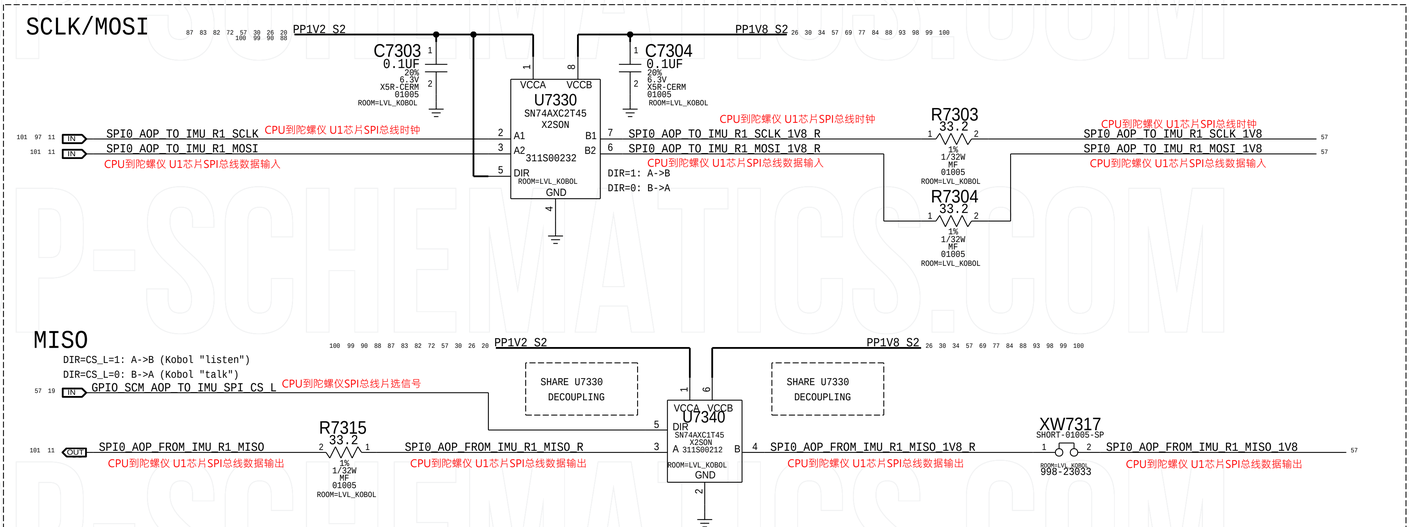
KOBOL - ACCEL & GYRO

IMU

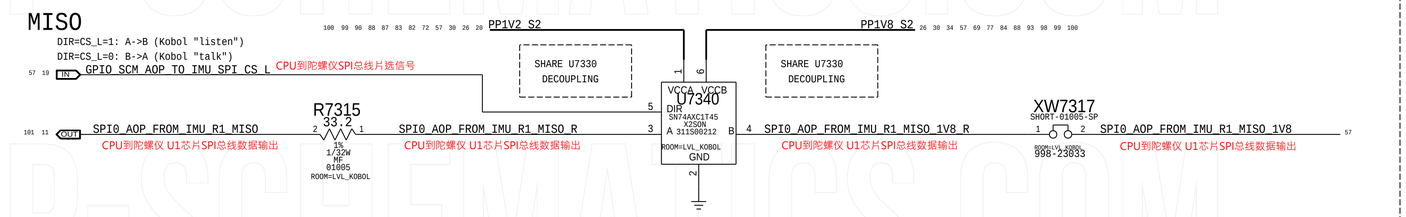


Level Translators

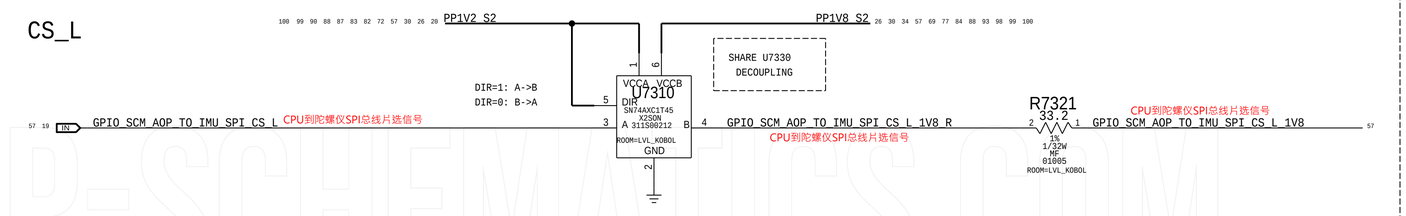
SCLK/MOSI



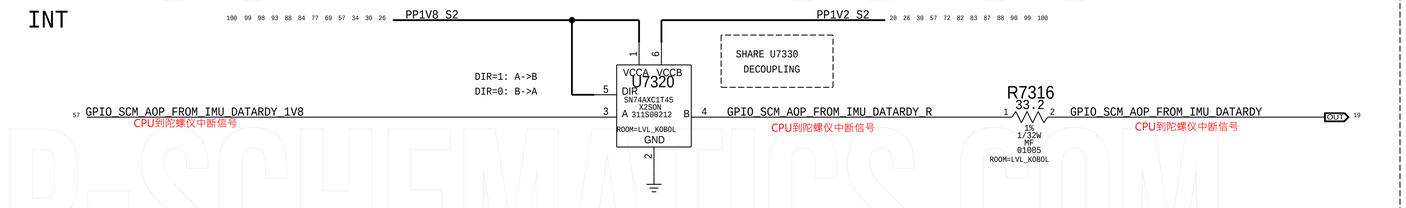
MISO



CS_L



INT



SYNCING: D52, D53, D54

PAGE TITLE	SENSORS: Accel / Gyro
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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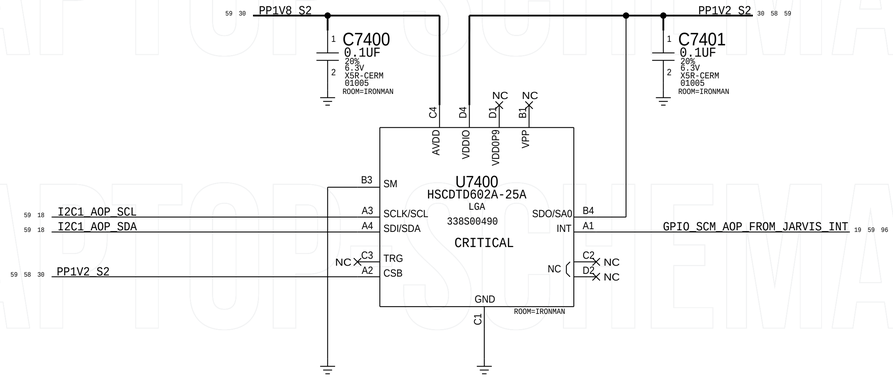
Jarvis (Top)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00665	338S00490	?	U7400	IC,COMPASS,MOL?BDC9(MP2,-25A,I2C,FLGA14



SYNCING: D52, D53, D54

PAGE TITLE	SENSORS: Jarvis (Top)
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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BRIGHTON AUDIO CODEC
(ANALOG INPUTS & OUTPUTS)

SUBSYSTEM SPECIFIC BOM TABLE

Codec

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00631	338S00509	?	U7800	IC,CODEC,BRIGHTON,CS42L77,A1,WLCSP144

CRITICAL PART#	COMMENT
338S00509	IC,CODEC,BRIGHTON,CS42L77,A1,WLCSP144

U7800
CS42L77A1
WLCSP
SYM 1 OF 4
CRITICAL
ROOM=CODEC
338S00509

MIC1_LOWER_TO_CODEC_AIN1_P — M8 AIN1+
MIC1_LOWER_TO_CODEC_AIN1_N 麦克风1数据N — L8 AIN1-

MIC2_REAR_TO_CODEC_AIN2_P 麦克风2数据P — M11 AIN2+
MIC2_REAR_TO_CODEC_AIN2_N 麦克风2数据N — L11 AIN2-

MIC3_FRONT_TO_CODEC_AIN3_P 麦克风3数据P — M9 AIN3+
MIC3_FRONT_TO_CODEC_AIN3_N 麦克风3数据N — L9 AIN3-

MIC4_LOWER_TO_CODEC_AIN4_P 麦克风4数据P — M10 AIN4+
MIC4_LOWER_TO_CODEC_AIN4_N 麦克风4数据N — L10 AIN4-

PENROSE_IR_TO_CODEC_AIN5_P — M3 AIN5A+
PENROSE_IR_TO_CODEC_AIN5_N — L3 AIN5A-

L4 AIN5B+
L5 AIN5B-

PENROSE_VIS_TO_CODEC_AIN6_P — K5 AIN6A+
PENROSE_VIS_TO_CODEC_AIN6_N — K4 AIN6A-

L2 AIN6B+
M2 AIN6B-

J2 AIN7+
K2 AIN7-

J3 AIN8+
K3 AIN8-

H3 AIN9+
H2 AIN9-

J4 AIN10+
J5 AIN10-

L6 AIN11+
L7 AIN11-

K7 AIN12+
K6 AIN12-

PDM_OUT1_CODEC_TO_SPKRAMP_TOP_CLK — A6 PDMOUT1_CLK
PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA — D6 PDMOUT1_DATA

B6 PDMOUT2_CLK
C6 PDMOUT2_DATA

AOUT+ F11 CODEC_AOUT_TO_HAC_P
AOUT- G11 CODEC_AOUT_TO_HAC_N

DP F1 90_MIKEYBUS_DATA_P_R
DN E1 90_MIKEYBUS_DATA_N_R
MBUS_REF E2 ANALOG_MIKEYBUS_REFERENCE

R7810 100 5% 1/32W MF 01005 ROOM=CODEC
Can be placed near Dock Connector

C7800 100PF 5% 16V NP0-C0G 01005-1 ROOM=CODEC
R7800 20.0 5% 1/32W MF 01005 ROOM=CODEC
90_MIKEYBUS_DATA_P
R7801 20.0 5% 1/32W MF 01005 ROOM=CODEC
90_MIKEYBUS_DATA_N
C7801 100PF 5% 16V NP0-C0G 01005-1 ROOM=CODEC

LDCM

TIA_EXOUT G4 NC
TIA_OUT G5
TIA_SENSE G1

HALOGEN_TIA_IOUT
C7820 220PF 5% 10V C0G 01005 ROOM=CODEC
R7821 200K 1% 1/32W MF 01005 ROOM=CODEC NO_XNET_CONNECTION=1
C7821 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=CODEC NO_XNET_CONNECTION=1
HALOGEN_TIA_IN
USB芯片到电源的数据线ID识别信号
IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA

SYNCING: D52, D53, D54

PAGE TITLE: AUDIO: Codec: Analog (1/2)
DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: crb-1
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BRIGHTON AUDIO CODEC
(POWER & I/O)

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30 PP_VDD_BOOST

Can reduce to 2.2uF
if located near BOOST

C7910 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=CODEC PACK_OPTION=DS4_DEV
C7910 4UF 20% 6.3V CER-X5R 0201 ROOM=CODEC PACK_IGNORE=TRUE PACK_OPTION=DS2_DS3
C7911 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC

63 30 PP1V8_S2
63 30 PP1V2_S2

C7921 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC PACK_IGNORE=TRUE PACK_OPTION=DS2
C7902 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CODEC PACK_IGNORE=TRUE PACK_OPTION=DS3
C7902 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC
C7903 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC
C7904 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC
C7905 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC
C7920 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=CODEC PLACE_NEAR=U7800.A4:2MM
C7901 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=CODEC PLACE_NEAR=U7800.H1:2MM
PACK_OPTION=DS2_DS4_DEV

26 PP1V8_AUDIO_VA_S2 音频1.8V供电

C7915 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CODEC
61 AGND_CODEC

U7800
CS42L77A1
WLCSP
SYM 4 OF 4
CRITICAL
ROOM=CODEC
338S00509

G12	VDD_P	GND_D0	A1
F2	VDD_MBUS	GND_D1	A12
H1	VDD_1P8	GND_D2	A8
E12	VIO_GPIO	GND_D3	B4
D10	VIO_I2C	GND_D4	C12
A5	VIO_SPI	GND_D5	D1
E3	VIO_MCLK	GND_D6	E6
A11	VIO_ASP	GND_D7	J1
B3	VIO_SWIRE	GND_D8	M1
A7	VIO_PDM		
A4	VDD_D0	GND_P0	F12
D12	VDD_D1	GND_P1	M12
M4	VDD_A		

I2C ADDRESS: 1001 010x

U7800
CS42L77A1
WLCSP
SYM 3 OF 4
CRITICAL
ROOM=CODEC
338S00509

96 19 IN GPIO_AOP_TO_CODEC_RESET_L CPU到音频芯片复位信号	H7	RESET*	GPIO3_JTAG_TRST* E10
29 OUT GPIO_PMU_FROM_CODEC_WAKE_L 电源到音频的唤醒信号	H8	WAKE*	GPIO4_JTAG_TDO D11
96 19 OUT GPIO_AP_FROM_CODEC_INT_L CPU到音频的中断信号	E11	INT*	GPIO5_JTAG_TMS F8
	E9	I2C_ADDR	GPIO2_JTAG_TDI F9
18 IN I2C2_AOP_SCL	C11	I2C_SCL	GPIO1_JTAG_TCK F10
18 BI I2C2_AOP_SDA	E8	I2C_SDA	
20 IN SPI3_AP_TO_CODEC_SCLK CPU到大音频的SPI总线时钟	B5	SPI_SCK	
96 20 IN SPI3_AP_TO_CODEC_CS_L CPU到大音频的SPI总线片选信号	E5	SPI_SS*	
96 20 IN SPI3_AP_TO_CODEC_MOSI CPU到大音频的SPI总线数据	D5	SPI_MOSI	
96 20 OUT SPI3_AP_FROM_CODEC_MISO 大音频到CPU的SPI总线数据	C5	SPI_MISO	
11 IN I2S0_AOP_TO_CODEC_MCLK1 CPU逻辑模块到音频的I2S0总线主时钟	C2	MCLK1_IN	TSTI D2
	D3	MCLK2_IN	TSTI J7
NC	C1	MCLK_OUT	TSTO H4 NC
CPU逻辑模块到音频的I2S0总线串行时钟 OUT I2S0_AOP_FROM_CODEC_ASP1_BCLK	B7	ASP1_BCLK	
CPU逻辑模块到音频的I2S0总线帧时钟 OUT I2S0_AOP_FROM_CODEC_ASP1_LRCLK	E7	ASP1_FSYNC	
CPU逻辑模块到音频的I2S0总线数据 IN I2S0_AOP_TO_CODEC_ASP1_DOUT	D7	ASP1_DIN	
音频到CPU逻辑模块的I2S0总线数据 OUT I2S0_AOP_FROM_CODEC_ASP1_DIN	C7	ASP1_DOUT	
CPU逻辑模块到音频的I2S1总线串行时钟 OUT I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK	A9	ASP2_BCLK	
CPU逻辑模块到音频的I2S1总线帧时钟 OUT I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK	D8	ASP2_FSYNC	
CPU逻辑模块到音频的I2S1总线数据 IN I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT	C8	ASP2_DIN	
音频到CPU逻辑模块的I2S1总线数据 OUT I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN	B8	ASP2_DOUT	
96 9 OUT I2S0_AP_FROM_CODEC_ASP3_BCLK 音频到CPU的I2S0总线串行时钟	A10	ASP3_BCLK	
96 9 OUT I2S0_AP_FROM_CODEC_ASP3_LRCLK 音频到CPU的I2S0总线帧时钟	D9	ASP3_FSYNC	
96 9 IN I2S0_AP_TO_CODEC_ASP3_DOUT CPU到音频的I2S0总线数据	C9	ASP3_DIN	
96 9 OUT I2S0_AP_FROM_CODEC_ASP3_DIN 音频到CPU的I2S0总线数据	B9	ASP3_DOUT	
96 9 OUT I2S1_AP_FROM_CODEC_ASP4_BCLK 音频到CPU的I2S1总线串行时钟	B12	ASP4_BCLK	
96 9 OUT I2S1_AP_FROM_CODEC_ASP4_LRCLK 音频到CPU的I2S1总线帧时钟	C10	ASP4_FSYNC	
96 9 IN I2S1_AP_TO_CODEC_ASP4_DOUT CPU到音频的I2S1总线数据	B10	ASP4_DIN	
96 9 OUT I2S1_AP_FROM_CODEC_ASP4_DIN 音频到CPU的I2S1总线数据	B11	ASP4_DOUT	
	C4	SWIRE1_CLK0	
	A2	SWIRE1_CLK1	
	A3	SWIRE1_CLK2	
	C3	SWIRE1_DATA0	
	D4	SWIRE1_DATA1	
	E4	SWIRE1_DATA2	
	B1	SWIRE2_CLK0	
	B2	SWIRE2_CLK1	
	F4	SWIRE2_DATA0	
	F7	CLP_EN	

音频MIC线路偏压信号

86 IN PP_CODEC_TO_MIC1_LOWER_BIAS VOLTAGE=2.9
86 IN RET_CODEC_FROM_MIC1_LOWER
85 IN PP_CODEC_TO_MIC2_REAR_BIAS VOLTAGE=2.9
85 IN RET_CODEC_FROM_MIC2_REAR
84 IN PP_CODEC_TO_MIC3_FRONT_BIAS VOLTAGE=2.9
84 IN RET_CODEC_FROM_MIC3_FRONT
86 IN PP_CODEC_TO_MIC4_LOWER_BIAS VOLTAGE=2.9
86 IN RET_CODEC_FROM_MIC4_LOWER

C7928 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=CODEC
C7927 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=CODEC
C7926 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=CODEC
C7925 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=CODEC

U7800
CS42L77A1
WLCSP
SYM 2 OF 4
CRITICAL
ROOM=CODEC
338S00509

K9	MIC1_BIAS	MIC_FILT+ H12	CODEC_MIC_FILTP
J9	MIC1_BIAS_REF	MIC_FILT- J12	61 AGND_CODEC
K11	MIC2_BIAS	LP_FILT+ K1	CODEC_LP_FILTP
J10	MIC2_BIAS_REF	LP_FILT- L1	CODEC_LP_FILTN
L12	MIC3_BIAS	FILT+ M7	CODEC_FILTP
K10	MIC3_BIAS_REF	FILT- M6	61 AGND_CODEC
K12	MIC4_BIAS		
H9	MIC4_BIAS_REF		
NC H11	MIC5_BIAS		
NC G9	MIC5_BIAS_REF		
NC J11	MIC6_BIAS		
NC G10	MIC6_BIAS_REF		
G10	MICBIAS_DIS		

C7930 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CODEC NO_XNET_CONNECTION=1
C7931 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CODEC NO_XNET_CONNECTION=1
C7932 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=CODEC NO_XNET_CONNECTION=1

GND_A0	F3		
GND_A1	F5		
GND_A2	G7		
GND_A3	G8		
GND_A4	H5		
GND_A5	H6		
GND_A6	J6		
GND_A7	J8		
GND_A8	K8		
GND_A9	M5		
GND_A10	F6		
GND_A11	G2		
GND_A12	G3		
GND_A13	G6	61 AGND_CODEC	

OMIT
XW7902
SHORT-10L-0.1MM-SM
ROOM=CODEC
NO_XNET_CONNECTION

SYNCING: D52, D53, D54

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PAGE TITLE	AUDIO: Codec: Power & I/O (2/2)
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
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BOT SPEAKER AMP

ALLSTON

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POWER DOMAIN NOTES:
1. Use S4 domain if possible, then GND VD_FILT_SEL
2. Can use S2 domain if routing constrained, then NC VD_FILT_SEL

62 30 PP1V2_S4
C8008 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK

30 PP1V8_S4
C8007 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK

PP_VA_BOT_SPK_INTERNAL
VOLTAGE=1.8
C8006 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK
AGND_BOT_SPK 62

62 30 PP1V2_S4

ANALOG_BOT_SPK_FILT
C8009 1.0UF 20% 6.3V X5R 0201-1 ROOM=BOT_SPK NO_XNET_CONNECTION=1
AGND_BOT_SPK 62

18 IN I2C2_AOP_SCL
18 BI I2C2_AOP_SDA
CPU逻辑模块到音频的I2S1总线 时钟
IN I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK
CPU逻辑模块到音频的I2S1总线 时钟
IN I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK
CPU逻辑模块到音频的I2S1总线 数据
IN I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT
CPU逻辑模块到音频的I2S1总线 帧时钟
IN I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK
音频到CPU逻辑模块的I2S1总线 数据
OUT I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN

VD_FILT_SEL: NC = internal LDO (use if S2 power domain)
GND = external power (use if S4 power domain)
96 29 IN GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L 电源到喇叭功放的复位
NC
96 65 63 OUT IO_SPKRAMP_TO_SPKRAMP_SYNC 听筒功放到喇叭功放的同步信号
98 IN GPIO_BT_TO_BOT_SPKR_TRIG
R8050 100K 5% 1/32W MF 01005 ROOM=BOT_SPK

OMIT
XW8000 SHORT-10L-0.1MM-SM
62 AGND_BOT_SPK
ROOM=BOT_SPK NO_XNET_CONNECTION

Place off of Allston GND pin

U8000 CS35L27A WLCSP CRITICAL 338S00537 ROOM=BOT_SPK

H2	VA	
H6	VL	
H7	VD_FILT	
H3	VP	
A1,A2,C5,C6,C7	VPB	
E7	VASP	
F7	VSWIRE	
H1	FILT+	
F5	PDM1_CLK/SWIRE_CLK	
F6	PDM1_DATA/SWIRE_SD1	
G7	PDM2_CLK	NC
G6	PDM2_DATA	
F4	SWIRE_SD2	
D5	SCL	
D4	SDA	
E6	MCLK	
E5	SCLK	
D6	SDIN	
D7	FSYNC	
E4	SDOUT	
C3	VD_FILT_SEL	
H4	RESET*	
G4	INT*	NC
H5	SYNC	
G3	AD0/GPI	
G2	AD1	
G1	GNDA	
A6,B3,B6,C4,C5	GNDB	
D3,E3,F3	GNDD	
	GNDP	
A5,B5	CF1+	
A7,B7	CF1-	CX_BOTSPK_P1_NEG
A3,B1,B2	CF2+	CX_BOTSPK_P2_POS
A4,B4	CF2-	CX_BOTSPK_P2_NEG
C1,C2	VBST	
D1,E1	VSPK	
E2	OUT+	底部喇叭数据P SPKRAMP_BOT_TO_COIL_OUT_POS 96
D2	OUT-	底部喇叭数据N SPKRAMP_BOT_TO_COIL_OUT_NEG 96
F2	VSNS+	底部喇叭数据P检测 COIL_TO_SPKRAMP_BOT_VSENSE_POS 96
F1	VSNS-	底部喇叭数据N检测 COIL_TO_SPKRAMP_BOT_VSENSE_NEG 96

Placement Notes:
A1,A2: 15uF (1x), 2.2uF(1x)
C5,C6,C7: 15uF (2x)

PP_VDD_MAIN 30 63 65
C8003 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BOT_SPK
CRITICAL C8000 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK
CRITICAL C8001 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK
CRITICAL C8002 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK
CRITICAL C8004 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BOT_SPK

CRITICAL C8030 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=BOT_SPK NO_XNET_CONNECTION=1
CRITICAL C8040 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=BOT_SPK NO_XNET_CONNECTION=1

VOLTAGE=12.0
底部喇叭功放升压供电 PP_SPKRAMP_BOT_VBOOST
CRITICAL C8020 4.2UF 10% 10V X5R-CERM 0402-0.1MM ROOM=BOT_SPK
CRITICAL C8021 4.2UF 10% 10V X5R-CERM 0402-0.1MM ROOM=BOT_SPK
CRITICAL C8022 4.2UF 10% 10V X5R-CERM 0402-0.1MM ROOM=BOT_SPK
C8025 1UF 20% 10V CER-XSR 0201 ROOM=BOT_SPK
C8023 220PF 5% 25V C0G 01005 ROOM=BOT_SPK
C8024 2200PF 10% 16V X5R-CERM 01005 ROOM=BOT_SPK

SYNCING: D52, D53, D54

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-	
DRAWING NUMBER	051-05170
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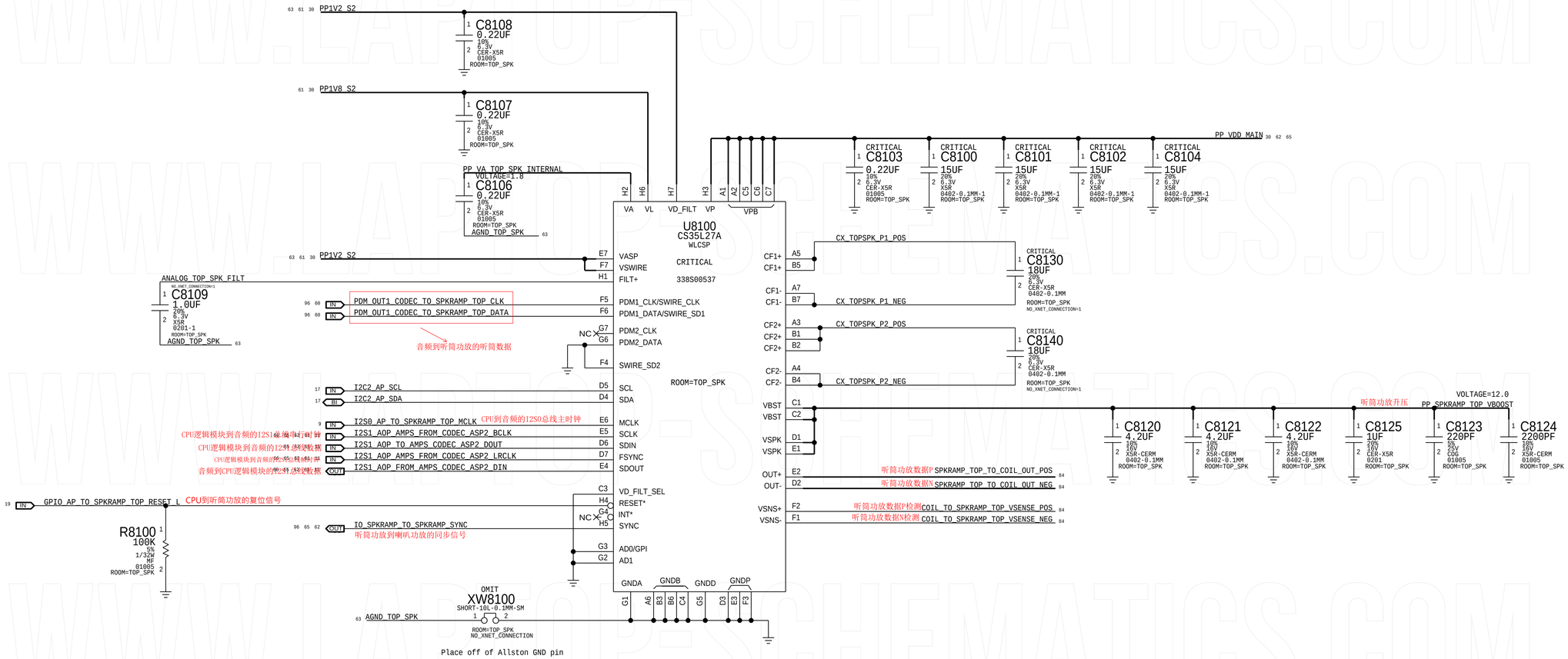
TOP SPEAKER AMP

ALLSTON



SYNCING: D52, D53, D54

PAGE TITLE	AUDIO: Top Speaker Amp
-	
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SYNCING: D52, D53, D54

SYNC_MASTER=0.143.0	SYNC_DATE=05/14/2019
PAGE TITLE	AUDIO: Aliases
DRAWING NUMBER	051-05170
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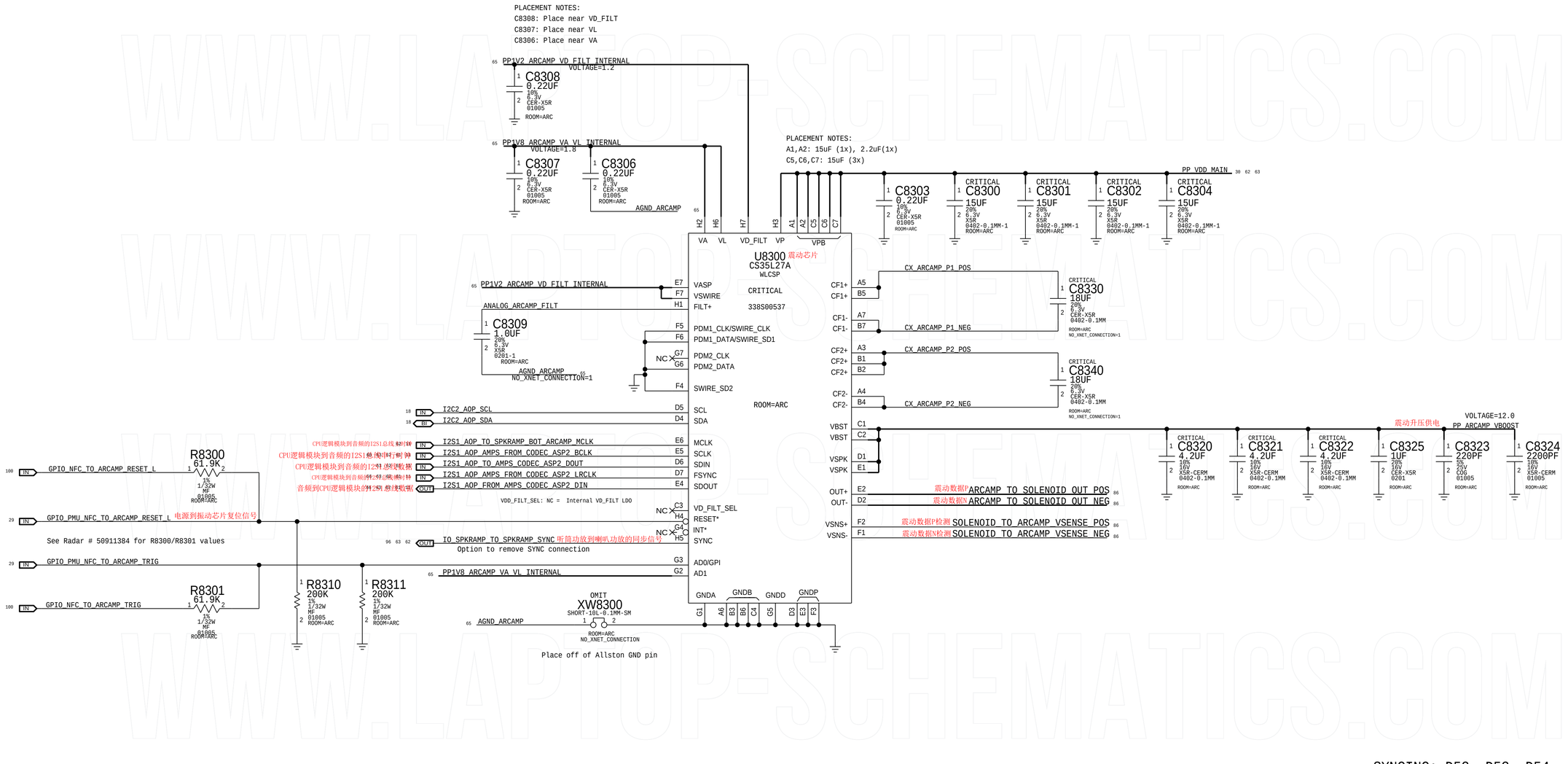
ARC SPEAKER AMP

ALLSTON



SYNCING: D52, D53, D54

PAGE TITLE	HAPTIC: Haptic Amp
DRAWING NUMBER	051-05170
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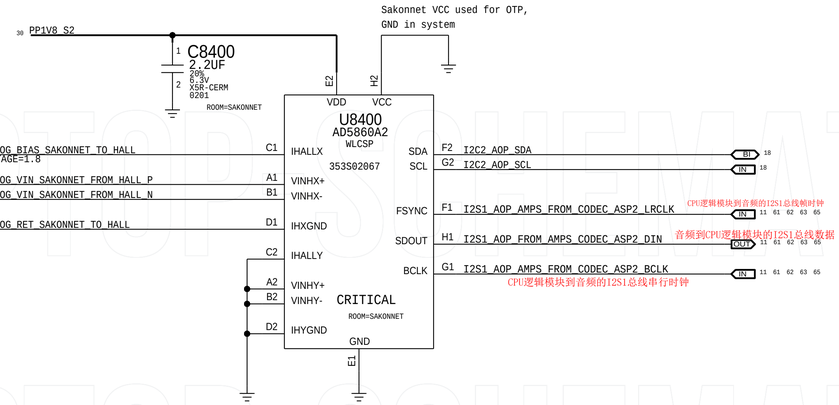
HALL SENSOR

SAKONNET



SYNCING: D52, D53, D54

PAGE TITLE	HAPTIC: Sakonnet
DRAWING NUMBER	051-05170
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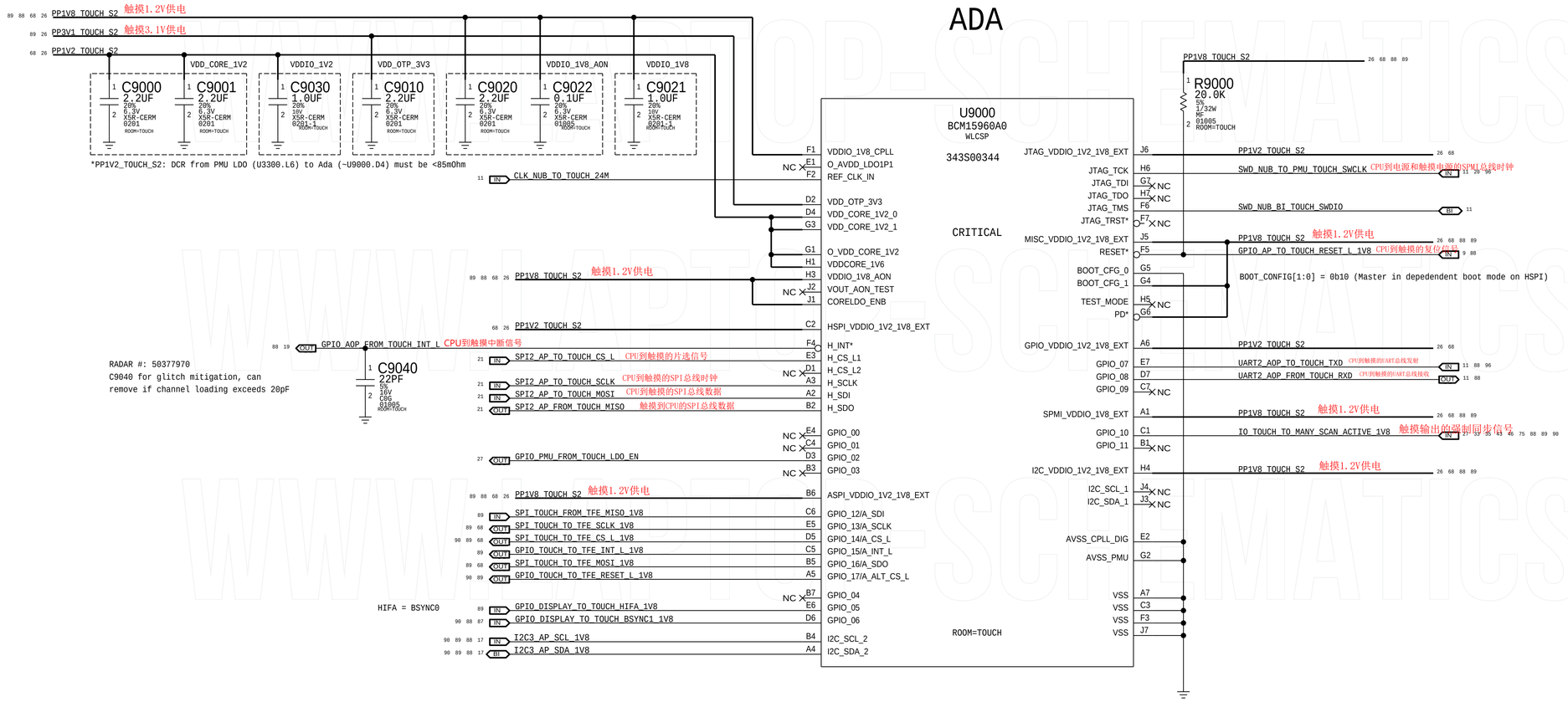

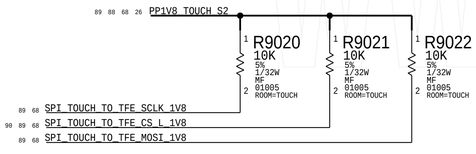

SYNCING: D52, D54

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PAGE TITLE: TOP MODULE: Touch Processor

DRAWING NUMBER: 051-05170 SIZE: D
REVISION: 10.0.0
BRANCH: crb-1
PAGE: 90 OF 138
SHEET: 65 OF 117

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DISPLAY PMIC

GALENA/CHELAN

Galena vs. Chelan2

D52/D53P = Chelan2 , D53G/D54 = Galena A2E1

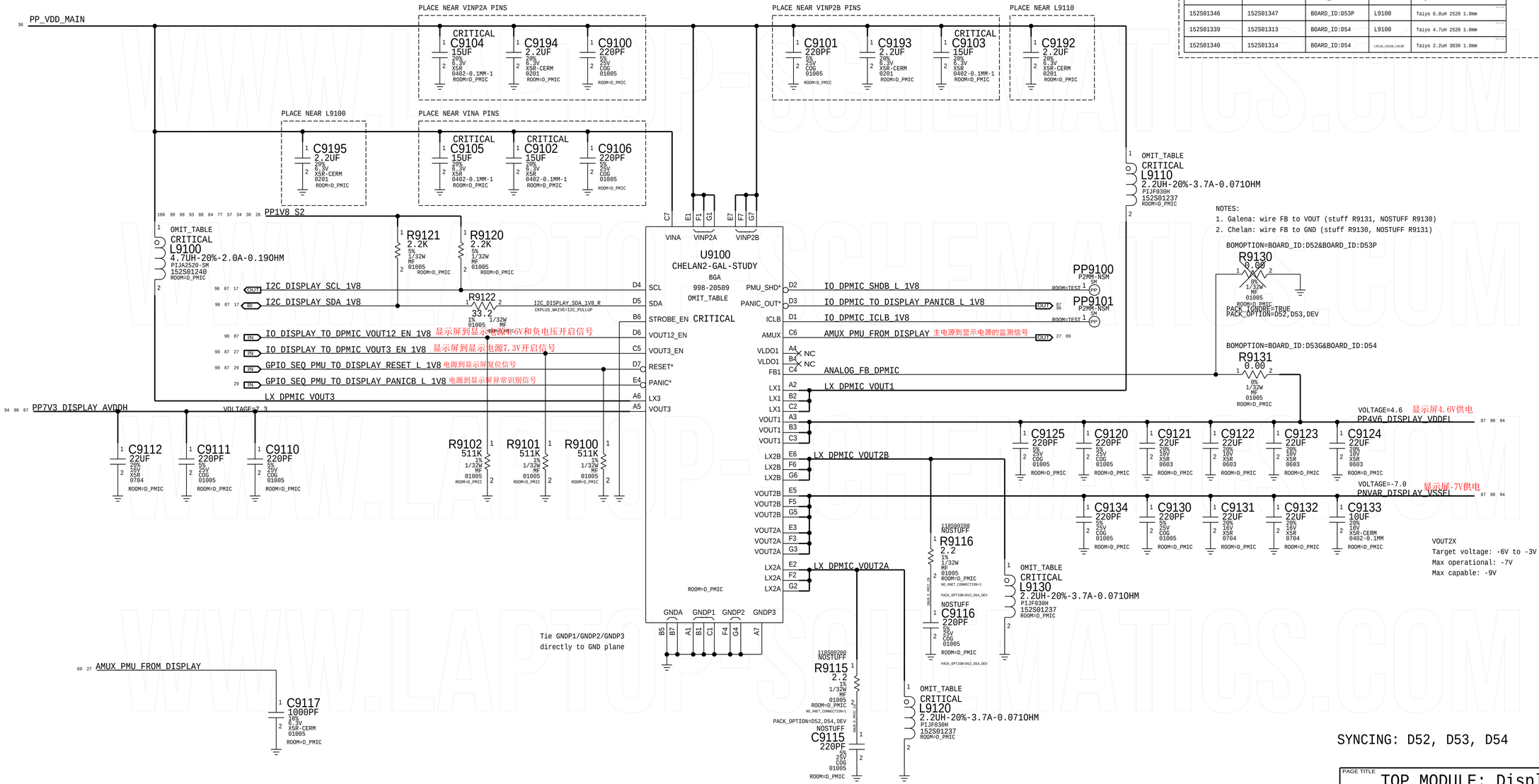
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00655	1	Galena A2 OTP-1 (A2E1)	U9100	CRITICAL	BOARD_ID:D53G&BOARD_ID:D54
338S00578	1	Chelan	U9100	CRITICAL	BOARD_ID:D52&BOARD_ID:D53P

Inductors

D52/D53P = Taiyo on VOUT3, D53G = no Taiyo, D54 = all Taiyo

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S01355	1	Cyntec VOUT3 Inductor (6.8uH 2520 0.95mm)	L9100	CRITICAL	BOARD_ID:D52
152S01347	1	Cyntec VOUT3 Inductor (6.8uH 2520 1.0mm)	L9100	CRITICAL	BOARD_ID:D53P
152S01313	1	Cyntec VOUT3 Inductor (4.7uH 2520 1.0mm)	L9100	CRITICAL	BOARD_ID:D53G&BOARD_ID:D54
152S01237	1	Cyntec VOUT1/2 Inductor (2.2uH 3030 0.8mm)	L9110	CRITICAL	BOARD_ID:D52
152S01357	2	Cyntec VOUT1/2 Inductor (2.2uH 3030 0.95mm)	L9120, L9130	CRITICAL	BOARD_ID:D52
152S01314	3	Cyntec VOUT1/2 Inductor (2.2uH 3030 1.0mm)	L9110, L9120, L9130	CRITICAL	BOARD_ID:D53G&BOARD_ID:D53P&BOARD_ID:D54

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01356	152S01355	BOARD_ID:D52	L9100	Taiyo 6.8uH 2520 0.95mm
152S01346	152S01347	BOARD_ID:D53P	L9100	Taiyo 6.8uH 2520 1.0mm
152S01339	152S01313	BOARD_ID:D54	L9100	Taiyo 4.7uH 2520 1.0mm
152S01340	152S01314	BOARD_ID:D54	L9110,L9120,L9130	Taiyo 2.2uH 3030 1.0mm



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PAGE TITLE: TOP MODULE: Display Power

DRAWING NUMBER: 051-05170 SIZE: D
REVISION: 10.0.0
BRANCH: crb-1
PAGE: 91 OF 138
SHEET: 66 OF 117

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SUBSYSTEM SPECIFIC BOM TABLES

LIGHTNING CONTROLLER

KRAKEN

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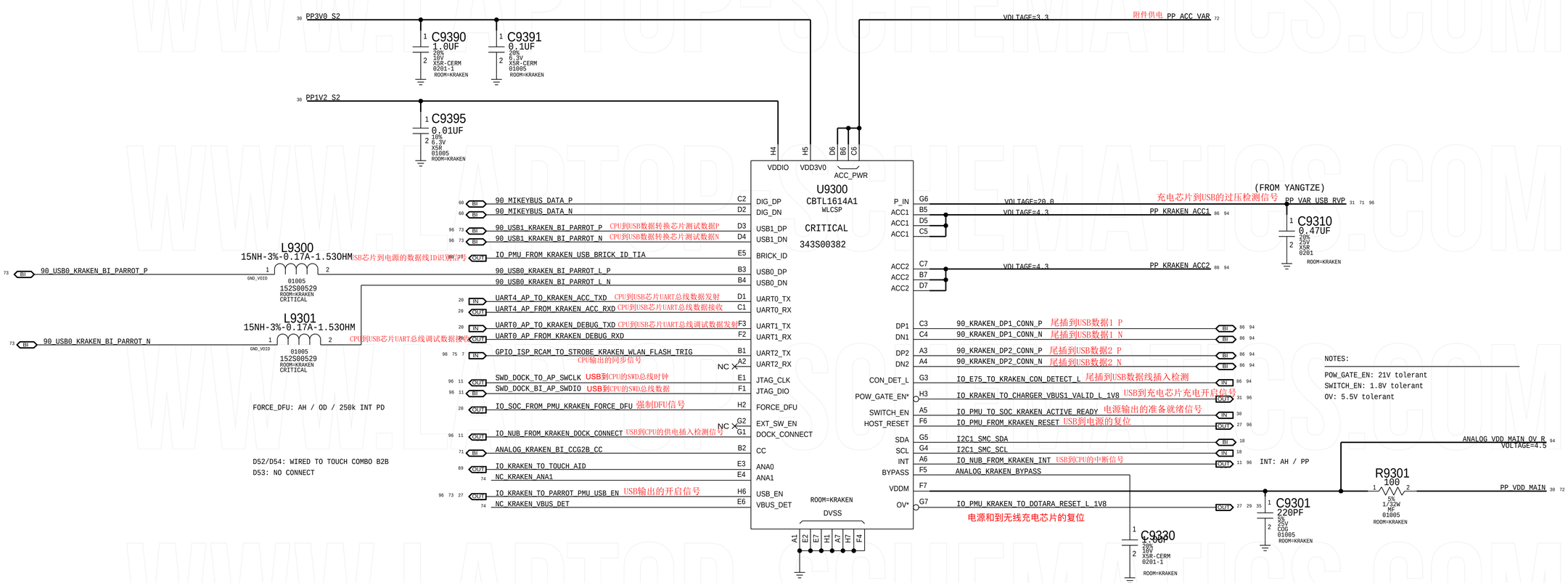
I2C Address: 0011010X



SYNCING: D52, D53, D54

PAGE TITLE	LIGHTNING: Lightning Controller
-	
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	93 OF 138
SHEET	67 OF 117

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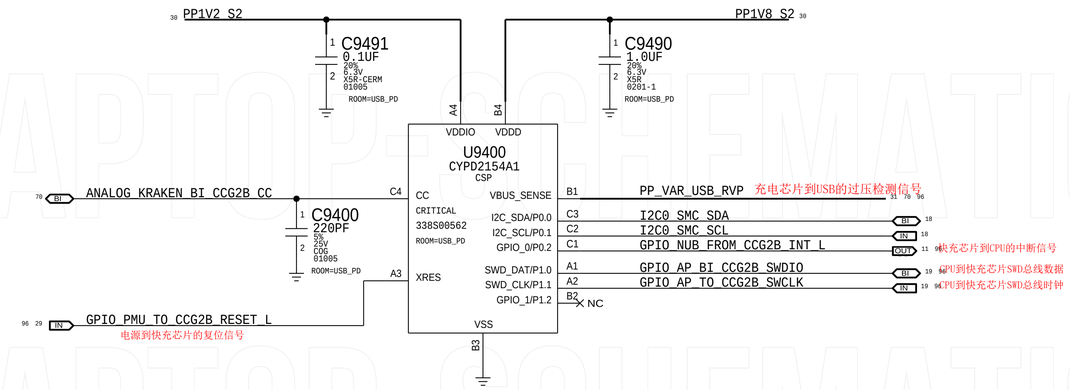
USB-PD

CCG2B



SYNCING: D52, D53, D54

PAGE TITLE	LIGHTNING: USB-PD
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	94 OF 138
SHEET	68 OF 117

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ACCESSORY POWER

GECKO2

SUBSYSTEM SPECIFIC BOM TABLES

Inductor

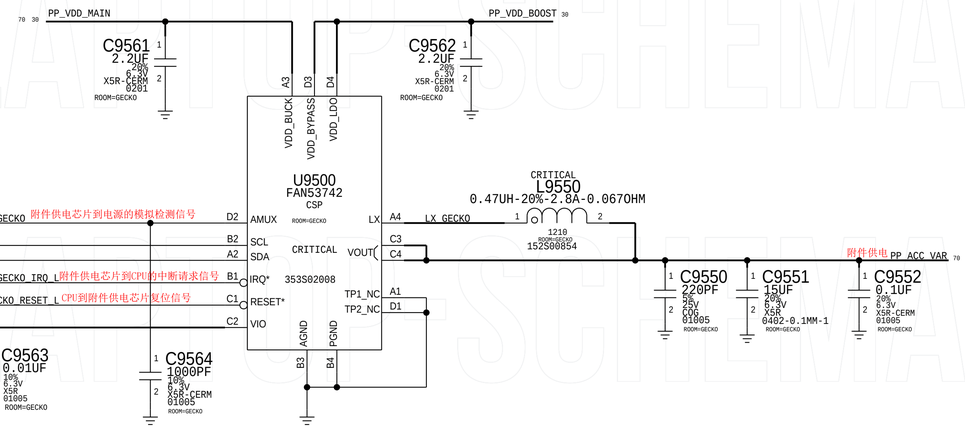
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01279	152S00854	?	L9550	IND,PWR,0.47UH,20%,2.7A,TY

Output Capacitor (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C9551)	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

I2C ADDRESS: 0X52



SYNCING: D52, D53, D54

PAGE TITLE	LIGHTNING: Accessory Buck
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	95 OF 138
SHEET	69 OF 117

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USB REPEATER

PARROT

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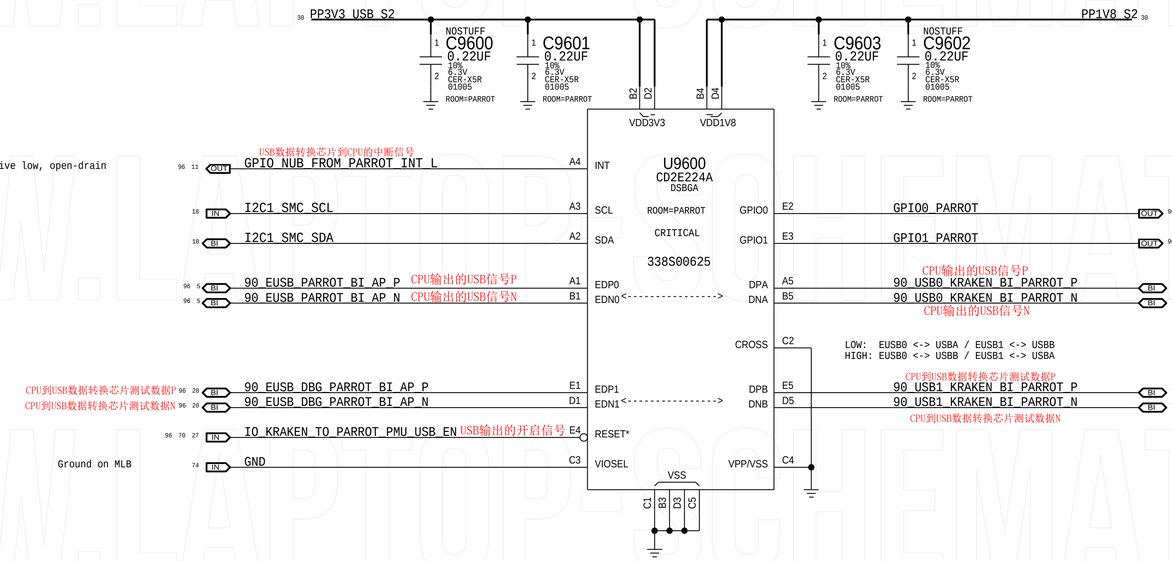
[LAYOUT] Parrot layout guidelines:
1. 3.3V power pins are shorted together internally, as are 1.8V pins
2. Keep decoupling cap <3mm from power pin
3. Minimize coupling between 1.8V and 3.3V rails



PLACE PARROT NEAR SOC

SYNCING: D52, D53, D54, DEV

PAGE TITLE	LIGHTNING: eUSB
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	96 OF 138
SHEET	70 OF 117

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70 NC_KRAKEN_VBUS_DET — NC_KRAKEN_VBUS_DET
MAKE_BASE=TRUE
NO_TEST=1

70 NC_KRAKEN_ANA1 — NC_KRAKEN_ANA1
MAKE_BASE=TRUE
NO_TEST=1

73 GND

LOW: 1.2V IO / HIGH: 1.8V IO

SYNCING: D52, D53, D54

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PAGE TITLE
LIGHTNING: Aliases

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH crb-1
PAGE 97 OF 138
SHEET 71 OF 117

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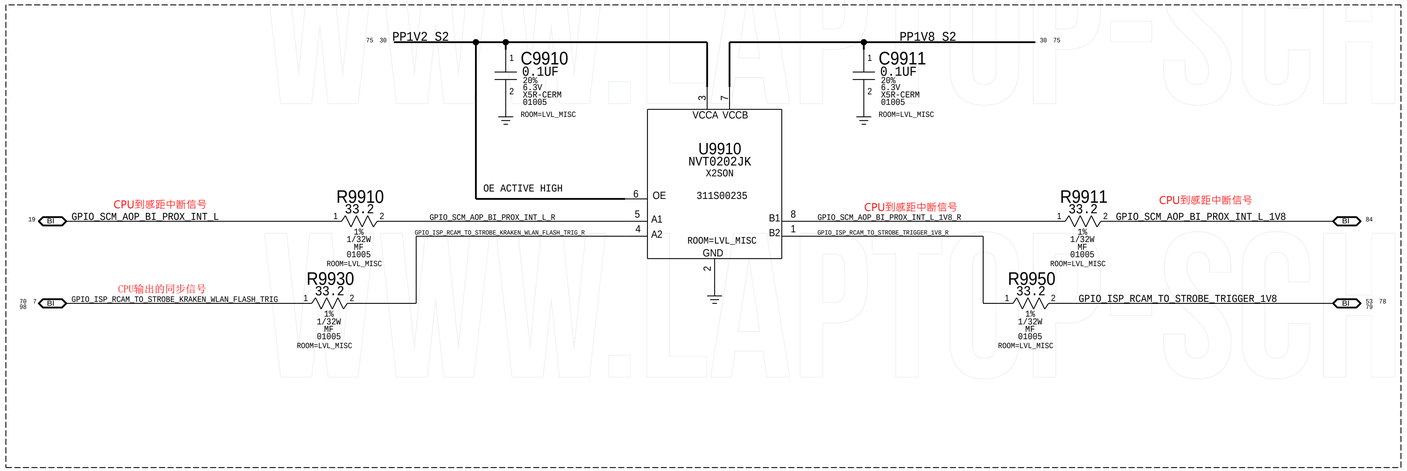
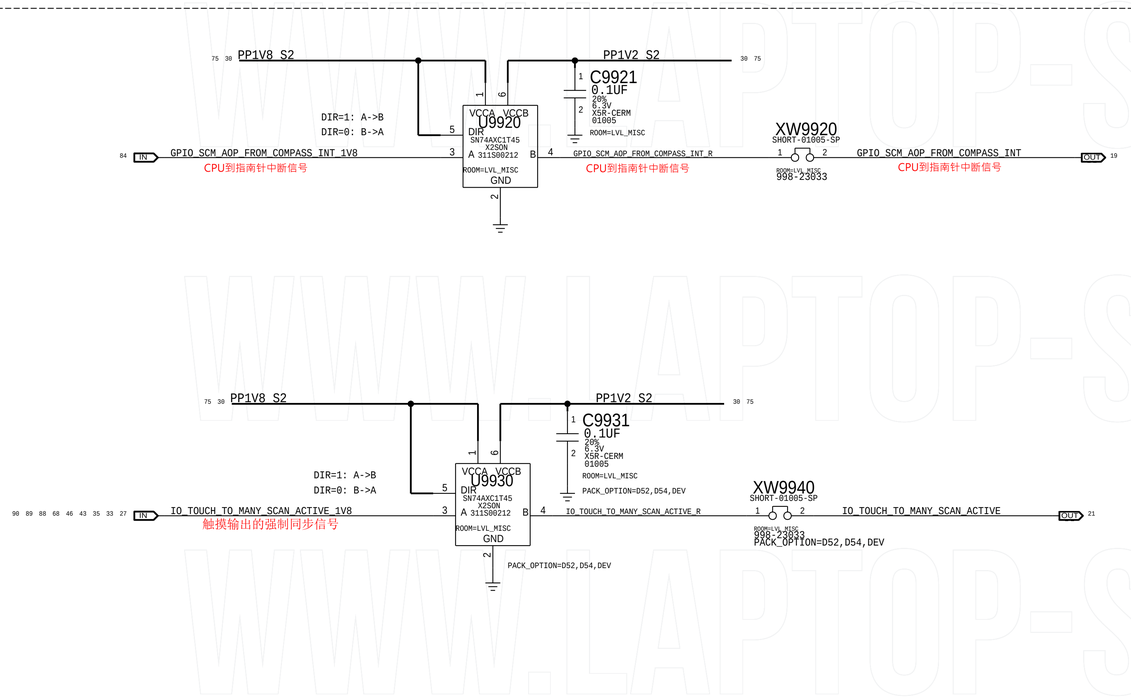
MISCELLANEOUS LEVEL TRANSLATORS

PROX INTERRUPT + STROBE TRIGGER



TOUCH SCAN ACTIVE + COMPASS INTERRUPT



SYNCING: D52, D53, D54, DEV

PAGE TITLE	LVL SHIFT: Misc Nets
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	99 OF 138
SHEET	72 OF 117

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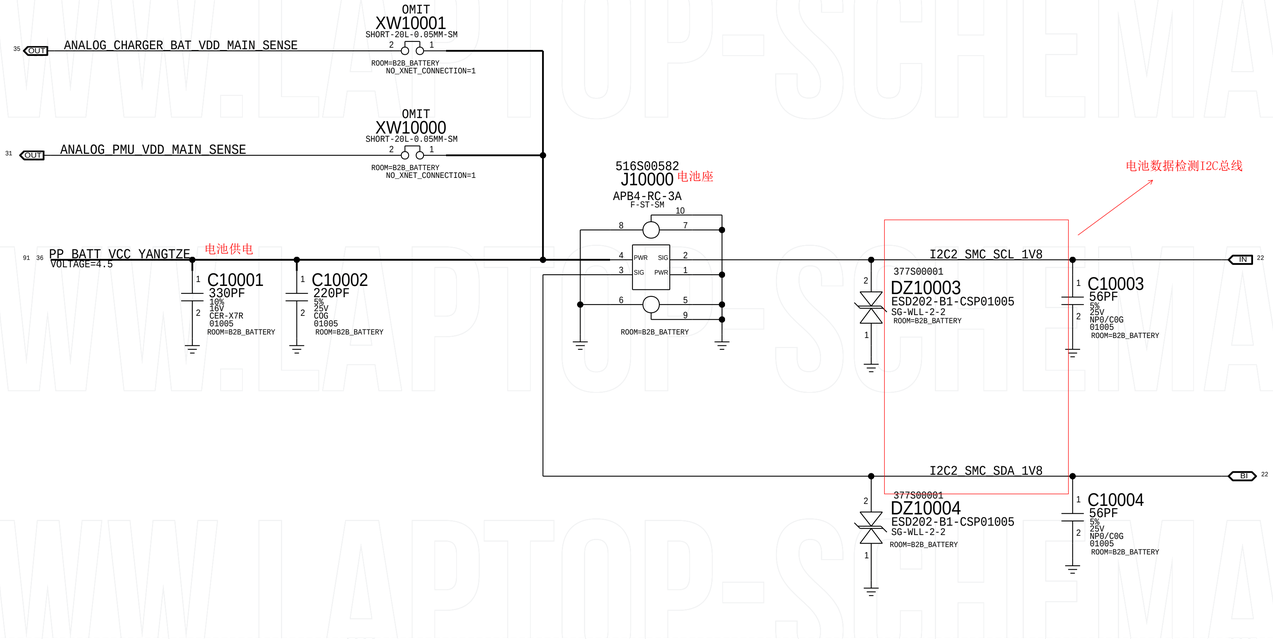
BATTERY B2B

CONNECTOR



NOT SYNCING

PAGE TITLE	B2B: Battery
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	100 OF 138
SHEET	73 OF 117

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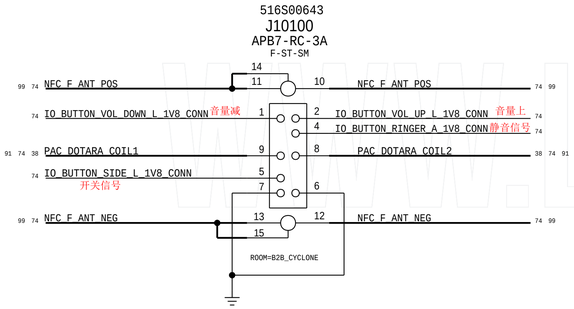
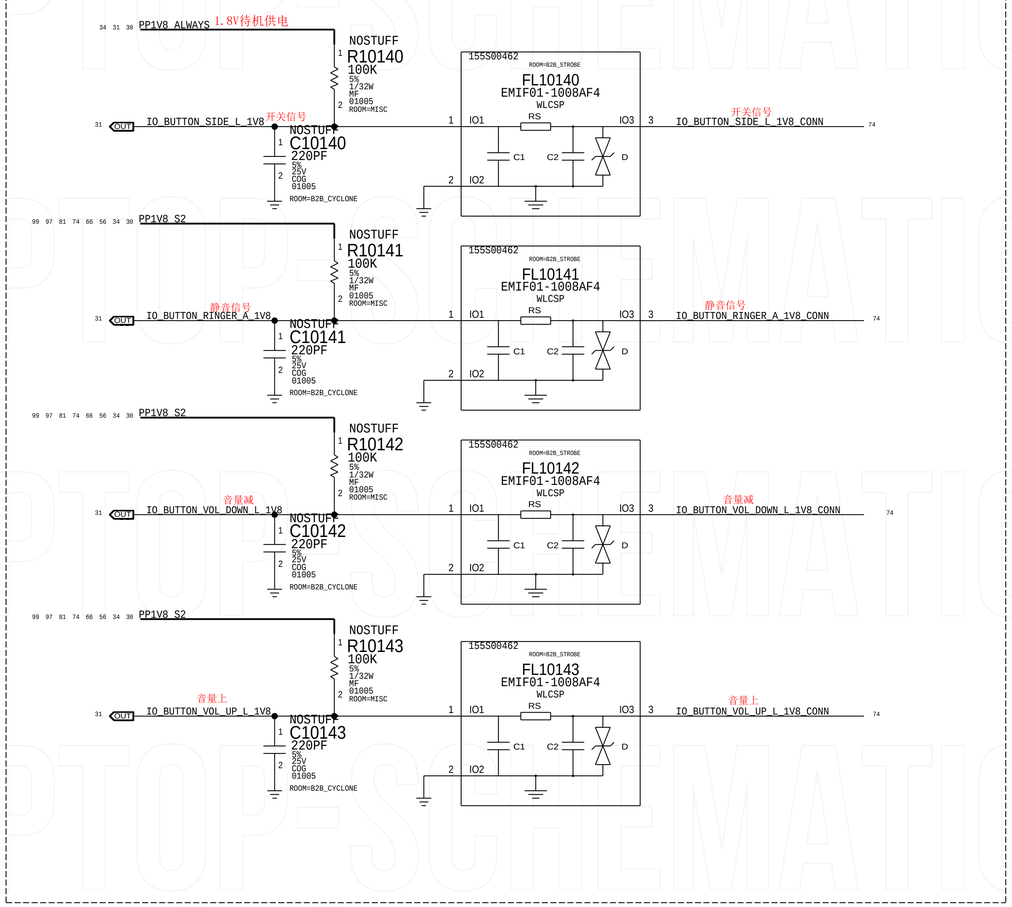
CYCLONE B2B

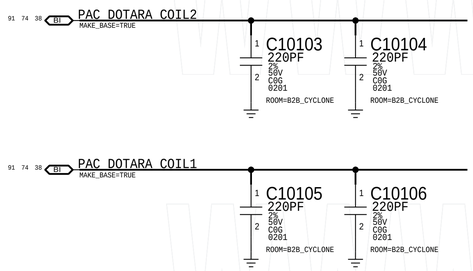
CONNECTOR



IO FILTERS



POWER FILTERS



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PAGE TITLE: B2B: Cyclone

DRAWING NUMBER: 051-05170 | SIZE: D

REVISION: 10.0.0

BRANCH: crb-1

PAGE: 101 OF 138

SHEET: 74 OF 117

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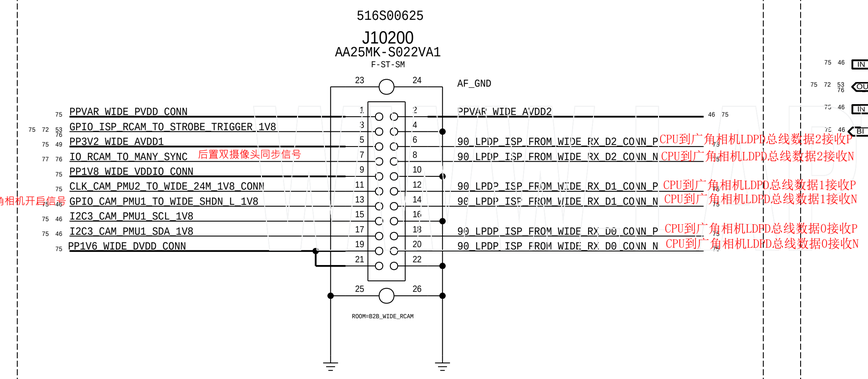
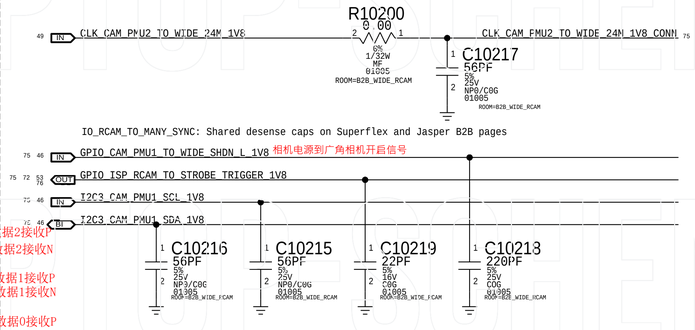
WIDE CAMERA B2B

CONNECTOR



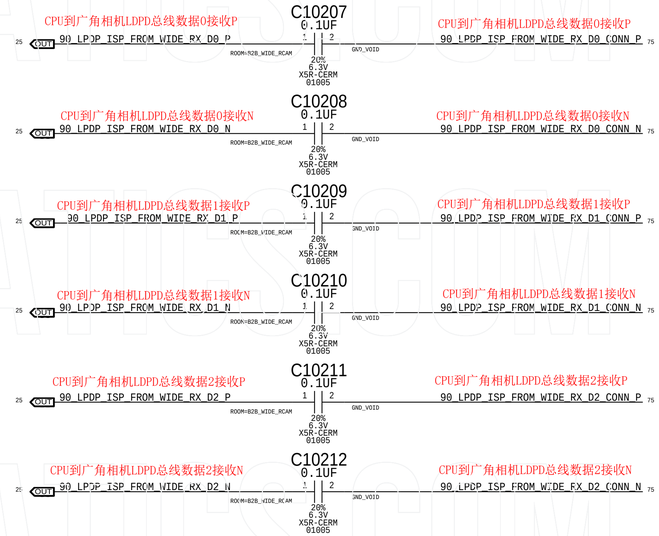
CPU到广角相机LDPD总线数据2接收P
CPU到广角相机LDPD总线数据2接收N
后置双摄像头同步信号
CPU到广角相机LDPD总线数据1接收P
相机电源到广角相机开启信号
CPU到广角相机LDPD总线数据1接收N
CPU到广角相机LDPD总线数据0接收P
CPU到广角相机LDPD总线数据0接收N

IO FILTERS



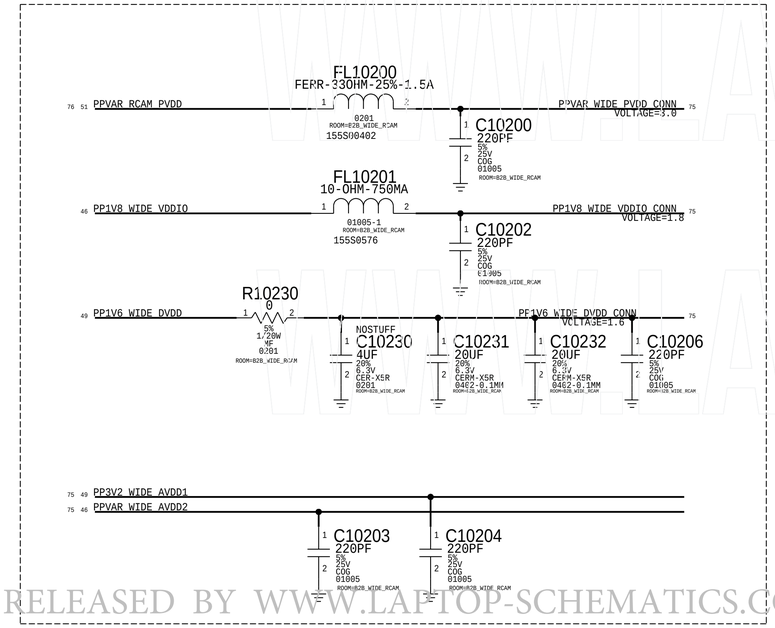
相机电源到广角相机开启信号

LPDP FILTERS



CPU到广角相机LDPD总线数据0接收P
CPU到广角相机LDPD总线数据0接收N
CPU到广角相机LDPD总线数据1接收P
CPU到广角相机LDPD总线数据1接收N
CPU到广角相机LDPD总线数据2接收P
CPU到广角相机LDPD总线数据2接收N

POWER FILTERS



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PAGE TITLE	B2B: Camera Wide
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	102 OF 138
SHEET	75 OF 117

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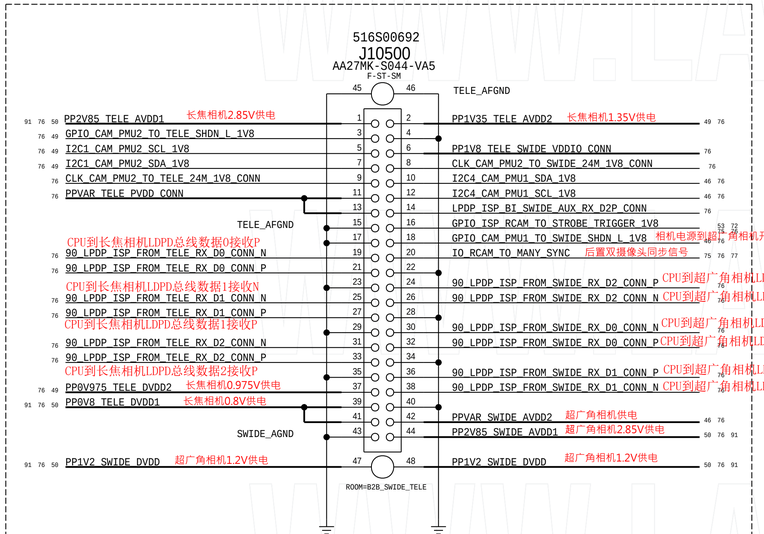
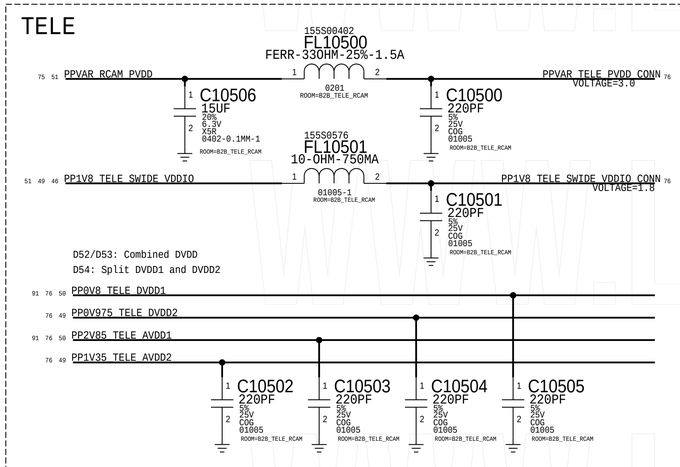
SUPERFLEX B2B
SWIDE + TELE COMBO

CONNECTOR

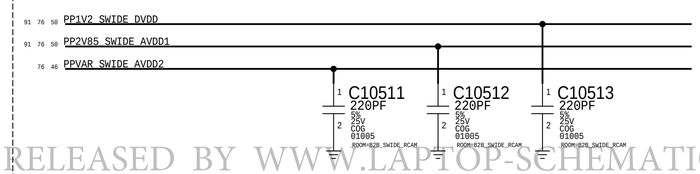


POWER FILTERS

TELE

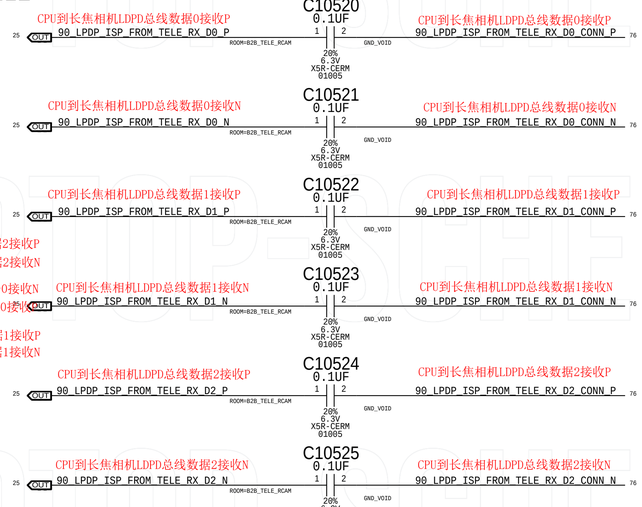


SWIDE

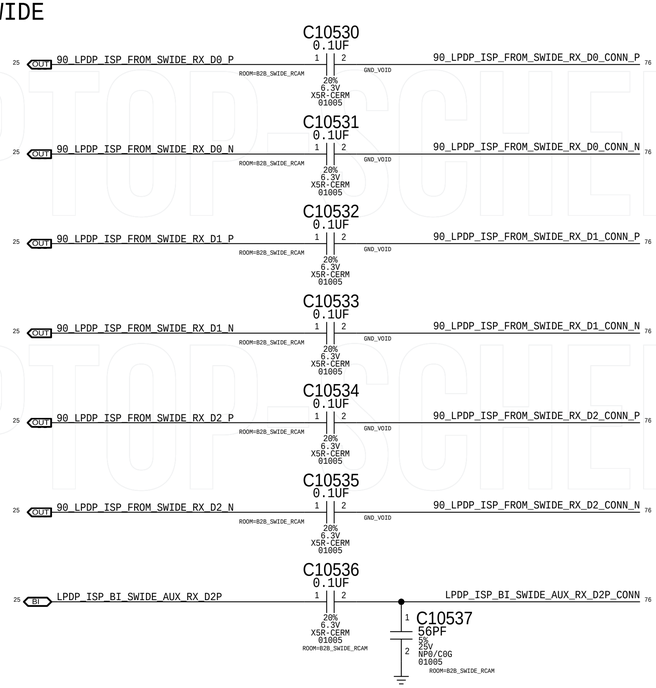


LPDP FILTERS

TELE

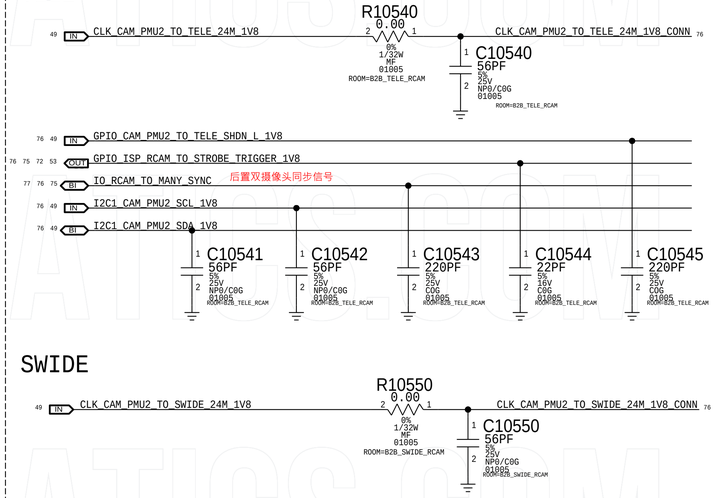


SWIDE

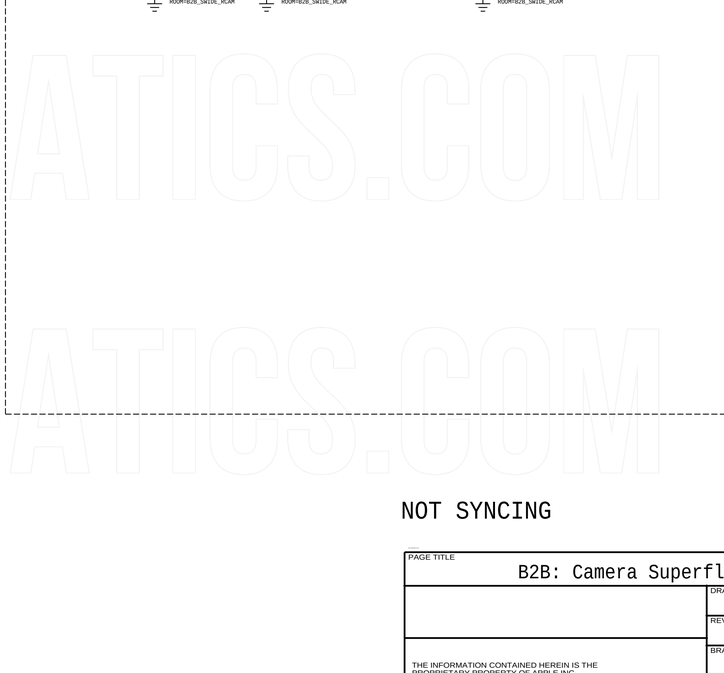


IO FILTERS

TELE



SWIDE



NOT SYNCING

PAGE TITLE	B2B: Camera Superflex
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	105 OF 138
SHEET	76 OF 117

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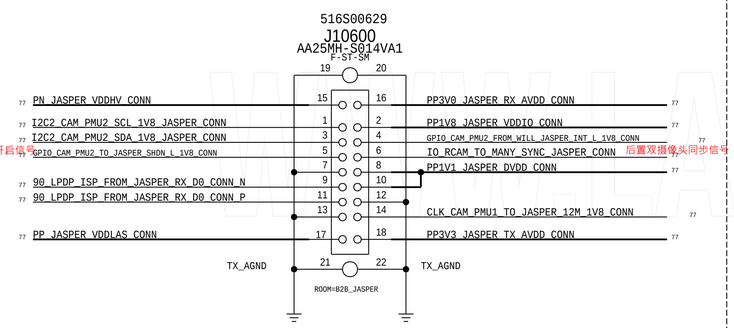
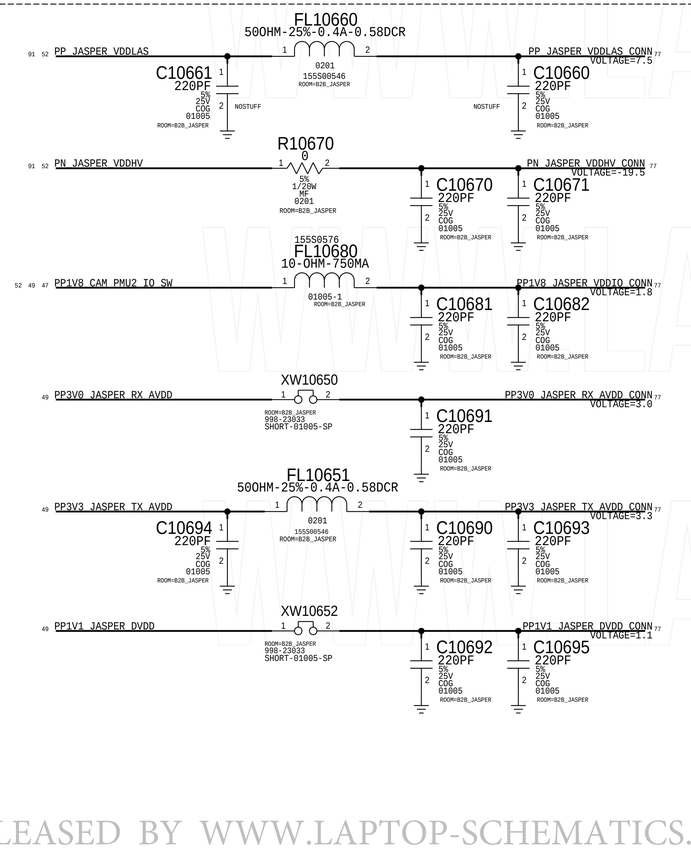
JASPER CAMERA B2B

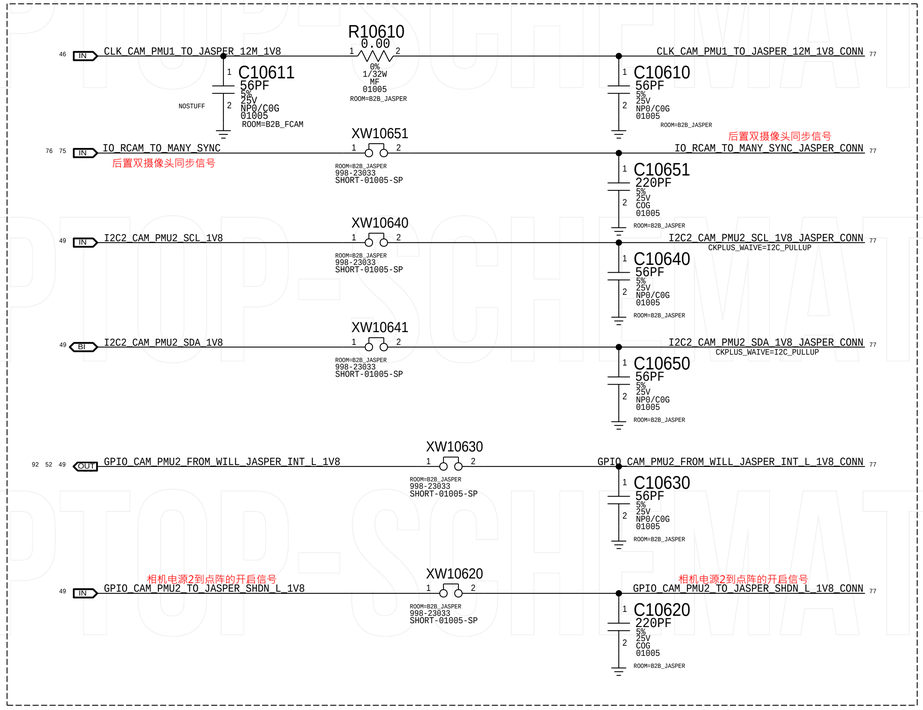
JASPER CONNECTOR



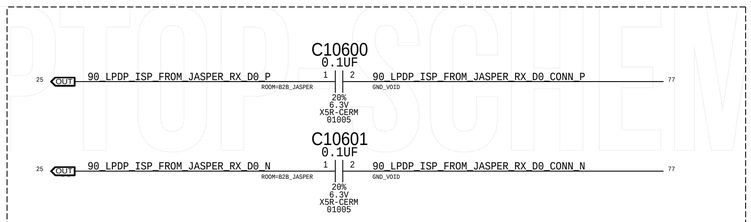
POWER FILTERS



IO FILTERS



LPDP FILTERS



NOT SYNCING

PAGE TITLE	B2B: Jasper
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	crb-1
PAGE	106 OF 138
SHEET	77 OF 117

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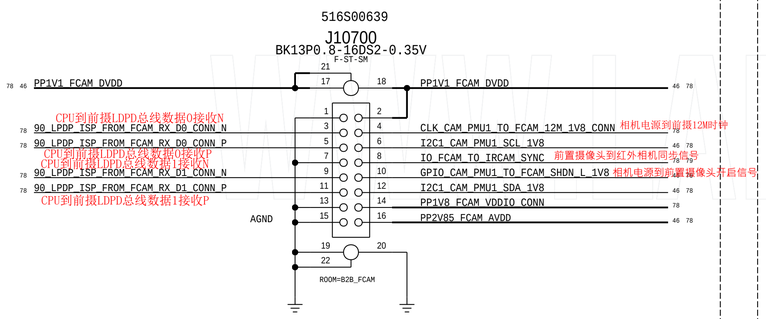
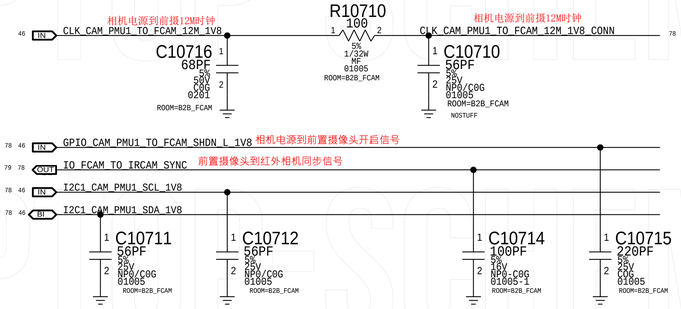
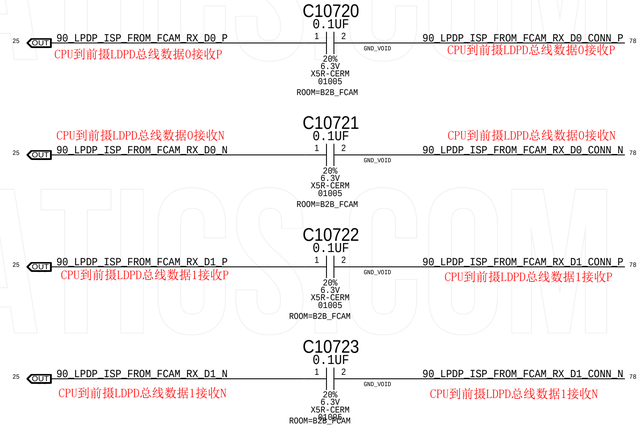


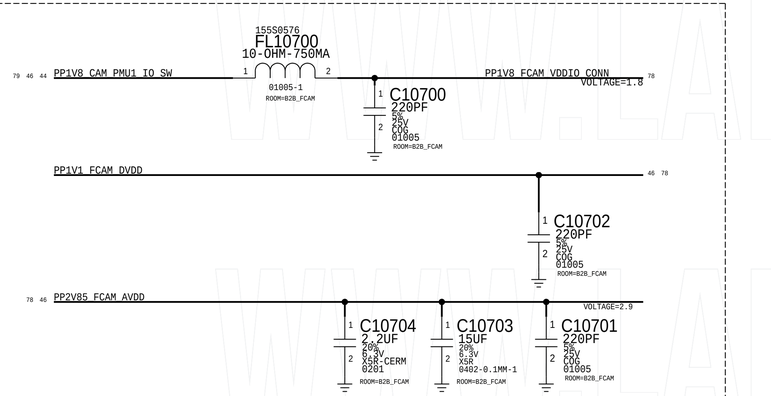
IO FILTERS



LPDP FILTERS



POWER FILTERS



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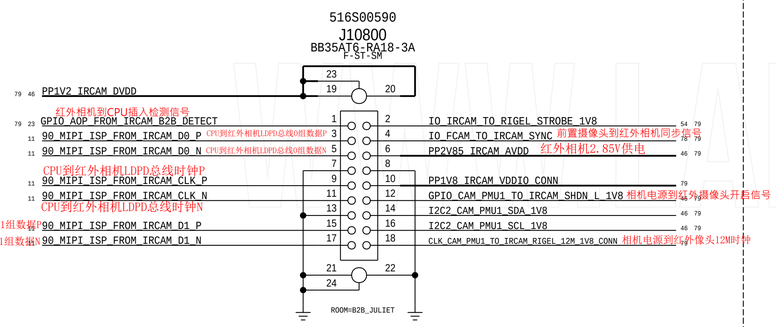
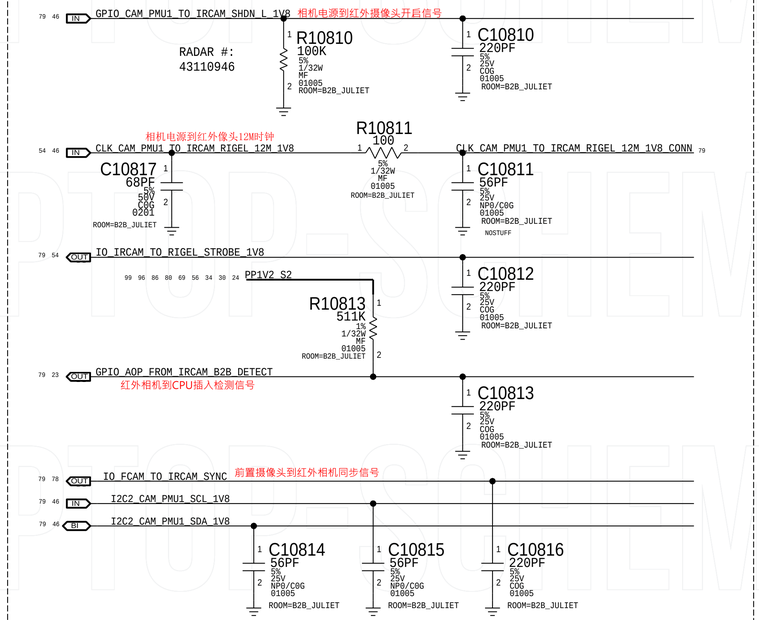
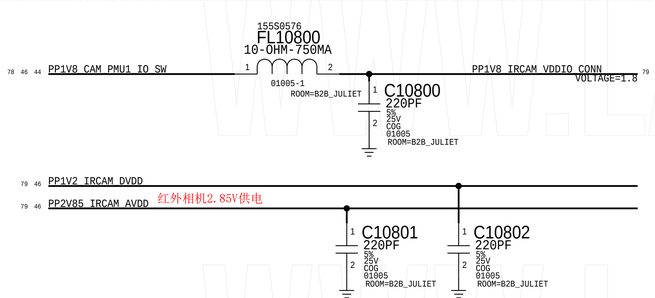
CONNECTOR



IO FILTERS



POWER FILTERS



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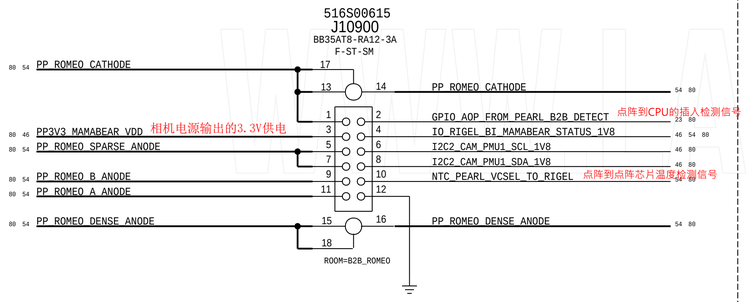
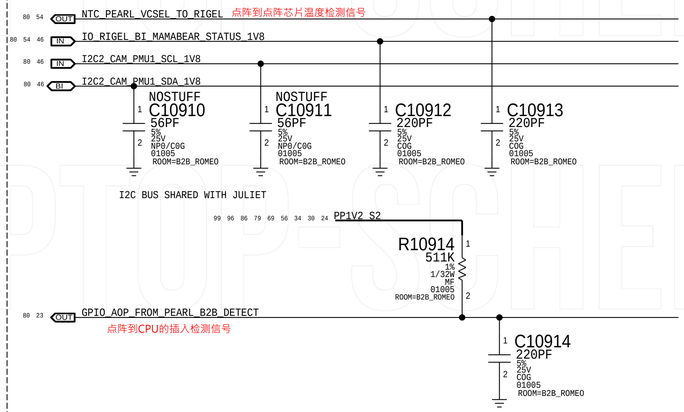
ROMEO B2B

CONNECTOR

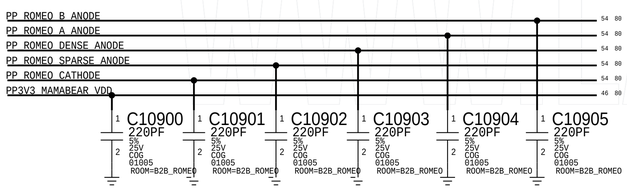


IO FILTERS



LPDP FILTERS

POWER FILTERS



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SYNC_MASTER=0.99.0 SYNC_DATE=04/03/2019

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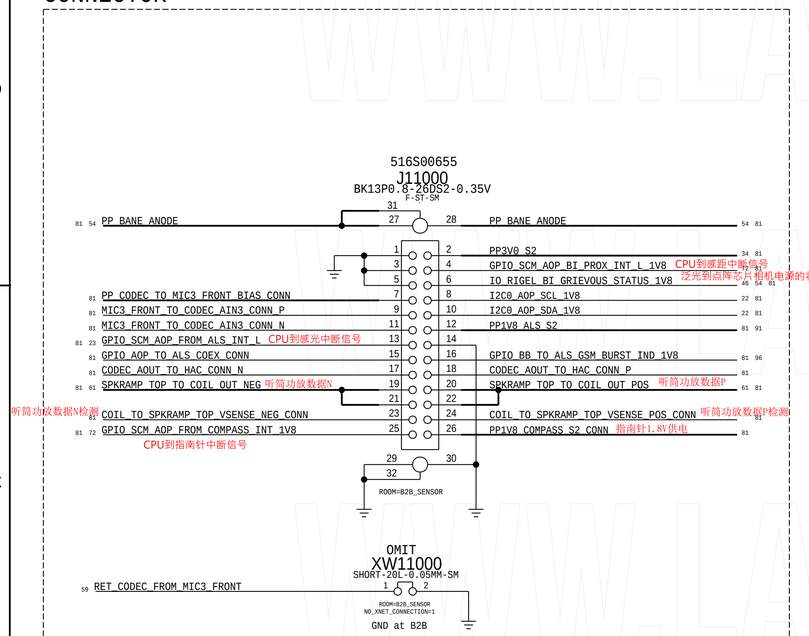
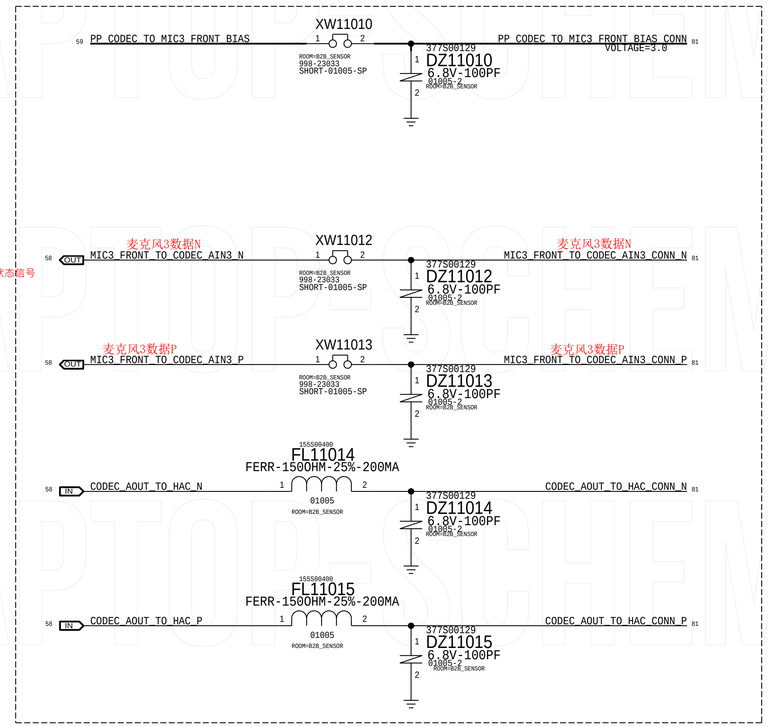
SENSOR B2B

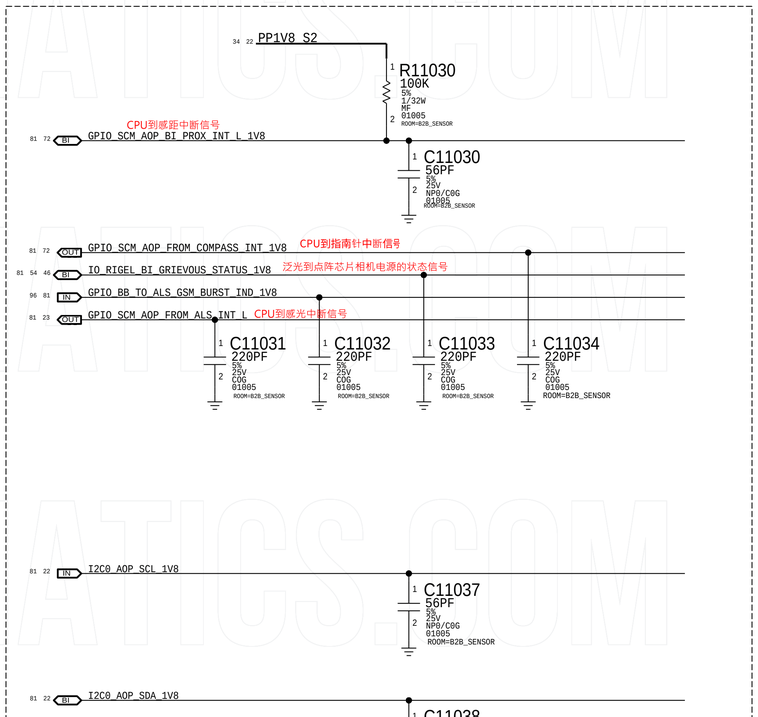
CONNECTOR



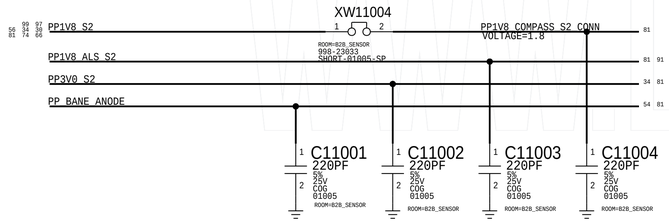
MIC3



IO FILTERS

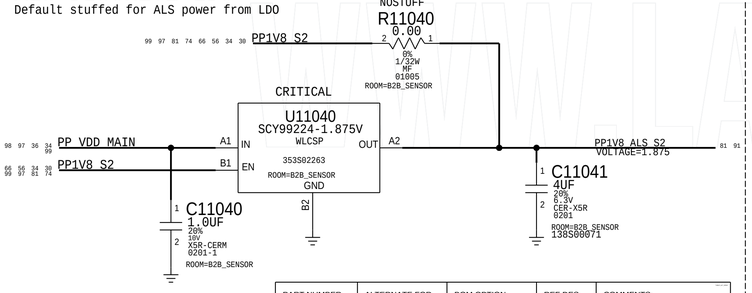


POWER FILTERS



ALS DISCRETE LDO

Default stuffed for ALS power from LDO



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00016	353S02263	?	U11040	IC,LDO,REG,1.875V,200MA

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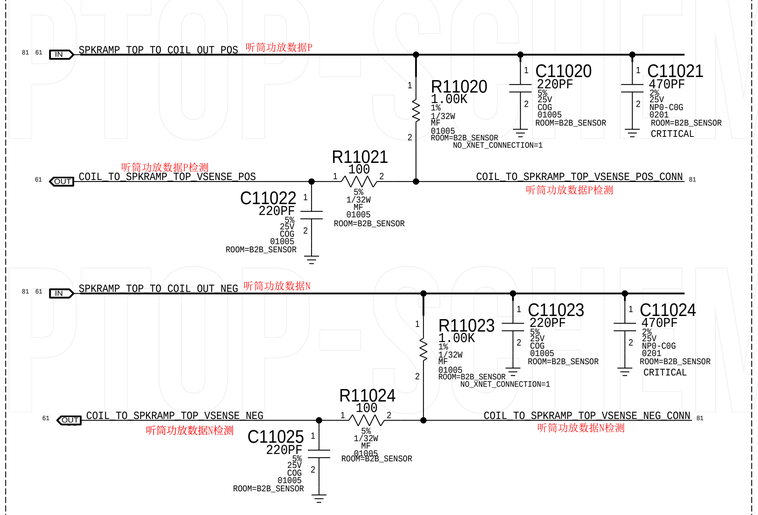
SPEAKER2



NOT SYNCING

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STROBE B2B

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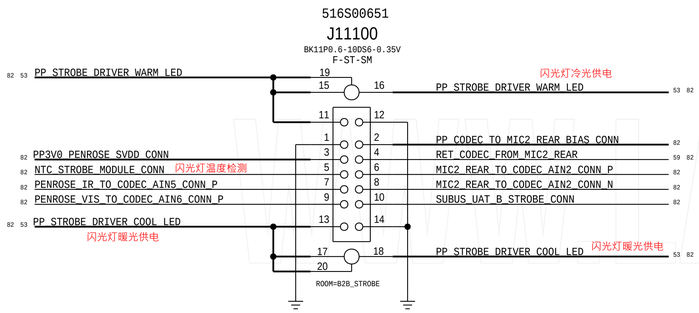
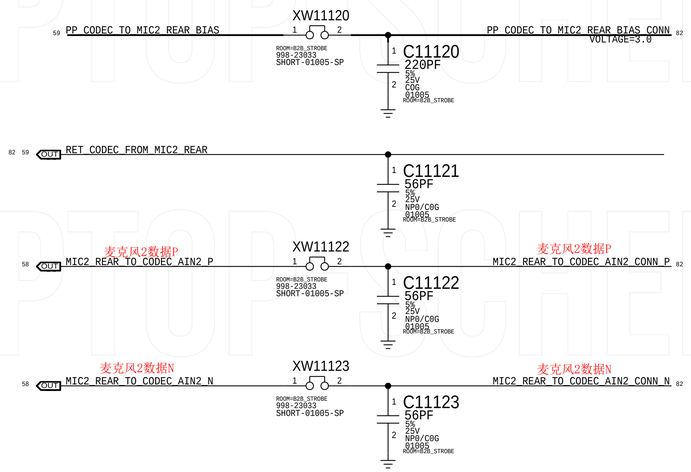
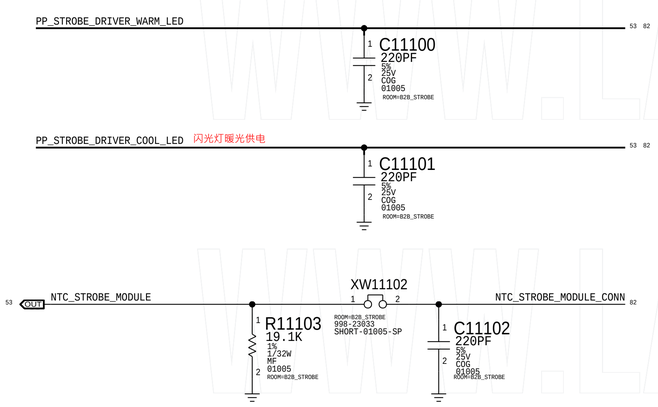


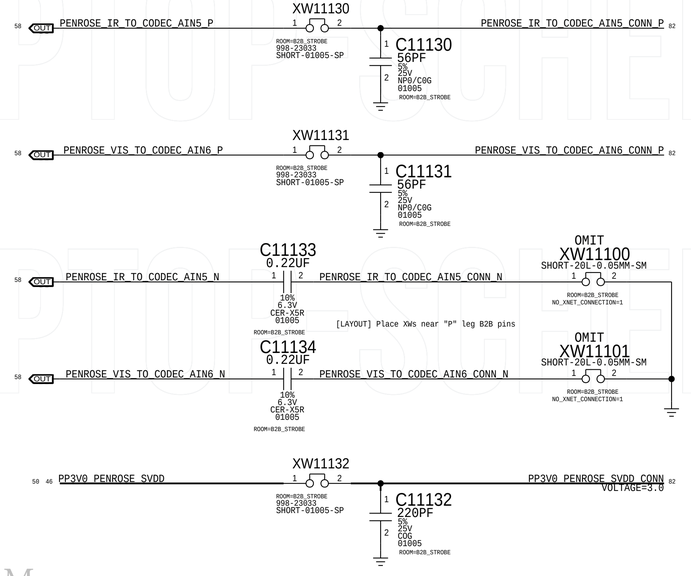
MIC2



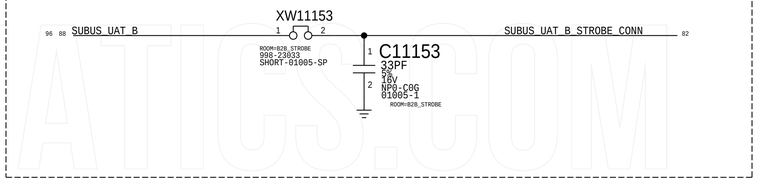
STROBE



PENROSE



SUBUS



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DOCK B2B

CONNECTOR

516S00649
J11200
AA26MK-S048VA1
F-ST-SM

97 83 35	PP_VBUS1_E75	尾插到充电芯片的充电电压	49	50	PP_VBUS1_E75 尾插到充电芯片的充电电压 35 83 97
83	MIC4_LOWER_TO_CODEC_AIN4_CONN_P		1	2	MIC4_LOWER_TO_CODEC_AIN4_CONN_N 83
83	PP_CODEC_TO_MIC4_LOWER_BIAS_CONN		3	4	RET_CODEC_FROM_MIC4_LOWER 59 83
83	COIL_TO_SPKRAMP_BOT_VSENSE_POS_CONN	底部喇叭数据P检测	5	6	SUBUS_LAT_B_CONN 84
83 60	SPKRAMP_BOT_TO_COIL_OUT_POS		7	8	COIL_TO_SPKRAMP_BOT_VSENSE_NEG_CONN 底部喇叭数据N检测 60 83
			9	10	SPKRAMP_BOT_TO_COIL_OUT_NEG 底部喇叭数据N 60 83
			11	12	
83 63	ARCAMP_TO_SOLENOID_OUT_POS	震动数据P	13	14	ARCAMP_TO_SOLENOID_OUT_NEG 震动数据N 63 83
			15	16	
83	SOLENOID_TO_ARCAMP_VSENSE_POS_CONN	震动数据P检测	17	18	SOLENOID_TO_ARCAMP_VSENSE_NEG_CONN 震动数据N检测 83
83	PP1V8_DOCK_S2_CONN		19	20	ANALOG_MIKEYBUS_REFERENCE 58 83
83 64	ANALOG_VIN_SAKONNET_FROM_HALL_N		21	22	ANALOG_VIN_SAKONNET_FROM_HALL_P 64 83
83 64	ANALOG_BIAS_SAKONNET_TO_HALL		23	24	ANALOG_RET_SAKONNET_TO_HALL 64 83
			25	26	
83	IO_E75_TO_KRAKEN_CON_DETECT_L_CONN	尾插到USB数据线插入检测	27	28	90_KRAKEN_DP2_CONN_P 尾插到USB数据2 P 67 91
			29	30	90_KRAKEN_DP2_CONN_N 尾插到USB数据2 N 67 91
83	MIC1_LOWER_TO_CODEC_AIN1_CONN_P		31	32	90_KRAKEN_DP1_CONN_N 尾插到USB数据1 N 67 91
83 59	RET_CODEC_FROM_MIC1_LOWER		33	34	90_KRAKEN_DP1_CONN_P 尾插到USB数据1 P 67 91
83	PP_KRAKEN_ACC2_CONN		35	36	
	附件供电2		37	38	MIC1_LOWER_TO_CODEC_AIN1_CONN_N 83
83	I2C1_AOP_SCL		39	40	PP_CODEC_TO_MIC1_LOWER_BIAS_CONN 83
83	PPVAR_EIGER_S2_CONN		41	42	PP_KRAKEN_ACC1_CONN 附件供电1 83
84	SUBUS_LAT_C_CONN		43	44	I2C1_AOP_SDA 83
84	SUBUS_LAT_A_CONN		45	46	GPIO_SCM_AOP_FROM_EIGER_INT_L 23 83
			47	48	
			51	52	

ROOM=B2B_DOCK

POWER FILTERS

PP_VBUS1_E75 尾插到充电芯片的充电电压 35 83 97

C11290 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C11291 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C11292 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C11293 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11294 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11295 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C11296 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C11297 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK

XW11211 SHORT-0201 ROOM=B2B_DOCK
PP_KRAKEN_ACC1 91 67 → PP_KRAKEN_ACC1_CONN 83 VOLTAGE=5.0
C11211 100PF 5% 16V NP0-C0G 01005-1 ROOM=B2B_DOCK

XW11213 SHORT-0201 ROOM=B2B_DOCK
PP_KRAKEN_ACC2 91 67 → PP_KRAKEN_ACC2_CONN 83 VOLTAGE=5.0
C11213 100PF 5% 16V NP0-C0G 01005-1 ROOM=B2B_DOCK

155S00400
FL11200
FERR-150OHM-25%-200MA
01005 ROOM=B2B_DOCK
PP1V8_S2 34 → PP1V8_DOCK_S2_CONN 83 VOLTAGE=1.8
C11200 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

155S00148
FL11230
33OHM-25%-0.4A-0.20DCR
01005 ROOM=B2B_DOCK
PPVAR_EIGER_S2 39 → PPVAR_EIGER_S2_CONN 83 VOLTAGE=3.0
C11230 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

MIC1 + MIC4

XW11203 998-23033 SHORT-01005-SP ROOM=B2B_DOCK
PP_CODEC_TO_MIC1_LOWER_BIAS 59 → PP_CODEC_TO_MIC1_LOWER_BIAS_CONN 83 VOLTAGE=3.0
C11254 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

RET_CODEC_FROM_MIC1_LOWER 83 59 OUT
C11253 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

XW11250 998-23033 SHORT-01005-SP ROOM=B2B_DOCK
MIC1_LOWER_TO_CODEC_AIN1_P 58 OUT → MIC1_LOWER_TO_CODEC_AIN1_CONN_P 83
C11250 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

麦克风1数据N
XW11252 998-23033 SHORT-01005-SP ROOM=B2B_DOCK
MIC1_LOWER_TO_CODEC_AIN1_N 58 OUT → 麦克风1数据N MIC1_LOWER_TO_CODEC_AIN1_CONN_N 83
C11252 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

XW11202 998-23033 SHORT-01005-SP ROOM=B2B_DOCK
PP_CODEC_TO_MIC4_LOWER_BIAS 59 → PP_CODEC_TO_MIC4_LOWER_BIAS_CONN 83 VOLTAGE=3.0
C11264 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK

RET_CODEC_FROM_MIC4_LOWER 83 59 OUT
C11263 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

麦克风4数据P
XW11260 998-23033 SHORT-01005-SP ROOM=B2B_DOCK
MIC4_LOWER_TO_CODEC_AIN4_P 58 OUT → 麦克风4数据P MIC4_LOWER_TO_CODEC_AIN4_CONN_P 83
C11260 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

麦克风4数据N
XW11262 998-23033 SHORT-01005-SP ROOM=B2B_DOCK
MIC4_LOWER_TO_CODEC_AIN4_N 58 OUT → 麦克风4数据N MIC4_LOWER_TO_CODEC_AIN4_CONN_N 83
C11262 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

SAKONNET

ANALOG_VIN_SAKONNET_FROM_HALL_P 83 64 OUT
C11240 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

ANALOG_VIN_SAKONNET_FROM_HALL_N 83 64 OUT
C11241 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

ANALOG_BIAS_SAKONNET_TO_HALL 83 64
C11242 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

ANALOG_RET_SAKONNET_TO_HALL 83 64
C11243 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

ARC + BOT SPEAKER

震动数据P
ARCAMP_TO_SOLENOID_OUT_POS 83 63
R11276 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C11271 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11272 470PF 2% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
震动数据P检测
SOLENOID_TO_ARCAMP_VSENSE_POS 63
R11290 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
C11275 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
SOLENOID_TO_ARCAMP_VSENSE_POS_CONN 83 震动数据P检测

震动数据N
ARCAMP_TO_SOLENOID_OUT_NEG 83 63
R11275 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C11270 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11273 470PF 2% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
震动数据N检测
SOLENOID_TO_ARCAMP_VSENSE_NEG 63
R11291 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
C11274 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
SOLENOID_TO_ARCAMP_VSENSE_NEG_CONN 83 震动数据N检测

SPKRAMP_BOT_TO_COIL_OUT_POS 83 60
R11283 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C11283 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11286 470PF 2% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
底部喇叭数据P检测
COIL_TO_SPKRAMP_BOT_VSENSE_POS 60 OUT
R11282 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
C11282 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
COIL_TO_SPKRAMP_BOT_VSENSE_POS_CONN 83 底部喇叭数据P检测

SPKRAMP_BOT_TO_COIL_OUT_NEG 83 60 底部喇叭数据
R11281 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C11285 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11287 470PF 2% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
底部喇叭数据N检测
COIL_TO_SPKRAMP_BOT_VSENSE_NEG 60 OUT
R11280 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
C11280 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
COIL_TO_SPKRAMP_BOT_VSENSE_NEG_CONN 83 底部喇叭数据N检测

IO FILTERS

R11210 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
IO_E75_TO_KRAKEN_CON_DETECT_L 91 67 OUT 尾插到USB数据线插入检测
C11210 27PF 5% 16V NP0-C0G 01005-1 ROOM=B2B_DOCK
IO_E75_TO_KRAKEN_CON_DETECT_L_CONN 83 尾插到USB数据线插入检测

ANALOG_MIKEYBUS_REFERENCE 83 58 OUT

GPIO_SCM_AOP_FROM_EIGER_INT_L 83 23 OUT

I2C1_AOP_SCL 22 IN
I2C1_AOP_SCL 22 IN
I2C1_AOP_SCL 83

I2C1_AOP_SDA 22 BI
I2C1_AOP_SDA 22 BI
I2C1_AOP_SDA 83

C11206 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
C11207 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
C11208 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C11212 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

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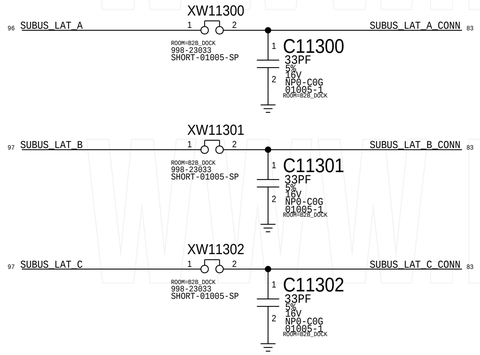
DOCK B2B FILTERS (CONT)

DOCK SUBUS FILTERS



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PAGE TITLE
B2B: Dock (Cont)

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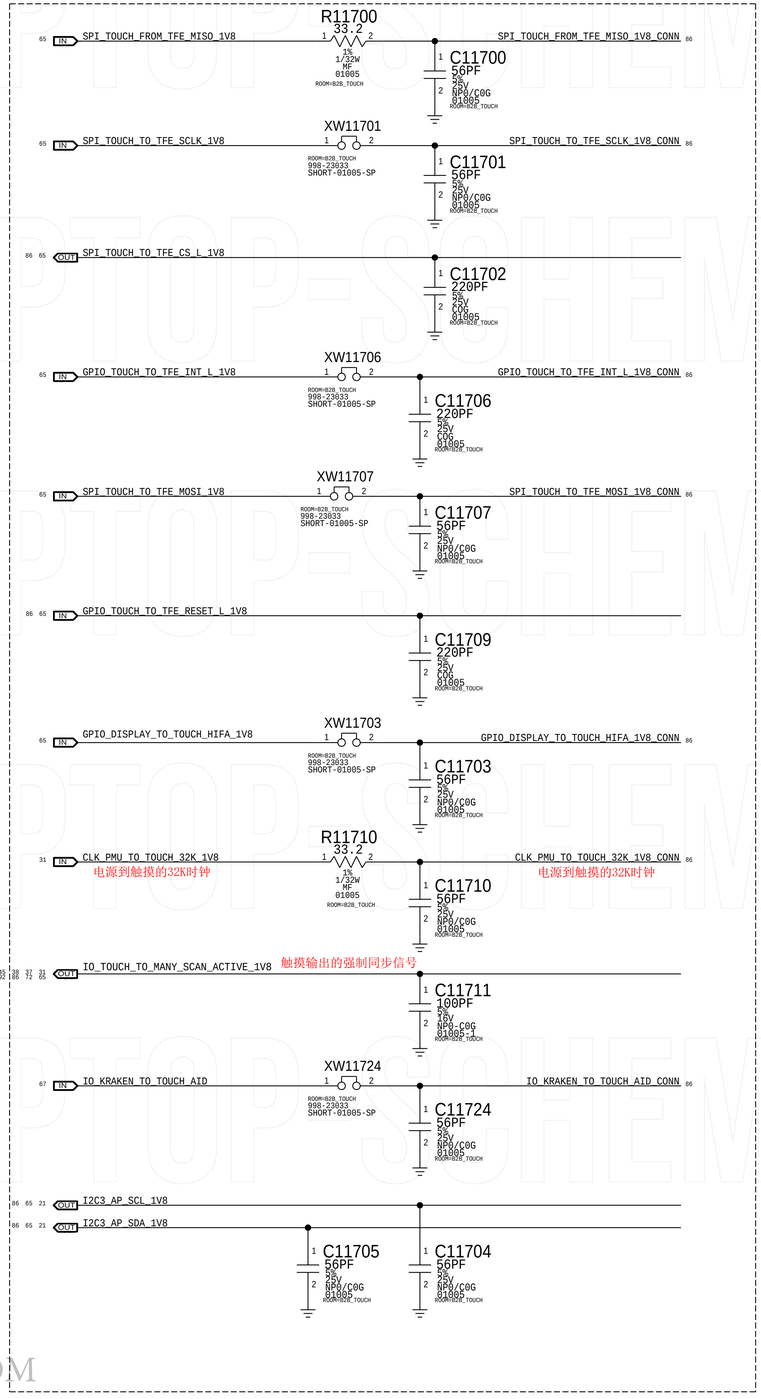
TOUCH B2B

CONNECTOR

DISPLAY/TOUCH COMBO B2B
MAINTAINED ON NEXT PAGE

POWER FILTERS

IO FILTERS



NOT SYNCING

SYNC_MASTER=0.99.0	SYNC_DATE=04/03/2019
PAGE TITLE	B2B: Display/Touch Combo (1/2)
DRAWING NUMBER	051-05170
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BRANCH	crb-1
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DISPLAY B2B

CONNECTOR

516S00593
J11800
2089750521
F-ST-SM

86	PP4V6_DISPLAY_VDDEL_CONN	显示屏4.6V供电	57 / 53	54
			1	2 PNVAR_DISPLAY_VSSEL_CONN 显示屏-7V供电 86
85	GPIO_DISPLAY_TO_TOUCH_HIFA_1V8_CONN		3	4
86 12	IO_AOP_TO_DISPLAY_MIPI_PWR_DWN	CPU到显示屏的开启信号	5	6
86 66 21	I2C_DISPLAY_SDA_1V8		7	8 GPIO_AP_FROM_DISPLAY_PANEL_ID_CONN CPU到显示屏ID识别信号 86
86 66 21	I2C_DISPLAY_SCL_1V8		9	10 SPI_MIPI_WPB/VPP: GND on MLB
86 66	IO_DPMIC_TO_DISPLAY_PANICB_L_1V8		11	12 PP1V8_DISPLAY_DVDD_CONN 86
86	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8_CONN	电源到显示屏复位信号	13	14 PP3V0_DISPLAY_S2_CONN 显示屏3V供电 86
86	PP7V3_DISPLAY_AVDDH_CONN		15	16 PP1V2_DISPLAY_S2_CONN 86
86	GPIO_DISPLAY_TO_TOUCH_BSYNC1_1V8_CONN		17	18 PP1VX_DISPLAY_S2_CONN 显示屏1V供电 86
86	IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8_CONN	显示屏到显示电源7.3V开启信号	19	20 IO_DISPLAY_TO_DPMIC_VOUT12_EN_1V8_CONN 显示屏到显示电源4.6V和负电压开启信号 86
86	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8_CONN	电源到显示屏32K时钟信号	21	22 IO_AOP_FROM_DISPLAY_TE CPU到显示屏的显示数据同步信号 86
			23	24
86	90_MIPI_AP_TO_DISPLAY_D3_CONN_N	CPU到显示屏3组数据N	25	26 90_MIPI_AP_TO_DISPLAY_D0_CONN_N CPU到显示屏0组数据N 86
86	90_MIPI_AP_TO_DISPLAY_D3_CONN_P	CPU到显示屏3组数据P	27	28 90_MIPI_AP_TO_DISPLAY_D0_CONN_P CPU到显示屏0组数据P 86
			29	30
86	90_MIPI_AP_TO_DISPLAY_CLK_CONN_N	CPU到显示屏数据时钟N	31	32 90_MIPI_AP_TO_DISPLAY_D1_CONN_N CPU到显示屏1组数据N 86
86	90_MIPI_AP_TO_DISPLAY_CLK_CONN_P	CPU到显示屏数据时钟P	33	34 90_MIPI_AP_TO_DISPLAY_D1_CONN_P CPU到显示屏1组数据P 86
			35	36
86	90_MIPI_AP_TO_DISPLAY_D2_CONN_N	CPU到显示屏2组数据N	37	38 I2C3_AP_SCL_1V8 21 65 85
86	90_MIPI_AP_TO_DISPLAY_D2_CONN_P	CPU到显示屏2组数据P	39	40 I2C3_AP_SDA_1V8 21 65 85
			41	42 SPI_TOUCH_TO_TFE_CS_L_1V8 65 85
85	IO_KRAKEN_TO_TOUCH_AID_CONN		43	44 GPIO_TOUCH_TO_TFE_INT_L_1V8_CONN 85
85	SPI_TOUCH_FROM_TFE_MISO_1V8_CONN		45	46 GPIO_TOUCH_TO_TFE_RESET_L_1V8 65 85
85	SPI_TOUCH_TO_TFE_MOSI_1V8_CONN		47	48 CLK_PMU_TO_TOUCH_32K_1V8_CONN 电源到触摸的32K时钟 85
85	SPI_TOUCH_TO_TFE_SCLK_1V8_CONN		49	50 PP3V1_TOUCH_S2_CONN 触摸3.1V供电 85
45 85 38 72 37 65 92 48	IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8		51	52 PP1V8_TOUCH_S2_CONN 触摸1.2V供电 85
	触摸输出的强制同步信号		55 / 58	56

ROOM=B2B_DISPLAY

MIPI FILTERS

25	90_MIPI_AP_TO_DISPLAY_D0_N	XW11800	90_MIPI_AP_TO_DISPLAY_D0_CONN_N 86
	CPU到显示屏0组数据N		CPU到显示屏0组数据N
25	90_MIPI_AP_TO_DISPLAY_D0_P	XW11801	90_MIPI_AP_TO_DISPLAY_D0_CONN_P 86
	CPU到显示屏0组数据P		CPU到显示屏0组数据P
25	90_MIPI_AP_TO_DISPLAY_D1_N	XW11802	90_MIPI_AP_TO_DISPLAY_D1_CONN_N 86
	CPU到显示屏1组数据N		CPU到显示屏1组数据N
25	90_MIPI_AP_TO_DISPLAY_D1_P	XW11803	90_MIPI_AP_TO_DISPLAY_D1_CONN_P 86
	CPU到显示屏1组数据P		CPU到显示屏1组数据P
25	90_MIPI_AP_TO_DISPLAY_D2_P	XW11804	90_MIPI_AP_TO_DISPLAY_D2_CONN_P 86
	CPU到显示屏2组数据P		CPU到显示屏2组数据P
25	90_MIPI_AP_TO_DISPLAY_D2_N	XW11805	90_MIPI_AP_TO_DISPLAY_D2_CONN_N 86
	CPU到显示屏2组数据N		CPU到显示屏2组数据N
25	90_MIPI_AP_TO_DISPLAY_D3_P	XW11806	90_MIPI_AP_TO_DISPLAY_D3_CONN_P 86
	CPU到显示屏3组数据P		CPU到显示屏3组数据P
25	90_MIPI_AP_TO_DISPLAY_D3_N	XW11807	90_MIPI_AP_TO_DISPLAY_D3_CONN_N 86
	CPU到显示屏3组数据N		CPU到显示屏3组数据N
25	90_MIPI_AP_TO_DISPLAY_CLK_P	XW11808	90_MIPI_AP_TO_DISPLAY_CLK_CONN_P 86
	CPU到显示屏数据时钟P		CPU到显示屏数据时钟P
25	90_MIPI_AP_TO_DISPLAY_CLK_N	XW11809	90_MIPI_AP_TO_DISPLAY_CLK_CONN_N 86
	CPU到显示屏数据时钟N		CPU到显示屏数据时钟N

ROOM=D_PMIC 998-23033 SHORT-01005-SP

IO FILTERS

86 12	IO_AOP_TO_DISPLAY_MIPI_PWR_DWN	CPU到显示屏的开启信号	C11813 220PF 5% 25V C0G 01005
66 33	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8	电源到显示屏复位信号	XW11814 SHORT-0201 → GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8_CONN 电源到显示屏复位信号 86
			C11814 220PF 5% 25V C0G 01005
			C11818 1000PF 10% 50V X5R-CERM 01005
33	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8	电源到显示屏32K时钟信号	XW11817 0 → CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8_CONN 电源到显示屏32K时钟信号 86
			C11817 56PF 5% 25V NP0/C0G 01005
23	GPIO_AP_FROM_DISPLAY_PANEL_ID	CPU到显示屏ID识别信号	R11818 1.00K 1% 1/32W MF 01005 → GPIO_AP_FROM_DISPLAY_PANEL_ID_CONN CPU到显示屏ID识别信号 86
86 12	IO_AOP_FROM_DISPLAY_TE	CPU到显示屏的显示数据同步信号	C11819 56PF 5% 25V NP0/C0G 01005
65	GPIO_DISPLAY_TO_TOUCH_BSYNC1_1V8		XW11820 → GPIO_DISPLAY_TO_TOUCH_BSYNC1_1V8_CONN 86
			C11820 56PF 5% 25V NP0/C0G 01005
86 66	IO_DPMIC_TO_DISPLAY_PANICB_L_1V8		C11821 220PF 5% 25V C0G 01005
66	IO_DISPLAY_TO_DPMIC_VOUT12_EN_1V8	显示屏到显示电源4.6V和负电压开启信号	XW11822 → IO_DISPLAY_TO_DPMIC_VOUT12_EN_1V8_CONN 显示屏到显示电源4.6V和负电压开启信号 86
			C11822 220PF 5% 25V C0G 01005
66 31	IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8	显示屏到显示电源7.3V开启信号	XW11823 → IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8_CONN 显示屏到显示电源7.3V开启信号 86
			C11823 220PF 5% 25V C0G 01005
86 66 21	I2C_DISPLAY_SCL_1V8		C11815 56PF 5% 25V NP0/C0G 01005
86 66 21	I2C_DISPLAY_SDA_1V8		C11816 56PF 5% 25V NP0/C0G 01005

ROOM=B2B_DISPLAY 998-23033 SHORT-01005-SP

POWER FILTERS

91 66	PP7V3_DISPLAY_AVDDH	XW11850 SHORT-01005-SP	PP7V3_DISPLAY_AVDDH_CONN VOLTAGE=7.3 86
			C11850 220PF 5% 25V C0G 01005
91 66	PP4V6_DISPLAY_VDDEL 显示屏4.6V供电	XW11860 SHORT-0201	显示屏4.6V供电 PP4V6_DISPLAY_VDDEL_CONN VOLTAGE=4.6 86
			C11860 220PF 5% 25V C0G 01005
91 66	PNVAR_DISPLAY_VSSEL 显示屏-7V供电	R11870 0 5% 1/20W MF 0201	显示屏-7V供电 PNVAR_DISPLAY_VSSEL_CONN VOLTAGE=-7.0 86
			C11870 220PF 5% 25V C0G 01005
			C11871 1.0UF 20% 10V X5R-CERM 0201-1
55 34 80 70 69	PP1V2_S2	XW11880 SHORT-01005-SP	PP1V2_DISPLAY_S2_CONN VOLTAGE=1.2 86
			C11880 220PF 5% 25V C0G 01005
34	PP1V8_S2	155S0960 FL11881 FERR-700HM-25%-0.300A 01005	PP1V8_DISPLAY_DVDD_CONN VOLTAGE=1.8V 86
			C11881 220PF 5% 25V C0G 01005
28	PP1VX_DISPLAY_S2 显示屏1V供电	XW11882 SHORT-0201	显示屏1V供电 PP1VX_DISPLAY_S2_CONN 86
			C11882 220PF 5% 25V C0G 01005
30	PP3V0_DISPLAY_S2 显示屏3V供电	155S0960 FL11801 FERR-700HM-25%-0.300A 01005	显示屏3V供电 PP3V0_DISPLAY_S2_CONN 86
			C11883 220PF 5% 25V C0G 01005

ROOM=B2B_DISPLAY 998-23033 SHORT-01005-SP

NOT SYNCING

SYNC_MASTER=0.99.0	SYNC_DATE=04/03/2019
PAGE TITLE	B2B: Display/Touch Combo (2/2)
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REVISION	10.0.0
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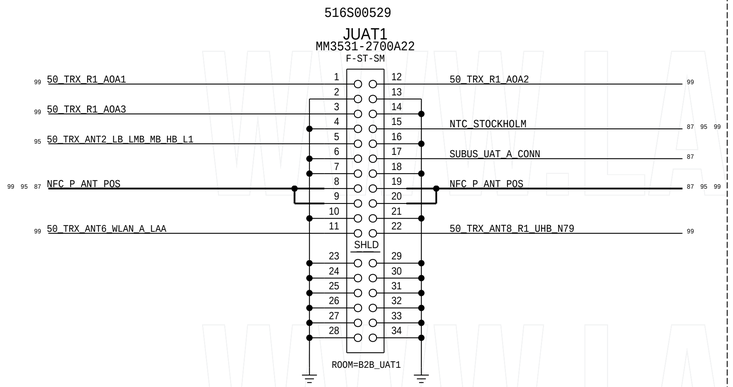
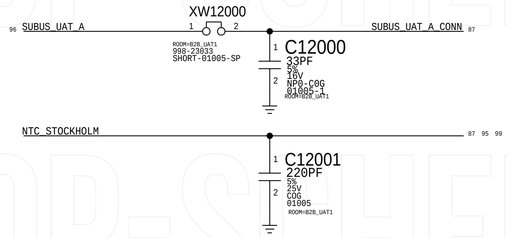
UAT1 B2B

CONNECTOR



SUBUS FILTERS



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SYNC_MASTER=D53_mlb_ice_0.19.0 SYNC_DATE=02/01/2019

PAGE TITLE: B2B: UAT1

DRAWING NUMBER: 051-05170 SIZE: D

REVISION: 10.0.0

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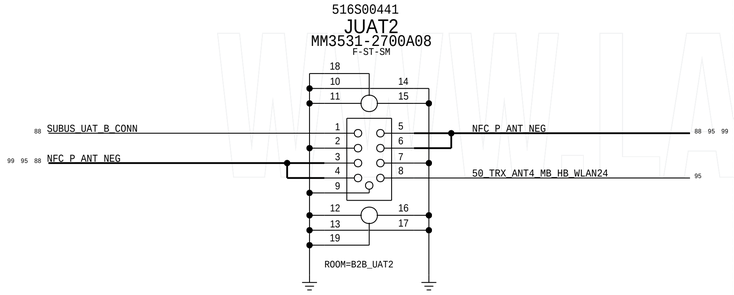
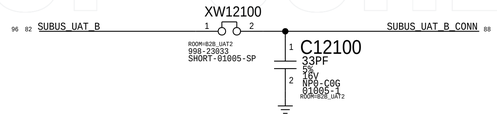
UAT2 B2B

CONNECTOR



SUBUS FILTERS



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B2B: UAT2

DRAWING NUMBER 051-05170
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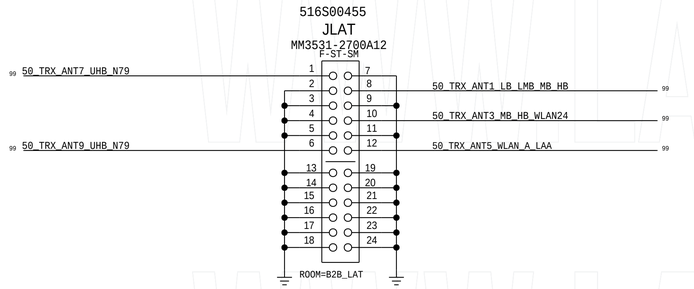
LAT B2B

CONNECTOR



SUBUS FILTERS

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PAGE TITLE: B2B: LAT

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
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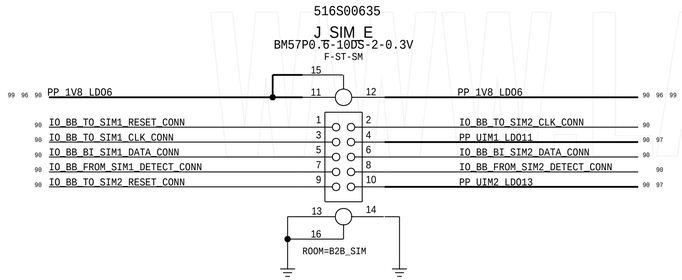
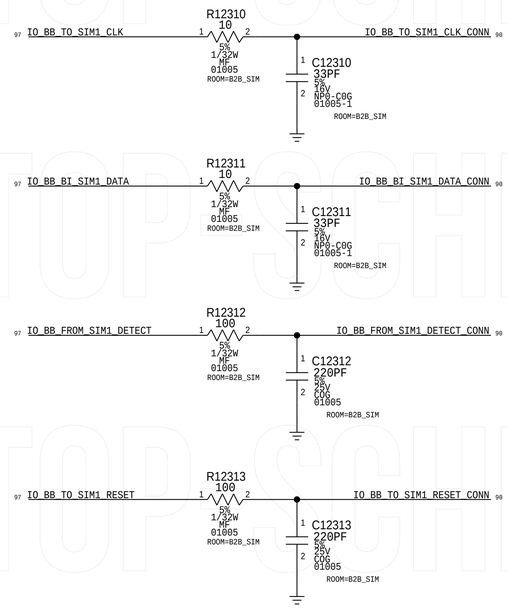
SIM B2B

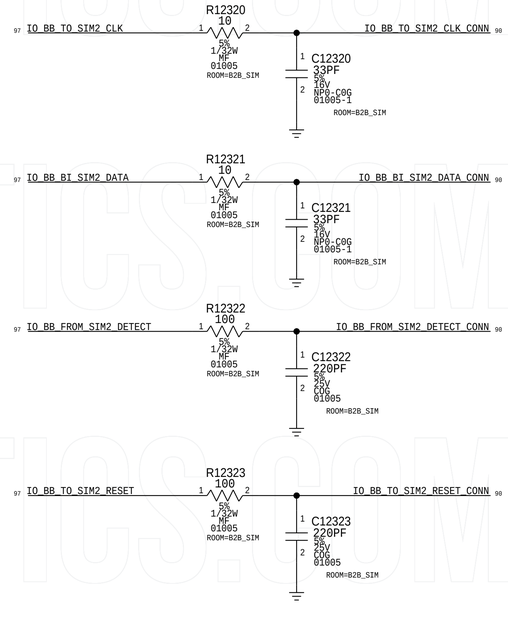
CONNECTOR



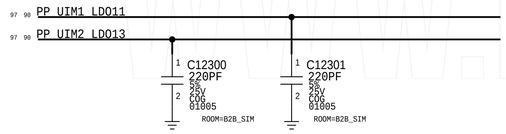
SIM1 IO FILTERS



SIM2 IO FILTERS



SIM POWER + DETECT



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PAGE TITLE: B2B: SIM

DRAWING NUMBER: 051-05170 | SIZE: D
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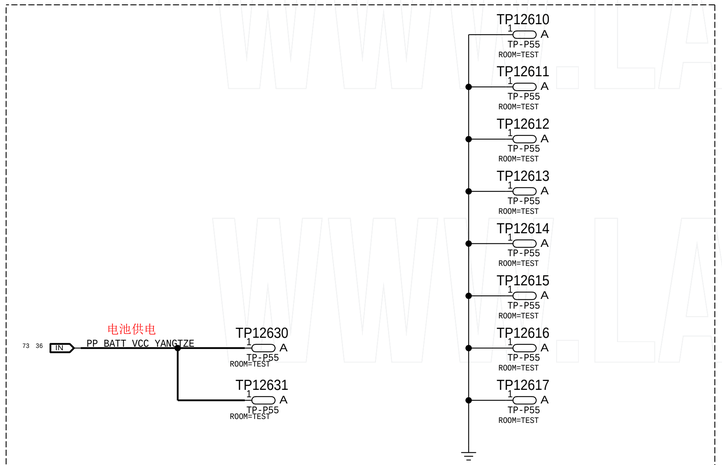
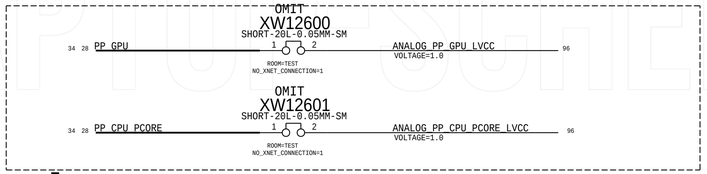
Test Points

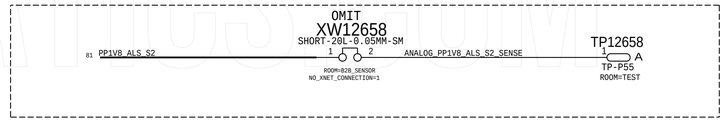
Power + GND



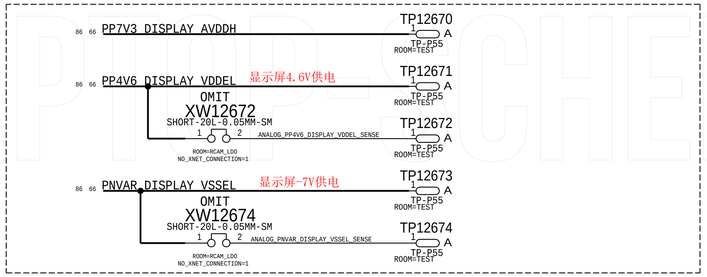
LVCC



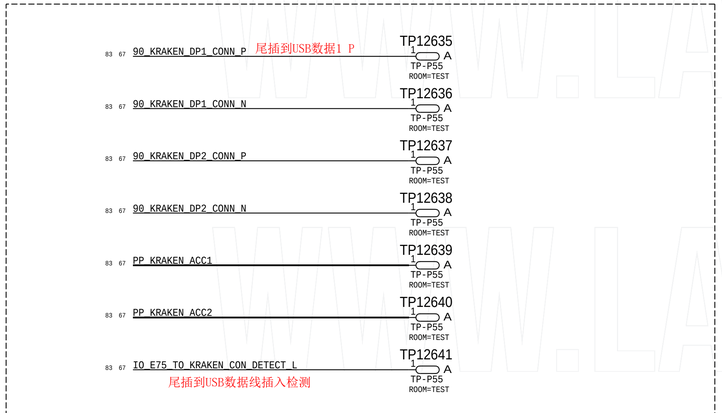
ALS Discrete LDO



Galena

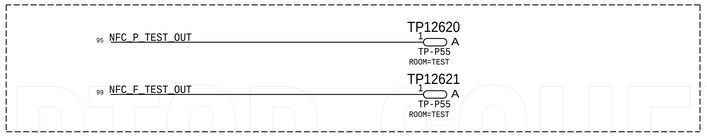


E75

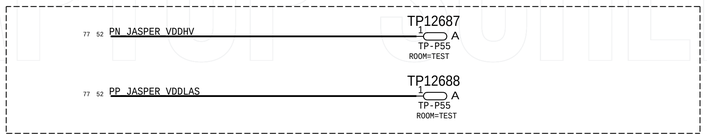


OV COMP

NFC

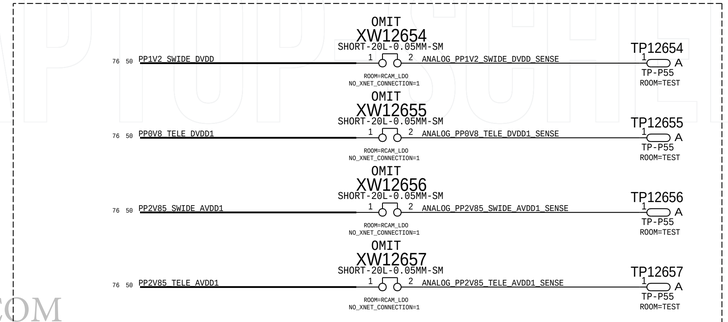


Will



Dotara Power

Discrete Camera LDO



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Probe Points

CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	电源到WIFI 超带宽芯片的时钟	PP12800	P2MM-NSM SM ROOM=TEST	
GPIO_SCM_AOP_FROM_JARVIS_INT		PP12801	P2MM-NSM SM ROOM=TEST	
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK	CPU逻辑模块到音频的I2S1总线串行时钟	PP12869	P2MM-NSM SM ROOM=TEST	
GPIO_AOP_TO_CODEC_RESET_L	CPU到音频芯片复位信号	PP12803	P2MM-NSM SM ROOM=TEST	
GPIO_AP_BI_CCG2B_SWDIO	CPU到快充芯片SWD总线数据	PP12804	P2MM-NSM SM ROOM=TEST	
GPIO_AP_FROM_CODEC_INT_L	CPU到音频的中断信号	PP12805	P2MM-NSM SM ROOM=TEST	
GPIO_BOARD_ID0	PLACE_SIDE=TOP	PP12806	P2MM-NSM SM ROOM=TEST	
GPIO_AP_TO_AMUX_PMU_SYNC	CPU到电源数模转换同步信号	PP12807	P2MM-NSM SM ROOM=TEST	
GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	点阵到相机电源和电源的中断信号	PP12808	P2MM-NSM SM ROOM=TEST	
GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	相机电源到点阵芯片开启信号	PP12809	P2MM-NSM SM ROOM=TEST	
GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	相机电源到闪光灯芯片开启	PP12810	P2MM-NSM SM ROOM=TEST	
GPIO_NUB_FROM_CCG2B_INT_L	快充芯片到CPU的中断信号	PP12811	P2MM-NSM SM ROOM=TEST	
GPIO_NUB_FROM_GECKO_IRQ_L	附件供电芯片到CPU的中断请求信号	PP12812	P2MM-NSM SM ROOM=TEST	
GPIO_NUB_FROM_PARROT_INT_L	USB数据转换芯片到CPU的中断信号	PP12813	P2MM-NSM SM ROOM=TEST	
GPIO_NUB_TO_GECKO_RESET_L	CPU到附件供电芯片复位信号	PP12814	P2MM-NSM SM ROOM=TEST	
GPIO_PMU_FROM_CODEC_WAKE_L	电源到音频的唤醒信号	PP12815	P2MM-NSM SM ROOM=TEST	
GPIO_PMU_TO_AMUX_PMU_SUPER_TP		PP12816	P2MM-NSM SM ROOM=TEST	
GPIO_PMU_TO_CCG2B_RESET_L	电源到快充芯片的复位信号	PP12817	P2MM-NSM SM ROOM=TEST	
GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	电源到硬盘低电量启动信号	PP12818	P2MM-NSM SM ROOM=TEST	
GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L	电源到CPU的检测信号	PP12819	P2MM-NSM SM ROOM=TEST	
GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	电源到喇叭功放的复位	PP12820	P2MM-NSM SM ROOM=TEST	
GPIO_SEQ_PMU_TO_BOOST_EN_1V8	电源到BOOST升压芯片开启信号	PP12821	P2MM-NSM SM ROOM=TEST	
GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	电源到显示屏异常识别信号	PP12822	P2MM-NSM SM ROOM=TEST	
I2S0_AOP_FROM_CODEC_ASP1_BCLK	CPU逻辑模块到音频的I2S0总线串行时钟	PP12823	P2MM-NSM SM ROOM=TEST	
I2S0_AOP_FROM_CODEC_ASP1_DIN	音频到CPU逻辑模块的I2S0总线数据	PP12824	P2MM-NSM SM ROOM=TEST	
I2S0_AOP_FROM_CODEC_ASP1_LRCLK	CPU逻辑模块到音频的I2S0总线帧时钟	PP12825	P2MM-NSM SM ROOM=TEST	
I2S0_AOP_TO_CODEC_ASP1_DOUT	CPU逻辑模块到音频的I2S0总线数据	PP12826	P2MM-NSM SM ROOM=TEST	
GPIO_PMU_FROM_TOUCH_LDO_EN		PP12827	P2MM-NSM SM ROOM=TEST	
IO_KRAKEN_TO_CHARGER_VBUS1_VALID_L_1V8	USB到充电芯片充电开启信号	PP12828	P2MM-NSM SM ROOM=TEST	
IO_KRAKEN_TO_PARROT_PMU_USB_EN	USB输出的开启信号	PP12829	P2MM-NSM SM ROOM=TEST	
IO_NUB_FROM_KRAKEN_DOCK_CONNECT	USB到CPU的供电插入检测信号	PP12830	P2MM-NSM SM ROOM=TEST	
IO_PMU_FROM_KRAKEN_RESET	USB到电源的复位	PP12831	P2MM-NSM SM ROOM=TEST	
IO_SPKRAMP_TO_SPKRAMP_SYNC	听筒功放到喇叭功放的同步信号	PP12832	P2MM-NSM SM ROOM=TEST	
PP_VAR_USB_RVP	充电芯片到USB的过压检测信号	PP12833	P2MM-NSM SM ROOM=TEST	
SPI3_AP_FROM_CODEC_MISO	大音频到CPU的SPI总线数据	PP12834	P2MM-NSM SM ROOM=TEST	
SPI3_AP_TO_CODEC_CS_L	CPU到大音频的SPI总线片选信号	PP12835	P2MM-NSM SM ROOM=TEST	
SPI3_AP_TO_CODEC_MOSI	CPU到大音频的SPI总线数据	PP12836	P2MM-NSM SM ROOM=TEST	
SWD_NUB_TO_PMU_TOUCH_SWCLK	CPU到电源和触摸电源的SPMI总线时钟	PP12837	P2MM-NSM SM ROOM=TEST	
UART2_AOP_TO_TOUCH_TXD	CPU到触摸的UART总线发射	PP12838	P2MM-NSM SM ROOM=TEST	
UART4_AP_FROM_KRAKEN_ACC_RXD	CPU到USB芯片UART总线数据接收	PP12839	P2MM-NSM SM ROOM=TEST	
UART4_AP_TO_KRAKEN_ACC_TXD	CPU到USB芯片UART总线数据发射	PP12840	P2MM-NSM SM ROOM=TEST	
UART2_AOP_FROM_TOUCH_RXD	CPU到触摸的UART总线接收	PP12863	P2MM-NSM SM ROOM=TEST	

Buck3 Load Testing

PP1V8_S4	PLACE_SIDE=TOP	PP12894	P2MM-NSM SM ROOM=TEST

90_EUSB_DBG_PARROT_BI_AP_N	CPU到USB数据转换芯片测试数据N	PP12841	P2MM-NSM SM ROOM=TEST
90_EUSB_DBG_PARROT_BI_AP_P	CPU到USB数据转换芯片测试数据P	PP12842	P2MM-NSM SM ROOM=TEST
90_EUSB_PARROT_BI_AP_N	CPU输出的USB信号N	PP12843	P2MM-NSM SM ROOM=TEST
90_EUSB_PARROT_BI_AP_P	CPU输出的USB信号P	PP12844	P2MM-NSM SM ROOM=TEST
90_USB1_KRAKEN_BI_PARROT_N		PP12845	P2MM-NSM SM ROOM=TEST
90_USB1_KRAKEN_BI_PARROT_P		PP12846	P2MM-NSM SM ROOM=TEST
IO_AP_FROM_PMU_SW_SHDN_L	CPU到主电源节能开启信号	PP12847	P2MM-NSM SM ROOM=TEST
I2S0_AP_FROM_CODEC_ASP3_BCLK	音频到CPU的I2S0总线串行时钟	PP12848	P2MM-NSM SM ROOM=TEST
I2S0_AP_FROM_CODEC_ASP3_DIN	音频到CPU的I2S0总线数据	PP12849	P2MM-NSM SM ROOM=TEST
I2S0_AP_FROM_CODEC_ASP3_LRCLK	音频到CPU的I2S0总线帧时钟	PP12850	P2MM-NSM SM ROOM=TEST
I2S0_AP_TO_CODEC_ASP3_DOUT	CPU到音频的I2S0总线数据	PP12851	P2MM-NSM SM ROOM=TEST
I2S1_AP_FROM_CODEC_ASP4_BCLK	音频到CPU的I2S1总线串行时钟	PP12852	P2MM-NSM SM ROOM=TEST
I2S1_AP_FROM_CODEC_ASP4_DIN	音频到CPU的I2S1总线数据	PP12853	P2MM-NSM SM ROOM=TEST
I2S1_AP_FROM_CODEC_ASP4_LRCLK	音频到CPU的I2S1总线帧时钟	PP12854	P2MM-NSM SM ROOM=TEST
I2S1_AP_TO_CODEC_ASP4_DOUT	CPU到音频的I2S1总线数据	PP12855	P2MM-NSM SM ROOM=TEST
IO_AP_TO_NAND_FW_STRAP	CPU到硬盘的启动信号	PP12856	P2MM-NSM SM ROOM=TEST
IO_NUB_FROM_KRAKEN_INT	USB到CPU的中断信号	PP12857	P2MM-NSM SM ROOM=TEST
GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	充电芯片到主电源的中断信号	PP12858	P2MM-NSM SM ROOM=TEST
PDM_OUT1_CODEC_TO_SPKRAMP_TOP_CLK		PP12859	P2MM-NSM SM ROOM=TEST
PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA		PP12860	P2MM-NSM SM ROOM=TEST
UART0_AP_FROM_KRAKEN_DEBUG_RXD	CPU到USB芯片UART总线调试数据接收	PP12861	P2MM-NSM SM ROOM=TEST
UART0_AP_TO_KRAKEN_DEBUG_TXD	CPU到USB芯片UART总线调试数据发射	PP12862	P2MM-NSM SM ROOM=TEST
SWD_DOCK_TO_AP_SWCLK	USB到CPU的SWD总线时钟	PP12864	P2MM-NSM SM ROOM=TEST
SWD_DOCK_BI_AP_SWDIO	USB到CPU的SWD总线数据	PP12865	P2MM-NSM SM ROOM=TEST

NAND

SWD_AP_BI_NAND_SWDIO	CPU到硬盘的SWD总线数据	PP12866	P2MM-NSM SM ROOM=TEST
SPI0_AP_FROM_SSE_MISO_BOOT_CONFIG2	硬盘输出到CPU的SPI总线数据	PP12867	P2MM-NSM SM ROOM=TEST
IO_AP_TO_NAND_RESET_L	CPU到硬盘复位	PP12868	P2MM-NSM SM ROOM=TEST
ANALOG_NAND_ANI1_VREF		PP12870	P2MM-NSM SM ROOM=TEST
ANALOG_NAND_ANI0_VREF		PP12871	P2MM-NSM SM ROOM=TEST
IO_PMU_TO_NAND_SYSTEM_ALIVE	电源到硬盘激活信号	PP12872	P2MM-NSM SM ROOM=TEST

IO_SOC_DFU_STATUS	DFU状态信号	PP12873	P2MM-NSM SM ROOM=TEST
IO_SOC_DFU_STATUS	DFU状态信号 MAKE_BASE=TRUE		
IO_PAD_MTR_ANALOG_TEST_P		PP12874	P2MM-NSM SM ROOM=TEST
IO_PAD_MTR_ANALOG_TEST_P	MAKE_BASE=TRUE		
IO_PAD_MTR_ANALOG_TEST_N		PP12875	P2MM-NSM SM ROOM=TEST
IO_PAD_MTR_ANALOG_TEST_N	MAKE_BASE=TRUE		

Miscellaneous

GPIO_AP_TO_CCG2B_SWCLK	CPU到快充芯片SWD总线时钟	PP12876	P2MM-NSM SM ROOM=TEST

Parrot

GPIO0_PARROT		PP12877	P2MM-NSM SM ROOM=TEST
GPIO1_PARROT		PP12878	P2MM-NSM SM ROOM=TEST

Bump Sense

ANALOG_PCPU_SENSE_P		PP12879	P2MM-NSM SM ROOM=TEST
ANALOG_PCPU_SENSE_N		PP12880	P2MM-NSM SM ROOM=TEST
ANALOG_GPU_SENSE_P		PP12881	P2MM-NSM SM ROOM=TEST
ANALOG_GPU_SENSE_N		PP12882	P2MM-NSM SM ROOM=TEST
ANALOG_SOC_SENSE_P		PP12883	P2MM-NSM SM ROOM=TEST
ANALOG_SOC_SENSE_N		PP12884	P2MM-NSM SM ROOM=TEST
ANALOG_DCS_SENSE_SE		PP12885	P2MM-NSM SM ROOM=TEST
ANALOG_DDR_SENSE_SE		PP12886	P2MM-NSM SM ROOM=TEST
ANALOG_ECPU_SENSE_SE		PP12887	P2MM-NSM SM ROOM=TEST
ANALOG_VDDQL_SENSE_SE		PP12888	P2MM-NSM SM ROOM=TEST

SOC Debug

IO_AON_TO_AP_XTAL_CFSB	CPU内部端口休眠唤醒信号	PP12889	P2MM-NSM SM ROOM=TEST
CLK_AP_TO_PMU_TST_CLKOUT	CPU到电源的测试时钟	PP12890	P2MM-NSM SM ROOM=TEST
IO_AP_FROM_PMU_PRE_UVLO_L		PP12891	P2MM-NSM SM ROOM=TEST

Dotara

GPIO_DOTARA_SWD_1V8		PP12892	P2MM-NSM SM ROOM=DOTARA
DOTARA_SUPER_GPIO_1V8	MAKE_BASE=TRUE	PP12893	P2MM-NSM SM ROOM=DOTARA
I2C_SDA_DOTARA_1V8	CKPLUS_WAIVE=I2C_PULLUP	PP12895	P2MM-NSM SM ROOM=DOTARA
I2C_SCL_DOTARA_1V8	CKPLUS_WAIVE=I2C_PULLUP	PP12896	P2MM-NSM SM ROOM=DOTARA
IO_DOTARA_DFT1_1V8		PP12897	P2MM-NSM SM ROOM=DOTARA
IO_DOTARA_DFT2_1V8		PP12898	P2MM-NSM SM ROOM=DOTARA
IO_DOTARA_TO_DOMBRA_EN_1V8	无线充电芯片到转换芯片开启	PP12899	P2MM-NSM SM ROOM=DOTARA
GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	电源到点阵芯片的开启信号	PP128A0	P2MM-NSM SM ROOM=DOTARA
IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8	触摸输出的强制同步信号	PP128A1	P2MM-NSM SM ROOM=DOTARA
IO_DOTARA_MTP_WREN_1V8		PP128A2	P2MM-NSM SM ROOM=DOTARA
IO_DOTARA_TO_DOMBRA_FPWM_1V8	无线充电芯片到转换芯片供电调节信号	PP128A3	P2MM-NSM SM ROOM=DOTARA
PP1V8_DOTARA_LDO		PP128A4	P2MM-NSM SM ROOM=DOTARA
CLK_BBPMU_TO_DOTARA_38M4	基带时钟芯片到无线充电芯片38.4M时钟 PLACE_SIDE=TOP	PP12802	P2MM-NSM SM ROOM=DOTARA

TOUCH

SPI2_AP_TO_TOUCH_CS_L	CPU到触摸的片选信号	PP128C0	P2MM-NSM SM ROOM=TOUCH
SPI2_AP_TO_TOUCH_SCLK	CPU到触摸的SPI总线时钟	PP128C1	P2MM-NSM SM ROOM=TOUCH
SPI2_AP_FROM_TOUCH_MISO	触摸到CPU的SPI总线数据	PP128C2	P2MM-NSM SM ROOM=TOUCH
SPI2_AP_TO_TOUCH_MOSI	CPU到触摸的SPI总线数据	PP128C3	P2MM-NSM SM ROOM=TOUCH

PMU

CLK_PMU_TO_AOP_32K	电源到CPU的32K时钟	PP128A5	P2MM-NSM SM ROOM=TEST
IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY	电源输出的准备就绪信号	PP128A6	P2MM-NSM SM ROOM=TEST
IO_SOC_TO_PMU_WDOG_RESET	CPU到电源的看门狗信号	PP128A7	P2MM-NSM SM ROOM=TEST
IO_SOC_TO_PMU_SOCHOT_RESET_L		PP128A8	P2MM-NSM SM ROOM=TEST
SWD_NUB_BI_PMU_SWDIO	CPU到电源的SPMI总线数据	PP128A9	P2MM-NSM SM ROOM=TEST

Adams

GPIO_CAM_PMU2_TO_WILL_EN_1V8	相机电源2到点阵供电芯片的开启信号	PP128B2	P2MM-NSM SM ROOM=TEST
GPIO_CAM_PMU1_TO_SWIDE_LDO_EN_1V8		PP128B3	P2MM-NSM SM ROOM=TEST
GPIO_CAM_PMU2_TO_TELE_LDO_EN_1V8		PP128B4	P2MM-NSM SM ROOM=TEST
GPIO_CAM_PMU2_FROM_WILL_JASPER_INT_L_1V8		PP128B5	P2MM-NSM SM ROOM=TEST
SPMI_ISP_TO_CAM_PMU1_CLK	CPU到相机电源1 SPMI总线时钟	PP128B6	P2MM-NSM SM ROOM=TEST
SPMI_ISP_BI_CAM_PMU1_DATA	CPU到相机电源1 SPMI总线数据	PP128B7	P2MM-NSM SM ROOM=TEST
SPMI_ISP_TO_CAM_PMU2_CLK	CPU到相机电源2 SPMI总线时钟	PP128B8	P2MM-NSM SM ROOM=TEST
SPMI_ISP_BI_CAM_PMU2_DATA	CPU到相机电源2 SPMI总线数据	PP128B9	P2MM-NSM SM ROOM=TEST

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J_INT_BOT
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998-21759
OMIT

95	GND	1	IO1	IO91	91	IO_BT_TO_R1_WAKE	95
95	GND	2	IO2	IO92	92	GPIO_R1_TO_BB_LAA_SW_CTRL	95
95	GND	3	IO3	IO93	93	GND	95
95	GND	4	IO4	IO94	94	GPIO_AP_FROM_WLAN_TIME_SYNC	95
95	NFC_P_ANT_NEG	5	IO5	IO95	95	GPIO_BB_TO_R1_COEX	95
95	GND	6	IO6	IO96	96	GND	95
95	NFC_P_ANT_NEG	7	IO7	IO97	97	GND	95
95	GND	8	IO8	IO98	98	IO_BT_TO_R1_TIME_SYNC	95
95	NFC_P_ANT_NEG	9	IO9	IO99	99	GPIO_R1_TO_WLAN_COEX	95
95	GND	10	IO10	IO100	100	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	95
95	NFC_P_ANT_NEG	11	IO11	IO101	101	GND	95
95	GPIO_NFC_F_NFC_P_SYNC2	12	IO12	IO102	102	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	95
95	GND	13	IO13	IO103	103	GPIO_WLAN_TO_R1_COEX	95
95	GND	14	IO14	IO104	104	GND	95
95	50_TRX_ANT4_MB_HB_WLAN24	15	IO15	IO105	105	GND	95
95	GND	16	IO16	IO106	106	NFC_P_ANT_POS	95
95	GND	17	IO17	IO107	107	GND	95
95	PCIE_GP1_AP_TO_WLAN_PERST_L	18	IO18	IO108	108	NFC_P_ANT_POS	95
95	GPIO_AP_TO_BB_PEAK_PWR_IND	19	IO19	IO109	109	GND	95
95	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	20	IO20	IO110	110	NFC_P_ANT_POS	95
95	SWD_AP_BI_BB_SWDIO	21	IO21	IO111	111	GND	95
95	NTC_STOCKHOLM	22	IO22	IO112	112	NFC_P_ANT_POS	95
95	GPIO_R1_TO_BB_CH9_COEX	23	IO23	IO113	113	GND	95
95	GPIO_NFC_F_NFC_P_SYNC1	24	IO24	IO114	114	CLK_BBPMU_TO_DOTARA_38M4	95
95	GND	25	IO25	IO115	115	GND	95
95	GND	26	IO26	IO116	116	GND	95
95	PP1V2_S4	27	IO27	IO117	117	GND	95
95	GND	28	IO28	IO118	118	GND	95
95	I2C_R1_TO_NFC_SCL	29	IO29	IO119	119	50_WLAN_A_C0_TXRX_FEM_M	95
95	GND	30	IO30	IO120	120	GND	95
95	I2C_R1_TO_NFC_SDA	31	IO31	IO121	121	GND	95
95	GND	32	IO32	IO122	122	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	95
95	NFC_P_TEST_OUT	33	IO33	IO123	123	GND	95
95	GND	34	IO34	IO124	124	GND	95
95	GND	35	IO35	IO125	125	50_TRX_ANT2_LB_LMB_MB_HB_L1	95
95	GND	36	IO36	IO126	126	GND	95
95	GND	37	IO37	IO127	127	GND	95
95	GND	38	IO38	IO128	128	50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M	95
95	GND	39	IO39	IO129	129	GND	95
95	GND	40	IO40	IO130	130	GND	95
95	GND	41	IO41	IO131	131	50_LAA_RX_XCVR_DRX10	95
95	GND	42	IO42	IO132	132	GND	95
95	GND	43	IO43	IO133	133	GND	95
95	GND	44	IO44	IO134	134	GND	95
95	GND	45	IO45	IO135	135	IO_TOUCH_TO_MANY_SCAN_ACTIVE	95
95	GND	46	IO46	IO136	136	GND	95
95	GND	47	IO47	IO137	137	GND	95
95	GND	48	IO48	IO138	138	GND	95
95	GND	49	IO49	IO139	139	GPIO_CANARY_1B_TO_1C	95
95	GND	50	IO50	IO140	140	GND	95
95	GND	51	IO51	IO141	141	GND	95
95	GND	52	IO52	IO142	142	GND	95
95	GND	53	IO53	IO143	143	GND	95
95	GND	54	IO54	IO144	144	GND	95
95	GND	55	IO55	IO145	145	GND	95
95	GND	56	IO56	IO146	146	GND	95
95	GND	57	IO57				
95	GND	58	IO58				
95	GND	59	IO59	IO149	149	GND	95
95	GND	60	IO60	IO150	150	GND	95
95	GND	61	IO61	IO151	151	GND	95
95	GND	62	IO62	IO152	152	GND	95
95	GND	63	IO63	IO153	153	GND	95
95	GND	64	IO64	IO154	154	GND	95
95	GND	65	IO65	IO155	155	GND	95
95	GND	66	IO66	IO156	156	GND	95
95	GND	67	IO67	IO157	157	GND	95
95	GND	68	IO68	IO158	158	GND	95
95	GND	69	IO69	IO159	159	GND	95
95	GND	70	IO70	IO160	160	GND	95
95	GND	71	IO71	IO161	161	GND	95
95	GND	72	IO72	IO162	162	GND	95
95	GND	73	IO73	IO163	163	GND	95
95	GND	74	IO74	IO164	164	GND	95
95	GND	75	IO75	IO165	165	GND	95
95	GND	76	IO76	IO166	166	GND	95
95	GND	77	IO77	IO167	167	GND	95
95	GND	78	IO78	IO168	168	GND	95
95	GND	79	IO79	IO169	169	GND	95
95	GND	80	IO80	IO170	170	GND	95
95	GND	81	IO81	IO171	171	GND	95
95	GND	82	IO82	IO172	172	GPIO_CANARY_1B_TO_1C	95
95	GND	83	IO83	IO173	173	GND	95
95	GND	84	IO84	IO174	174	GND	95
95	GND	85	IO85	IO175	175	GND	95
95	GPIO_BB_TO_R1_CH9_REQ	86	IO86	IO176	176	SHIELD_RFFE5_SCLK_SDR	95
95	GND	87	IO87	IO177	177	GND	95
95	SWD_AP_TO_MANY_SWCLK	88	IO88	IO178	178	SHIELD_RFFE5_SDATA_SDR	95
95	GND	89	IO89	IO179	179	GND	95
95	UAT_TUNER_TO_R1_STATE	90	IO90	IO180	180	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	95

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96	GPIO_AP_CANARY1	181	IO181	IO271	271	GPIO_S4_PMU_TO_WLAN_REG_ON	96
96	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	182	IO182	IO272	272	GND	96
96	GND	183	IO183	IO273	273	GND	96
96	CLK_BBPMU_TO_NFC_38M	184	IO184	IO274	274	GPIO_PMU_FROM_WLAN_HOST_WAKE	96
96	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	185	IO185	IO275	275	GND	96
96	GND	186	IO186	IO276	276	PP1V8_S4	96
96	GND	187	IO187	IO277	277	PP_1V8_LDO6	96
96	I2S2_AP_TO_BB_DOUT	188	IO188	IO278	278	GND	96
96	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	189	IO189	IO279	279	PP_APT_L_PA	96
96	I2S2_AP_FROM_BB_DIN	190	IO190	IO280	280	GND	96
96	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	191	IO191	IO281	281	PP_APT_L_PA	96
96	I2S2_AP_FROM_BB_BCLK	192	IO192	IO282	282	IO_TOUCH_TO_MANY_SCAN_ACTIVE	96
96	GND	193	IO193	IO283	283	GND	96
96	I2S2_AP_FROM_BB_LRCLK	194	IO194	IO284	284	GND	96
96	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	195	IO195	IO285	285	SHIELD_ETDAC_QET1_N	96
96	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	196	IO196	IO286	286	GND	96
96	GPIO_NFC_TO_BBPMU_CLK_EN	197	IO197	IO287	287	SHIELD_ETDAC_QET1_P	96
96	GND	198	IO198	IO288	288	GND	96
96	GND	199	IO199	IO289	289	SUBUS_LAT_A	96
96	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	200	IO200	IO290	290	GND	96
96	GND	201	IO201	IO291	291	SHIELD_RFFE8_SCLK_SDR	96
96	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	202	IO202	IO292	292	GND	96
96	GND	203	IO203	IO293	293	SHIELD_RFFE8_SDATA_SDR	96
96	GND	204	IO204	IO294	294	GND	96
96	GND	205	IO205	IO295	295	GND	96
96	90_PCIE_GP2_AP_TO_BB_REFCLK_N	206	IO206	IO296	296	GND	96
96	GND	207	IO207	IO297	297	GND	96
96	90_PCIE_GP2_AP_TO_BB_REFCLK_P	208	IO208	IO298	298	GND	96
96	GND	209	IO209	IO299	299	GND	96
96	GND	210	IO210	IO300	300	GND	96
96	GND	211	IO211	IO301	301	GND	96
96	GND	212	IO212	IO302	302	GND	96
96	GND	213	IO213	IO303	303	GND	96
96	GND	214	IO214	IO304	304	GND	96
96	GND	215	IO215	IO305	305	GND	96
96	GND	216	IO216	IO306	306	50_RX_XCVR_PRX14_N79_RX_OUT1	96
96	GND	217	IO217	IO307	307	GND	96
96	GND	218	IO218	IO308	308	GND	96
96	GND	219	IO219	IO309	309	50_RX_XCVR_PRX16_UHB_RX_OUT1	96
96	GND	220	IO220	IO310	310	GND	96
96	GND	221	IO221	IO311	311	GND	96
96	GND	222	IO222	IO312	312	50_TRX_UHB_PAD_PORTB_TX_M	96
96	90_PCIE_GP1_AP_FROM_WLAN_RX_N	223	IO223	IO313	313	GND	96
96	GND	224	IO224	IO314	314	GND	96
96	90_PCIE_GP1_AP_FROM_WLAN_RX_P	225	IO225	IO315	315	50_TRX_UHB_PAD_N79_PORTB_TX_M	96
96	GND	226	IO226	IO316	316	GND	96
96	GND	227	IO227	IO317	317	GND	96
96	GND	228	IO228	IO318	318	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	96
96	90_PCIE_GP1_AP_TO_WLAN_TX_P	229	IO229	IO319	319	GND	96
96	GND	230	IO230	IO320	320	GND	96
96	90_PCIE_GP1_AP_TO_WLAN_TX_N	231	IO231	IO321	321	50_RX_XCVR_PRX15_N79_RX_OUT2	96
96	GND	232	IO232	IO322	322	GND	96
96	GND	233	IO233	IO323	323	GND	96
96	GND	234	IO234	IO324	324	50_TX_IN_XCVR_TX1_LB_JB	96
96	90_PCIE_GP2_AP_FROM_BB_RX_N	235	IO235	IO325	325	50_TX_IN_XCVR_TX0_LB	96
96	GND	236	IO236	IO326	326	GND	96
96	90_PCIE_GP2_AP_FROM_BB_RX_P	237	IO237	IO327	327	GND	96
96	GND	238	IO238	IO328	328	50_RX_XCVR_PRX6_LB_A_RX0	96
96	GND	239	IO239	IO329	329	50_RX_XCVR_PRX10_LB_PRX_OUT2	96
96	GND	240	IO240	IO330	330	GND	96
96	90_PCIE_GP2_AP_TO_BB_TX_P	241	IO241	IO331	331	GND	96
96	GND	242	IO242	IO332	332	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	96
96	90_PCIE_GP2_AP_TO_BB_TX_N	243	IO243	IO333	333	GND	96
96	GND	244	IO244	IO334	334	GND	96
96	GND	245	IO245	IO335	335	50_RX_XCVR_PRX17_UHB_RX_OUT2	96
96	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	246	IO246	IO336	336	GND	96
96	GND	247	IO247	IO337	337	GND	96
96	GND	248	IO248	IO338	338	50_UHB_L_CPLR_OUT	96
96	GPIO_AOP_TO_WLAN_CONTEXT_A	249	IO249	IO339	339	GND	96
96	GPIO_AOP_TO_BB_FORCE_PWM	250	IO250	IO340	340	GND	96
96	GPIO_AOP_TO_WLAN_CONTEXT_B	251	IO251	IO341	341	GND	96
96	GND	252	IO252	IO342	342	GND	96
96	ANALOG_PP_GPU_LVCC	253	IO253	IO343	343	GND	96
96	IO_PMU_TO_SYSTEM_RESET_L	254	IO254	IO344	344	GND	96
96	GND	255	IO255	IO345	345	GND	96
96	GND	256	IO256	IO346	346	GND	96
96	SUBUS_UAT_B	257	IO257	IO347	347	GND	96
96	ANALOG_PP_CPU_PCORE_LVCC	258	IO258	IO348	348	GND	96
96	SUBUS_UAT_A	259	IO259	IO349	349	GND	96
96	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	260	IO260	IO350	350	GND	96
96	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	261	IO261	IO351	351	GND	96
96	GND	262	IO262	IO352	352	GND	96
96	GND	263	IO263	IO353	353	GND	96
96	GND	264	IO264	IO354	354	GND	96
96	GND	265	IO265	IO355	355	GND	96
96	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	266	IO266	IO356	356	GND	96
96	GND	267	IO267	IO357	357	GND	96
96	GND	268	IO268	IO358	358	GND	96
96	GND	269	IO269	IO359	359	GND	96
96	PP1V2_S2	270	IO270	IO360	360	GND	96

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97	GND	361	IO361	451	SHIELD_RFFE3_SCLK_SDR
97	GND	362	IO362	452	GND
97	GND	363	IO363	453	SHIELD_RFFE3_SDATA_SDR
97	GND	364	IO364	454	GND
97	GND	365	IO365	455	SHIELD_RFFE2_SCLK_SDR
97	GND	366	IO366	456	GND
97	GND	367	IO367	457	SHIELD_RFFE2_SDATA_SDR
97	GND	368	IO368	458	GND
97	GND	369	IO369	459	GND
97	GND	370	IO370	460	GND
97	GND	371	IO371	461	GND
97	GND	372	IO372	462	PP_VBUS1_E75
97	GND	373	IO373	463	PP_VBUS1_E75
97	GND	374	IO374	464	GND
97	GND	375	IO375	465	PP_UIM1_LDO11
97	GND	376	IO376	466	IO_BB_FROM_SIM2_DETECT
97	GND	377	IO377	467	PP_UIM2_LDO13
97	GND	378	IO378	468	GND
97	GND	379	IO379	469	IO_BB_TO_SIM2_CLK
97	GND	380	IO380	470	IO_BB_TO_SIM2_RESET
97	GND	381	IO381	471	IO_BB_BI_SIM2_DATA
97	50_TRX_LB_PORTB_RX1_M	382	IO382	472	GND
97	GND	383	IO383	473	GND
97	GND	384	IO384	474	GND
97	50_TRX_LB_PORTB_TX_M	385	IO385	475	GND
97	GND	386	IO386	476	GND
97	GND	387	IO387	477	IO_BB_FROM_SIM1_DETECT
97	PP_VDD_RF_1V2	388	IO388	478	IO_BB_TO_SIM1_RESET
97	SUBUS_LAT_C	389	IO389	479	IO_BB_BI_SIM1_DATA
97	GND	390	IO390	480	GND
97	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	391	IO391	481	IO_BB_TO_SIM1_CLK
97	SUBUS_LAT_B	392	IO392	482	GPIO_SEQ_PMU_TO_NFC_EN
97	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	393	IO393	483	GND
97	GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN	394	IO394	484	GND
97	GND	395	IO395	485	AMUX_PMU_BY
97	GND	396	IO396	486	AMUX_PMU_AY
97	50_TRX_L5_LNA_IN	397	IO397	487	NTC_RADIO_BB_SE
97	GND	398	IO398	488	GND
97	GND	399	IO399	489	NTC_RADIO_PA_SE
97	GND	400	IO400	490	PP1V2_NFC_S2
97	50_TRX_WLAN_G_BT_ANT3_NPLXR	401	IO401	491	GND
97	GND	402	IO402	492	GND
97	GND	403	IO403	493	GND
97	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	404	IO404	494	GPIO_SEQ_PMU_TO_BBPMU_RESET_L
97	GND	405	IO405	495	GND
97	GND	406	IO406	496	GND
97	50_WLAN_A_C1_TXRX_FEM_M	407	IO407	497	GND
97	GND	408			
97	GND	409	IO409	499	GND
97	50_LAA_RX_XCVR_PRX12	410	IO410	500	GND
97	GND	411	IO411	501	GND
97	GND	412	IO412	502	GND
97	50_TRX_HB_PAD_ANT1	413	IO413	503	GND
97	RFFE_WLAN_TO_LAT_5G_FEM_RST_L	414	IO414	504	GND
97	GND	415	IO415	505	GND
97	GND	416	IO416	506	PP3V0_S2
97	SHIELD_RFFE1_SCLK_SDR	417	IO417	507	UART1_AOP_FROM_BB_RXD
97	GND	418	IO418	508	GND
97	SHIELD_RFFE1_SDATA_SDR	419	IO419	509	GND
97	GND	420	IO420	510	GPIO_NFC_TO_ARCAMP_RESET_L
97	GND	421	IO421	511	UART1_AOP_TO_BB_TXD
97	GND	422	IO422	512	GND
97	GND	423	IO423	513	GPIO_AP_TO_BB_TIME_MARK
97	GND	424	IO424	514	GPIO_NFC_TO_ARCAMP_TRIG
97	GND	425	IO425	515	GPIO_AP_FROM_BT_AUDIO_SYNC
97	GND	426	IO426	516	GND
97	GND	427	IO427	517	PP1V8_S2
97	GND	428	IO428	518	GPIO_AP_TO_BB_COREDUMP
97	PP_VDD_BOOST	429	IO429	519	GPIO_BT_TO_BOT_SPKR_TRIG
97	GND	430	IO430	520	GND
97	GND	431	IO431	521	GND
97	GND	432	IO432	522	GND
97	50_TRX_HB_PAD_ANT2_M	433	IO433	523	PP_VDD_MAIN
97	GND	434	IO434	524	GND
97	GND	435	IO435	525	PP_VDD_MAIN
97	GND	436	IO436	526	GND
97	GND	437	IO437	527	PP_VDD_MAIN
97	GND	438	IO438	528	GND
97	50_CPLR_L_CPL1_LAT_OUT	439	IO439	529	PP_VDD_MAIN
97	GND	440	IO440	530	GND
97	GND	441	IO441	531	PP_VDD_MAIN
97	GND	442	IO442	532	GND
97	GND	443	IO443	533	GND
97	GND	444	IO444	534	GND
97	GND	445	IO445	535	PP_VDD_MAIN
97	GND	446	IO446	536	GND
97	GND	447	IO447	537	PP_VDD_MAIN
97	GND	448	IO448	538	GND
97	GND	449	IO449	539	PP_VDD_MAIN
97	GND	450	IO450	540	GND

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98	PP_VDD_MAIN	541	IO541
98	GND	542	IO542
98	PP_VDD_MAIN	543	IO543
98	GPIO_AP_CANARY2	544	IO544
98	GND	545	IO545
98	GND	546	IO546
98	PP_VDD_MAIN	547	IO547
98	GND	548	IO548
98	GND	549	IO549
98	GND	550	IO550
98	GND	551	IO551
98	GND	552	IO552
98	GND	553	IO553
98	GND	554	IO554
98	GND	555	IO555
98	GND	556	IO556
98	GND	557	IO557
98	GND	558	IO558
98	GND	559	IO559
98	GND	560	IO560
98	GND	561	IO561
98	GPIO_CANARY_2B_TO_2C	562	IO562
98	GND	563	IO563
98	GND	564	IO564
98	GND	565	IO565
98	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	566	IO566
98	GND	567	IO567
98	GPIO_AP_FROM_BB_RESET_DETECT_L	568	IO568
98	GND	569	IO569
98	PCIE_GP2_AP_TO_BB_PERST_L	570	IO570
98	GND	571	IO571
98	GND	572	IO572
98	GND	573	IO573
98	PCIE_GP2_AP_BI_BB_CLKREQ_L	574	IO574
98	GND	575	IO575
98	GND	576	IO576
98	GND	577	IO577
98	GPIO_CANARY_2B_TO_2C	578	IO578
98	GND	579	IO579
98	GND	580	IO580
98	GND	581	IO581
98	GND	582	IO582
98	GND	583	IO583
98	GND	584	IO584
98	GND	585	IO585
98	GND	586	IO586
98	GND	587	IO587
98	GND	588	IO588
98	GND	589	IO589
98	GND	590	IO590
98	GND	591	IO591
98	GND	592	IO592
98	GND	593	IO593
98	GND	594	IO594
98	GND	595	IO595
98	GND	596	IO596
98	GND	597	IO597
98	GND	598	IO598
98	GND	599	IO599
98	GND	600	IO600
98	GND	601	IO601
98	GND	602	IO602
98	GND	603	IO603
98	GND	604	IO604
98	GND	605	IO605

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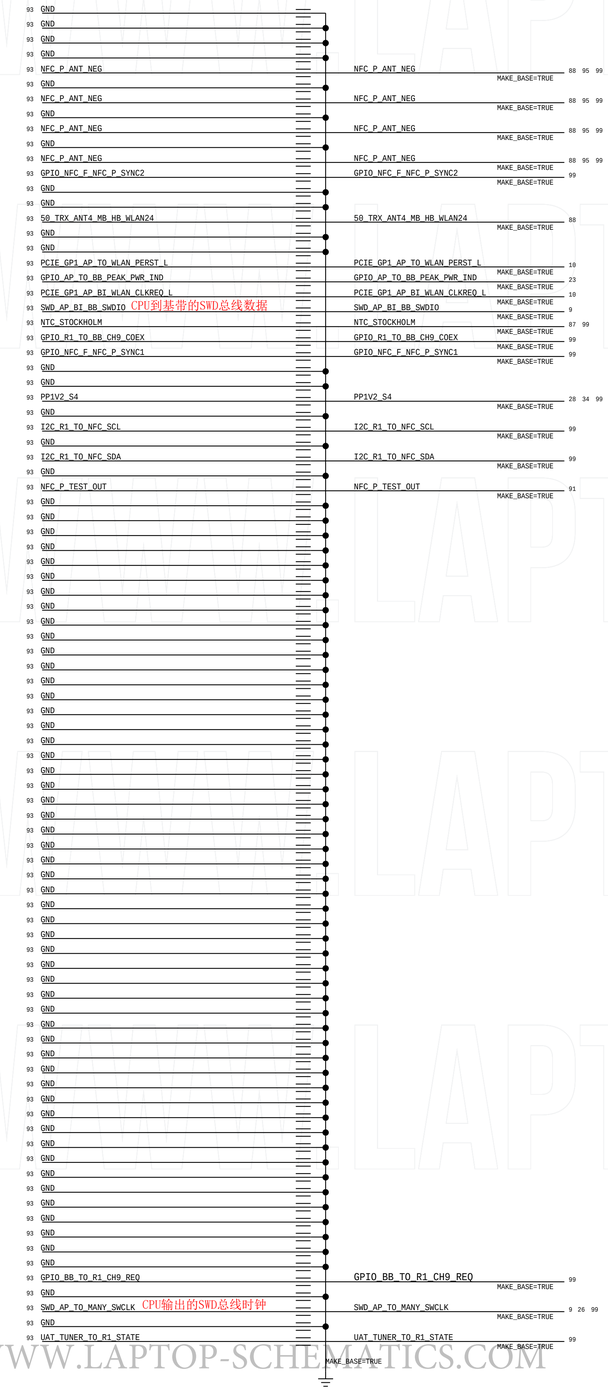

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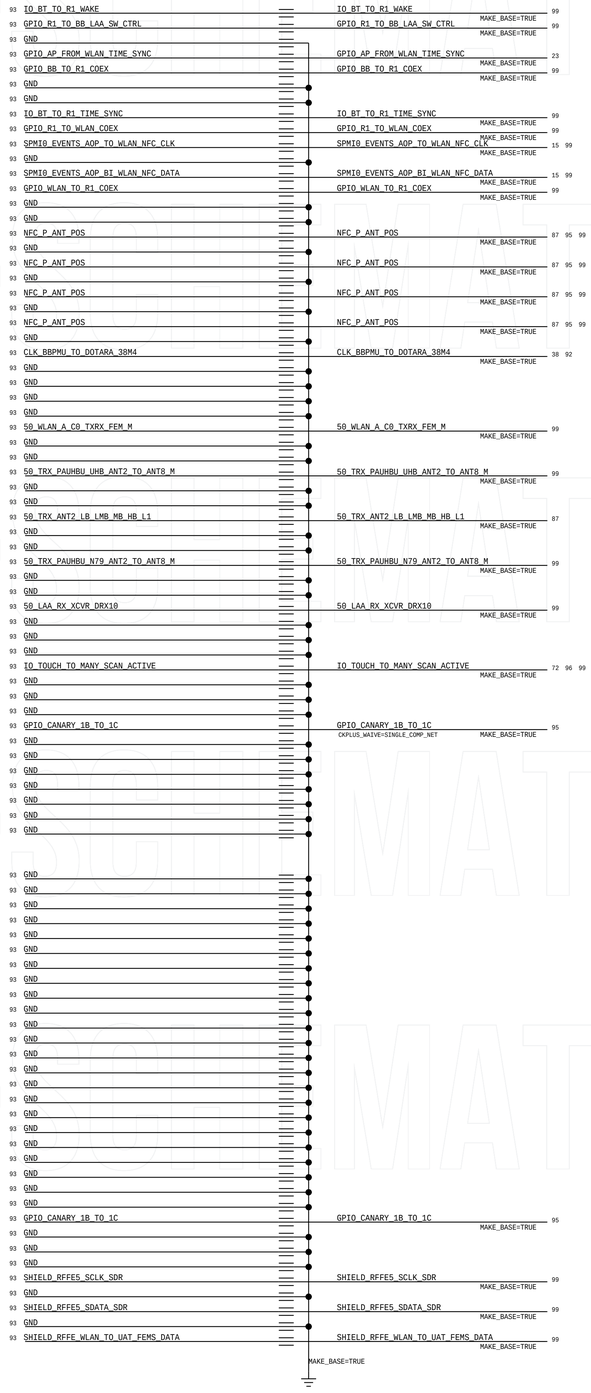
93 IO_BT_TO_R1_WAKE
IO_BT_TO_R1_WAKE
99
93 GPIO_R1_TO_BB_LAA_SW_CTRL
GPIO_R1_TO_BB_LAA_SW_CTRL
99
93 GND
93 GPIO_AP_FROM_WLAN_TIME_SYNC
GPIO_AP_FROM_WLAN_TIME_SYNC
23
93 GPIO_BB_TO_R1_COEX
GPIO_BB_TO_R1_COEX
99
93 GND
93 GND
93 IO_BT_TO_R1_TIME_SYNC
IO_BT_TO_R1_TIME_SYNC
99
93 GPIO_R1_TO_WLAN_COEX
GPIO_R1_TO_WLAN_COEX
99
93 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
15 99
93 GND
93 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA
SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA
15 99
93 GPIO_WLAN_TO_R1_COEX
GPIO_WLAN_TO_R1_COEX
99
93 GND
93 GND
93 NFC_P_ANT_POS
NFC_P_ANT_POS
87 95 99
93 GND
93 NFC_P_ANT_POS
NFC_P_ANT_POS
87 95 99
93 GND
93 NFC_P_ANT_POS
NFC_P_ANT_POS
87 95 99
93 GND
93 NFC_P_ANT_POS
NFC_P_ANT_POS
87 95 99
93 GND
93 CLK_BBPMU_TO_DOTARA_38M4
CLK_BBPMU_TO_DOTARA_38M4
38 92
93 GND
93 GND
93 GND
93 GND
93 50_WLAN_A_C0_TXRX_FEM_M
50_WLAN_A_C0_TXRX_FEM_M
99
93 GND
93 GND
93 50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M
99
93 GND
93 GND
93 50_TRX_ANT2_LB_LMB_MB_HB_L1
50_TRX_ANT2_LB_LMB_MB_HB_L1
87
93 GND
93 GND
93 50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M
99
93 GND
93 GND
93 50_LAA_RX_XCVR_DRX10
50_LAA_RX_XCVR_DRX10
99
93 GND
93 GND
93 GND
93 IO_TOUCH_TO_MANY_SCAN_ACTIVE
IO_TOUCH_TO_MANY_SCAN_ACTIVE
72 96 99
93 GND
93 GND
93 GND
93 GPIO_CANARY_1B_TO_1C
GPIO_CANARY_1B_TO_1C
CKFLUS_WAIVE=SINGLE_COMP_NET
95
93 GND
93 GND
93 GND
93 GND

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LEFT SIDE

93	GPIO_AP_CANARY1	GPIO_AP_CANARY1	MAKE_BASE=TRUE	23
93	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	MAKE_BASE=TRUE	99
93	GND			
93	CLK_BBPMU_TO_NFC_38M	CLK_BBPMU_TO_NFC_38M	MAKE_BASE=TRUE	99
93	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	I2S2_AP_TO_BB_DOUT	I2S2_AP_TO_BB_DOUT	MAKE_BASE=TRUE	13
93	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	MAKE_BASE=TRUE	99
93	I2S2_AP_FROM_BB_DIN	I2S2_AP_FROM_BB_DIN	MAKE_BASE=TRUE	13
93	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	MAKE_BASE=TRUE	99
93	I2S2_AP_FROM_BB_BCLK	I2S2_AP_FROM_BB_BCLK	MAKE_BASE=TRUE	13
93	GND			
93	I2S2_AP_FROM_BB_LRCLK	I2S2_AP_FROM_BB_LRCLK	MAKE_BASE=TRUE	13
93	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	MAKE_BASE=TRUE	81
93	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	MAKE_BASE=TRUE	31 33 92 99
93	GPIO_NFC_TO_BBPMU_CLK_EN	GPIO_NFC_TO_BBPMU_CLK_EN	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	MAKE_BASE=TRUE	10
93	GND			
93	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	MAKE_BASE=TRUE	10
93	GND			
93	GND			
93	GND			
93	90_PCIE_GP2_AP_TO_BB_REFCLK_N	90_PCIE_GP2_AP_TO_BB_REFCLK_N	MAKE_BASE=TRUE	10
93	GND			
93	90_PCIE_GP2_AP_TO_BB_REFCLK_P	90_PCIE_GP2_AP_TO_BB_REFCLK_P	MAKE_BASE=TRUE	10
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	90_PCIE_GP1_AP_FROM_WLAN_RX_N	90_PCIE_GP1_AP_FROM_WLAN_RX_N	MAKE_BASE=TRUE	25
93	GND			
93	90_PCIE_GP1_AP_FROM_WLAN_RX_P	90_PCIE_GP1_AP_FROM_WLAN_RX_P	MAKE_BASE=TRUE	25
93	GND			
93	GND			
93	GND			
93	90_PCIE_GP1_AP_TO_WLAN_TX_P	90_PCIE_GP1_AP_TO_WLAN_TX_P	MAKE_BASE=TRUE	10
93	GND			
93	90_PCIE_GP1_AP_TO_WLAN_TX_N	90_PCIE_GP1_AP_TO_WLAN_TX_N	MAKE_BASE=TRUE	10
93	GND			
93	GND			
93	GND			
93	90_PCIE_GP2_AP_FROM_BB_RX_N	90_PCIE_GP2_AP_FROM_BB_RX_N	MAKE_BASE=TRUE	25
93	GND			
93	90_PCIE_GP2_AP_FROM_BB_RX_P	90_PCIE_GP2_AP_FROM_BB_RX_P	MAKE_BASE=TRUE	25
93	GND			
93	GND			
93	GND			
93	90_PCIE_GP2_AP_TO_BB_TX_P	90_PCIE_GP2_AP_TO_BB_TX_P	MAKE_BASE=TRUE	10
93	GND			
93	90_PCIE_GP2_AP_TO_BB_TX_N	90_PCIE_GP2_AP_TO_BB_TX_N	MAKE_BASE=TRUE	10
93	GND			
93	GND			
93	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	MAKE_BASE=TRUE	15
93	GND			
93	GND			
93	GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A	MAKE_BASE=TRUE	24
93	GPIO_AOP_TO_BB_FORCE_PWM	GPIO_AOP_TO_BB_FORCE_PWM	MAKE_BASE=TRUE	23
93	GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B	MAKE_BASE=TRUE	24
93	GND			
93	ANALOG_PP_GPU_LVCC	ANALOG_PP_GPU_LVCC	MAKE_BASE=TRUE	91
93	IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	IO_PMU_TO_SYSTEM_RESET_L	MAKE_BASE=TRUE	24 31
93	GND			
93	GND			
93	SUBUS_UAT_B	SUBUS_UAT_B	MAKE_BASE=TRUE	82 88
93	ANALOG_PP_CPU_PCORE_LVCC	ANALOG_PP_CPU_PCORE_LVCC	MAKE_BASE=TRUE	91
93	SUBUS_UAT_A	SUBUS_UAT_A	MAKE_BASE=TRUE	87
93	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 强制DFU信号	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	MAKE_BASE=TRUE	9 24
93	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	GND			
93	GND			
93	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	MAKE_BASE=TRUE	33
93	GND			
93	GND			
93	GND			
93	PP1V2_S2	PP1V2_S2	MAKE_BASE=TRUE	24 30 34 56 69 79 80 86 99

RIGHT SIDE

93	GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO_S4_PMU_TO_WLAN_REG_ON	MAKE_BASE=TRUE	33
93	GND			
93	GND			
93	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE	MAKE_BASE=TRUE	33
93	GND			
93	PP1V8_S4	PP1V8_S4	MAKE_BASE=TRUE	28 34 92 99
93	PP_1V8_LDO6	PP_1V8_LDO6	MAKE_BASE=TRUE	90 99
93	GND			
93	PP_APT_L_PA	PP_APT_L_PA	MAKE_BASE=TRUE	96 99
93	GND			
93	PP_APT_L_PA	PP_APT_L_PA	MAKE_BASE=TRUE	96 99
93	IO_TOUCH_TO_MANY_SCAN_ACTIVE	IO_TOUCH_TO_MANY_SCAN_ACTIVE	MAKE_BASE=TRUE	72 95 99
93	GND			
93	GND			
93	SHIELD_ETDAC_QET1_N	SHIELD_ETDAC_QET1_N	MAKE_BASE=TRUE	99
93	GND			
93	SHIELD_ETDAC_QET1_P	SHIELD_ETDAC_QET1_P	MAKE_BASE=TRUE	99
93	GND			
93	SUBUS_LAT_A	SUBUS_LAT_A	MAKE_BASE=TRUE	84
93	GND			
93	SHIELD_RFFE8_SCLK_SDR	SHIELD_RFFE8_SCLK_SDR	MAKE_BASE=TRUE	99
93	GND			
93	SHIELD_RFFE8_SDATA_SDR	SHIELD_RFFE8_SDATA_SDR	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	50_RX_XCVR_PRX14_N79_RX_OUT1	50_RX_XCVR_PRX14_N79_RX_OUT1	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_RX_XCVR_PRX16_UHB_RX_OUT1	50_RX_XCVR_PRX16_UHB_RX_OUT1	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_TRX_UHB_PAD_PORTB_TX_M	50_TRX_UHB_PAD_PORTB_TX_M	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_TRX_UHB_PAD_N79_PORTB_TX_M	50_TRX_UHB_PAD_N79_PORTB_TX_M	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_RX_XCVR_PRX15_N79_RX_OUT2	50_RX_XCVR_PRX15_N79_RX_OUT2	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_TX_IN_XCVR_TX1_LB_JB	50_TX_IN_XCVR_TX1_LB_JB	MAKE_BASE=TRUE	99
93	50_TX_IN_XCVR_TX0_LB	50_TX_IN_XCVR_TX0_LB	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_RX_XCVR_PRX6_LB_A_RX0	50_RX_XCVR_PRX6_LB_A_RX0	MAKE_BASE=TRUE	99
93	50_RX_XCVR_PRX10_LB_PRX_OUT2	50_RX_XCVR_PRX10_LB_PRX_OUT2	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_RX_XCVR_PRX17_UHB_RX_OUT2	50_RX_XCVR_PRX17_UHB_RX_OUT2	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	50_UHB_L_CPLR_OUT	50_UHB_L_CPLR_OUT	MAKE_BASE=TRUE	99
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
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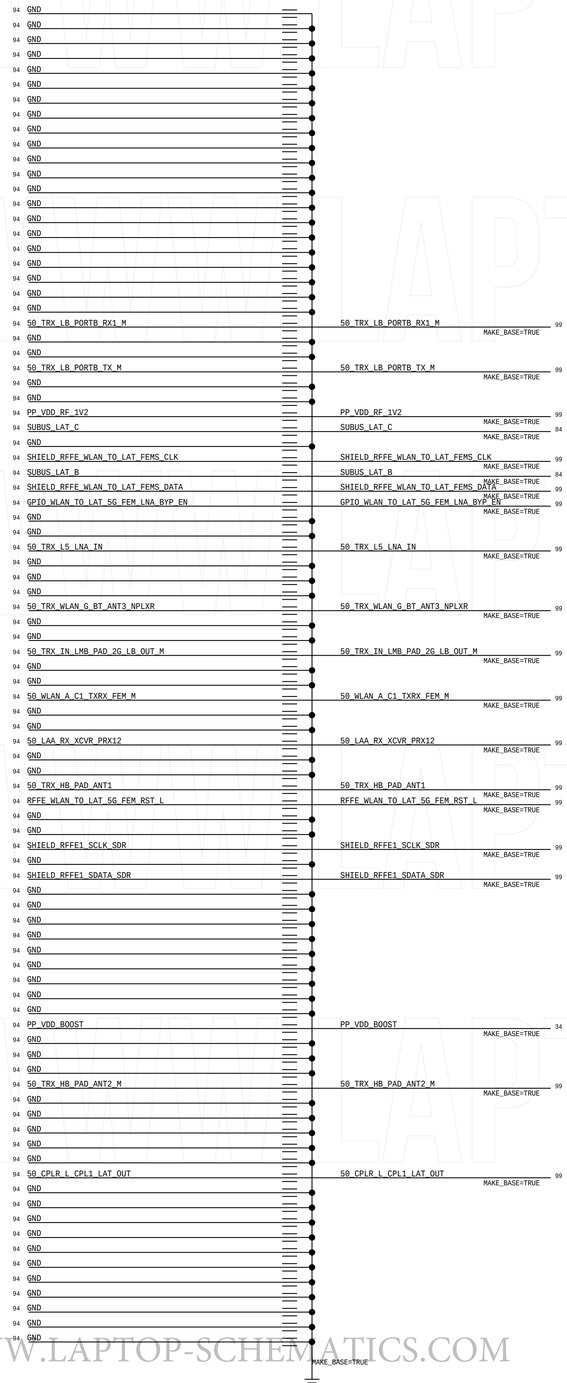
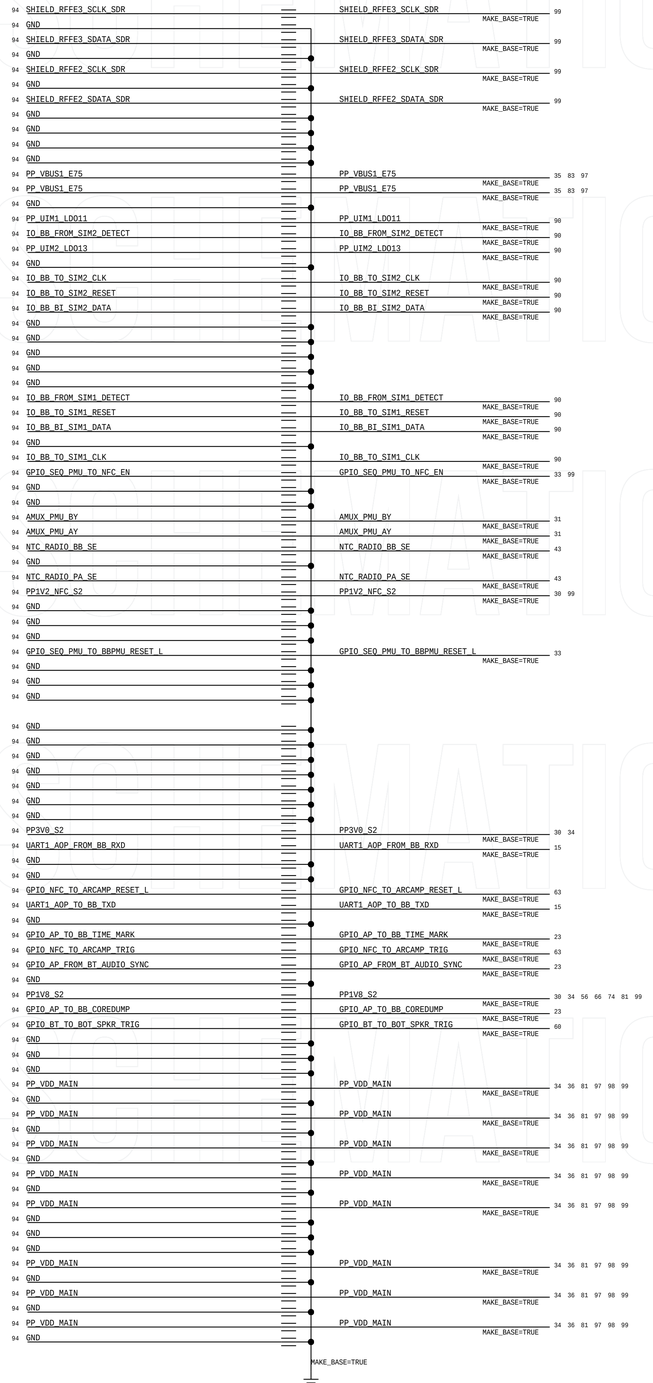
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND			
93	GND		

Interposer: Symbol 3 Aliases

LEFT SIDE



RIGHT SIDE



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PAGE TITLE	INTERPOSER: Aliases (3/4)
DRAWING NUMBER	051-05170
SIZE	D
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BRANCH	crb-1
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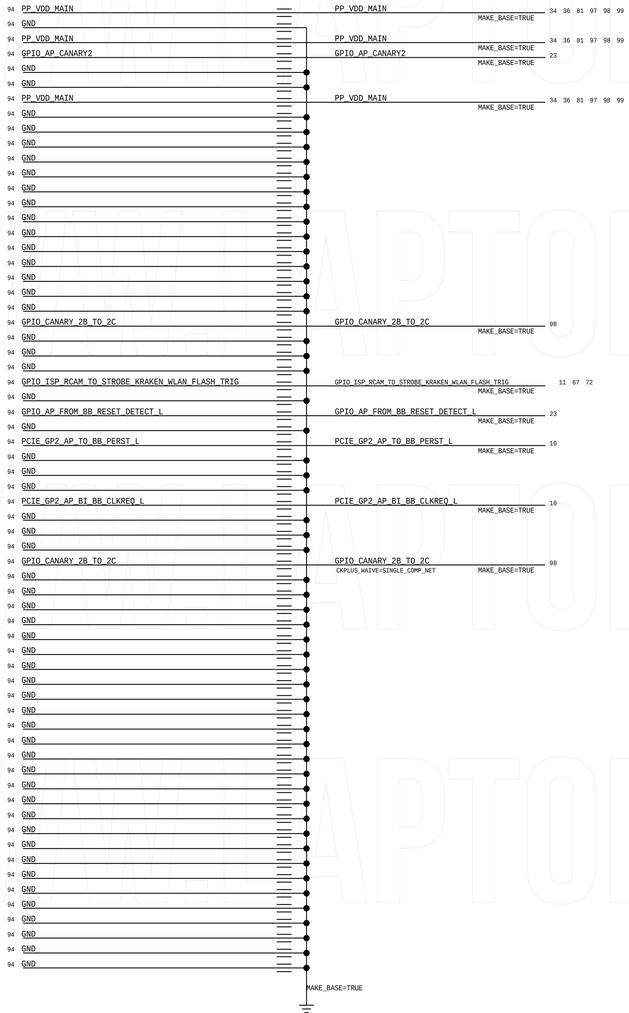
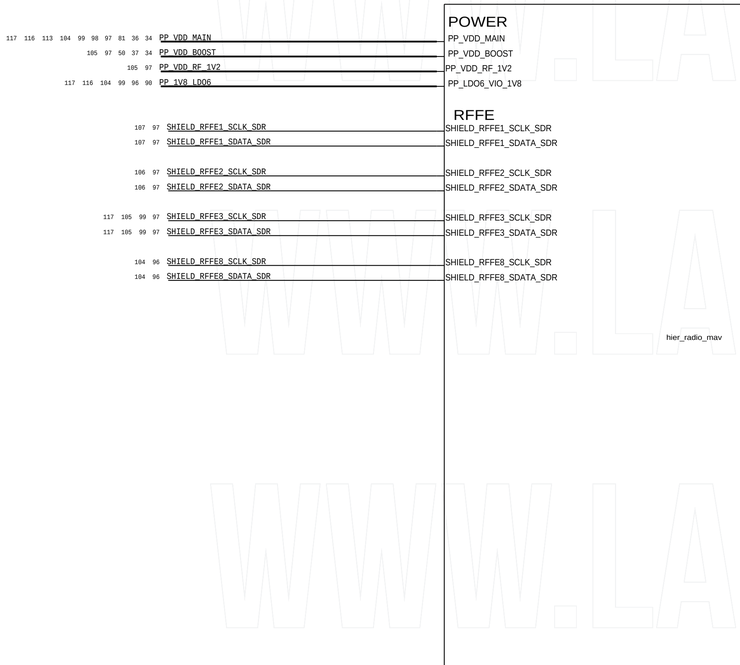
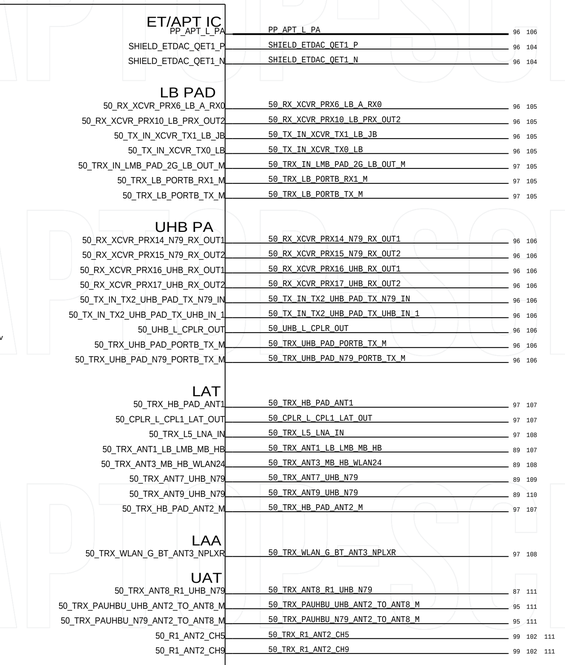
Interposer: Symbol 4 Aliases

LEFT SIDE

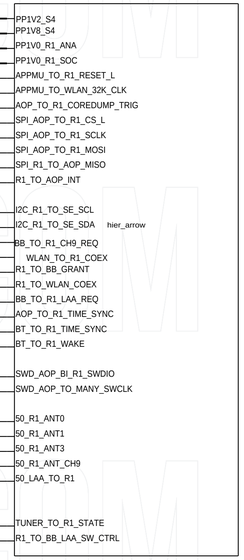

94 PP_VDD_MAIN
94 GND
94 PP_VDD_MAIN
94 GPIO_AP_CANARY2
94 GND
94 GND
94 PP_VDD_MAIN
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GPIO_CANARY_2B_TO_2C
94 GND
94 GND
94 GND
94 GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG
94 GND
94 GPIO_AP_FROM_BB_RESET_DETECT_L
94 GND
94 PCIE_GP2_AP_TO_BB_PERST_L
94 GND
94 GND
94 GND
94 PCIE_GP2_AP_BI_BB_CLKREQ_L
94 GND
94 GND
94 GND
94 GPIO_CANARY_2B_TO_2C
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND
94 GND

HIERARCHY BLOCKS





hier_radio_mav



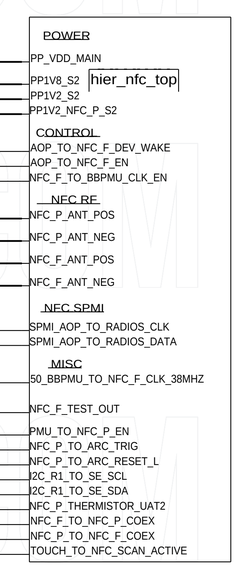
CPU到蓝牙WIFI NFC的SPMI总线数据

R13801 33.2 1% 1/32W MF 01005 ROOM=IRONMAN_NFC

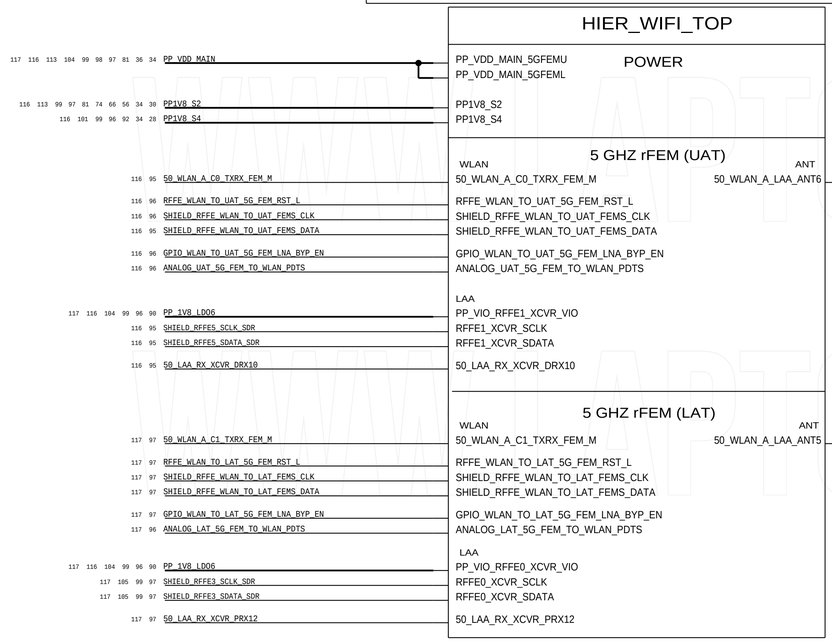
CPU到蓝牙WIFI NFC的SPMI总线数据

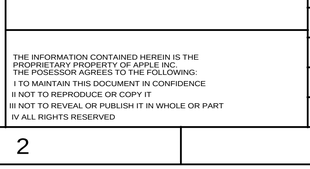
CPU到U1的SWD总线数据

CPU输出的SWD总线时钟



hier_nfc_top





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2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

ARROW MLB

LAST_MODIFICATION=Wed Jul 1 16:52:56 2020

PAGE	CSA	CONTENTS	SYNC	DATE
100 FRONT PAGE	1	FRONT PAGE		
101	2	MODULE		
102	3	FILTERS MATCHING		

POWER
- PP1V2_S4
- PP1V8_S4
- PP1V0_R1_ANA_S4
- PP1V0_S4

HOST IPC
- SPI0_AOP_TO_IMU_R1_SCLK
- GPIO_SCM_AOP_TO_R1_SPI_CS_L
- SPI0_AOP_FROM_IMU_R1_MISO
- SPI0_AOP_TO_IMU_R1_MOSI
- GPIO_AOP_TO_R1_COREDUMP_TRIGGER
- GPIO_SCM_AOP_FROM_R1_INT

RESET/CLOCK
- GPIO_S4_PMU_TO_R1_RESET_L
- CLK_GPIO_S4_PMU_TO_WLAN_R1_32K
- GPIO_AOP_TO_R1_TIME_SYNC_L

DEBUG
- SWD_AP_TO_MANY_SWCLK (CPU输出的SWD总线时钟)
- SWD_AP_BI_R1_SWDIO (CPU到U1的SWD总线数据)

SPMI/COEX GPIOS
- GPIO_WLAN_TO_R1_COEX
- GPIO_R1_TO_BB_CH9_COEX
- GPIO_R1_TO_WLAN_COEX
- GPIO_BB_TO_R1_COEX
- GPIO_BB_TO_R1_CH9_REQ

SE IPC
- I2C_R1_TO_NFC_SCL
- I2C_R1_TO_NFC_SDA

BT TIME SYNC / WAKE
- IO_BT_TO_R1_TIME_SYNC
- IO_BT_TO_R1_WAKE

ANTENNA SWITCH CTRL
- UAT_TUNER_TO_R1_STATE
- GPIO_R1_TO_BB_LAA_SW_CTRL

ANTENNA
- 50_TRX_R1_AOA1
- 50_TRX_R1_AOA2
- 50_TRX_R1_AOA3
- 50_TRX_R1_ANT2_CH9
- 50_TRX_R1_ANT2_CH5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00790	339S00774	?	U_ROSE_R	USI STRIDER2 MODULE

SCH #: 951-09582
PCB #: 920-05369
BOM #: 939-05686

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FRONT PAGE

DRAWING TITLE: SCH,MLB,TOP,D54
DRAWING NUMBER: 051-05170
SIZE: D
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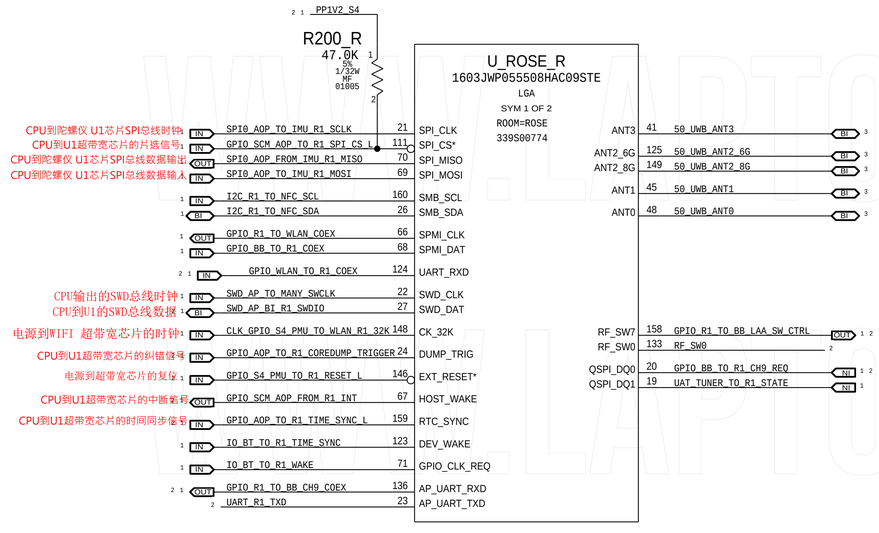
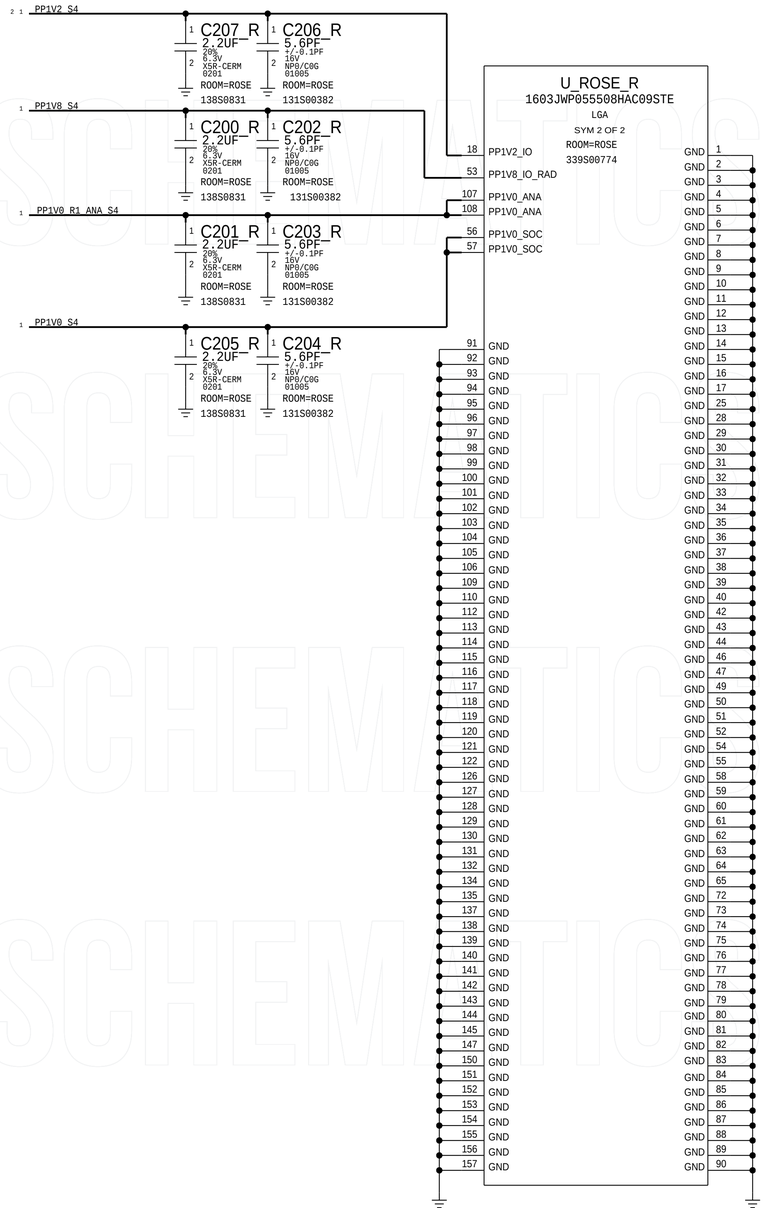
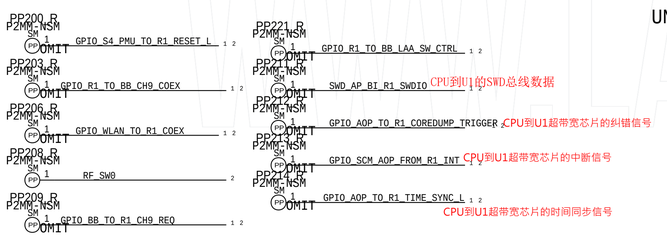
MODULE

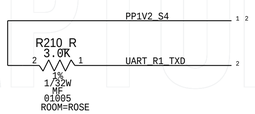


I2C PULL-UPS AT NFC





UNSECURE BOOT BOOTSTRAP PULLUP



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SIZE: D
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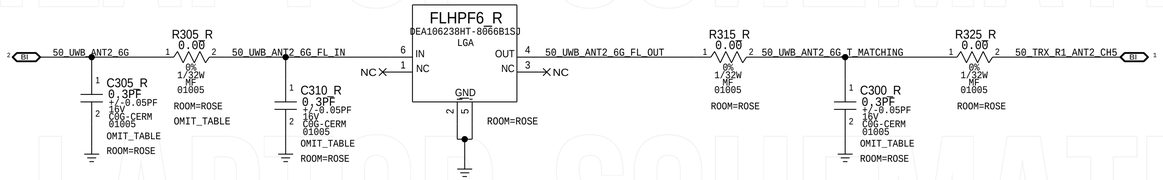
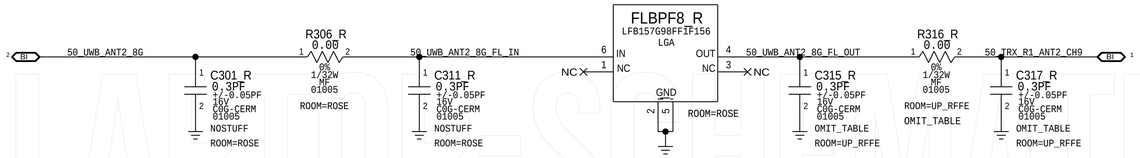
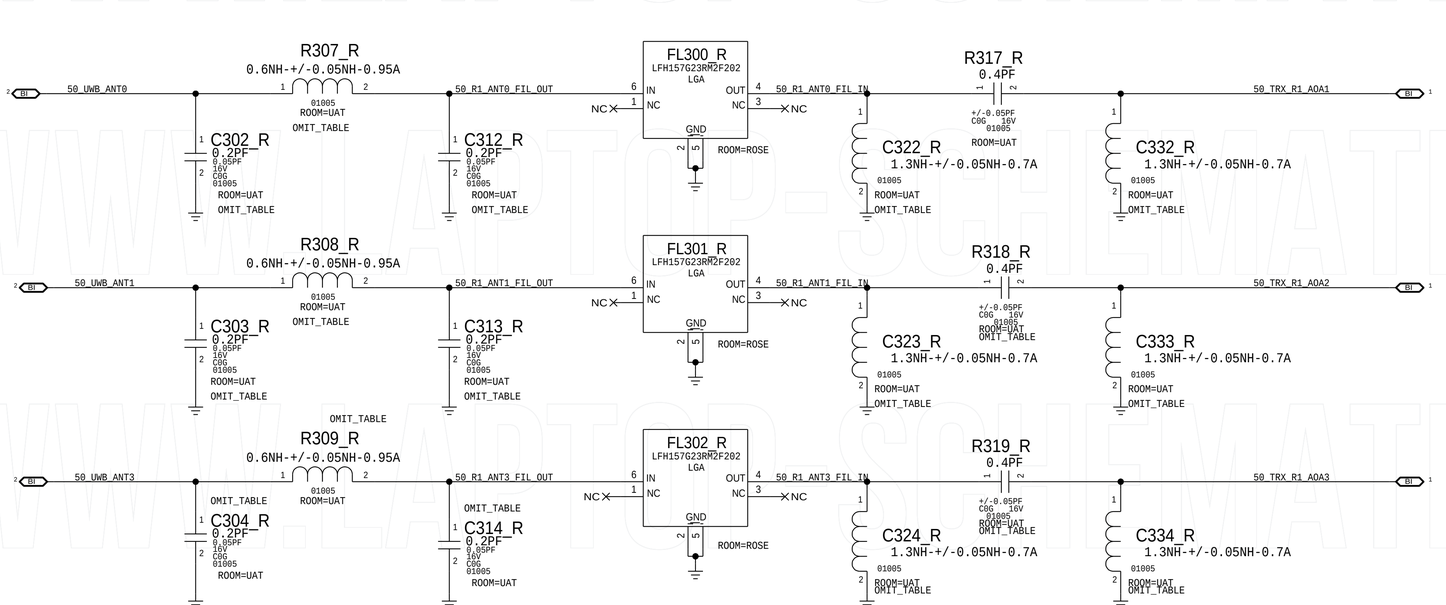
FILTERS/MATCHING AND ANTENNA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0893	1	0.2PF	C305_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0369	1	0.5PF	C305_R	BOARD_ID:D54
131S0369	1	0.5PF	C305_R	BOARD_ID:D52
152S00493	1	0.9NH	R305_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01247	1	1.0NH	R305_R	BOARD_ID:D54
152S01246	1	0.8NH	R305_R	BOARD_ID:D52
131S0893	1	0.2PF	C310_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0369	1	0.5PF	C310_R	BOARD_ID:D54
131S00030	1	0.4PF	C310_R	BOARD_ID:D52
152S00430	1	2.3NH	C300_R	BOARD_ID:D52
131S0893	1	0.2PF	C315_R	BOARD_ID:D54
131S0893	1	0.2PF	C315_R	BOARD_ID:D52
152S01109	1	0.6NH	R316_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01246	1	0.8NH	R316_R	BOARD_ID:D54
152S01109	1	0.6NH	R316_R	BOARD_ID:D52
131S0893	1	0.2PF	C317_R	BOARD_ID:D53G&B0ARD_ID:D53P

Note: C300_R, C315_R are NOSTUFF for D53
NOTE: C300_R IS NOSTUFF FOR D54
Note: C317_R is NOSTUFF for D52/D54







PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0648	1	0.3PF	C302_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0648	1	0.3PF	C302_R	BOARD_ID:D54
131S00030	1	0.4PF	C302_R	BOARD_ID:D52
152S00494	1	0.8NH	R307_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S00493	1	0.9NH	R307_R	BOARD_ID:D54
152S01246	1	0.8NH	R307_R	BOARD_ID:D52
131S0648	1	0.3PF	C312_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0893	1	0.2PF	C312_R	BOARD_ID:D54
131S0648	1	0.3PF	C312_R	BOARD_ID:D52
152S00421	1	1.4NH	C322_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01110	1	1.3NH	C322_R	BOARD_ID:D54
152S00416	1	1.2NH	C322_R	BOARD_ID:D52
152S00421	1	1.4NH	C332_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01110	1	1.3NH	C332_R	BOARD_ID:D54
152S00423	1	1.6NH	C332_R	BOARD_ID:D52
131S0648	1	0.3PF	C303_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0893	1	0.2PF	C303_R	BOARD_ID:D54
131S0648	1	0.3PF	C303_R	BOARD_ID:D52
152S00494	1	0.8NH	R308_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01247	1	1.0NH	R308_R	BOARD_ID:D54
152S00493	1	0.9NH	R308_R	BOARD_ID:D52
131S0648	1	0.3PF	C313_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0893	1	0.2PF	C313_R	BOARD_ID:D54
131S0893	1	0.2PF	C313_R	BOARD_ID:D52
152S00493	1	0.9NH	C323_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01110	1	1.3NH	C323_R	BOARD_ID:D54
152S00416	1	1.2NH	C323_R	BOARD_ID:D52
131S0648	1	0.3PF	R318_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S00030	1	0.4PF	R318_R	BOARD_ID:D54
131S0616	1	0.6PF	R318_R	BOARD_ID:D52
152S00493	1	0.9NH	C333_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S00423	1	1.6NH	C333_R	BOARD_ID:D54
152S00421	1	1.4NH	C333_R	BOARD_ID:D52
131S0648	1	0.3PF	C304_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0893	1	0.2PF	C304_R	BOARD_ID:D54
131S00030	1	0.4PF	C304_R	BOARD_ID:D52
152S01247	1	1.0NH	R309_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S00419	1	1.1NH	R309_R	BOARD_ID:D54
152S00493	1	0.9NH	R309_R	BOARD_ID:D52
131S0648	1	0.3PF	C314_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0893	1	0.2PF	C314_R	BOARD_ID:D54
131S0648	1	0.3PF	C314_R	BOARD_ID:D52
152S00421	1	1.4NH	C324_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01110	1	1.3NH	C324_R	BOARD_ID:D54
152S00419	1	1.1NH	C324_R	BOARD_ID:D52
131S0648	1	0.3PF	R319_R	BOARD_ID:D53G&B0ARD_ID:D53P
131S0617	1	0.9PF	R319_R	BOARD_ID:D54
131S00030	1	0.4PF	R319_R	BOARD_ID:D52
152S00421	1	1.4NH	C334_R	BOARD_ID:D53G&B0ARD_ID:D53P
152S01110	1	1.3NH	C334_R	BOARD_ID:D54
152S00423	1	1.6NH	C334_R	BOARD_ID:D52

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LAST_MODIFICATION=Wed Jul 1 16:52:55 2020

X1804

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103	1	FRONT PAGE		
104	17	QET_DISCRETE_1		08/01/2019
105	20	LB PAD		08/01/2019
106	22	UHB LAT PAD		08/01/2019
107	30	COUPLER LOWER		08/01/2019
108	35	LOWER ANTENNA FEEDS_ANT3		08/01/2019
109	36	LOWER ANTENNA FEEDS_ANT7		08/01/2019
110	38	LOWER ANTENNA FEEDS_ANT9		08/01/2019
111	40	UPPER ANTENNA FEEDS_ANT8		10/02/2019

POWER

PP_VDD_MAIN	VOLTAGE=3.8	IN	2
PP_VDD_BOOST	VOLTAGE=4.5	IN	3 4 5
PP_VDD_RF_1V2	VOLTAGE=1.2	IN	3 4
PP_1V8_LDO6	VOLTAGE=1.8	IN	2 3 4 5

ET/APT IC

PP_APT_L_PA	VOLTAGE=5.5	IN	4
SHIELD_ETDAC_QET1_P		IN	2
SHIELD_ETDAC_QET1_N		IN	2

RF RFFE

SHIELD_RFFE1_SCLK_SDR	IN	5
SHIELD_RFFE1_SDATA_SDR	IO	5
SHIELD_RFFE2_SCLK_SDR	IN	4
SHIELD_RFFE2_SDATA_SDR	IO	4
SHIELD_RFFE3_SCLK_SDR	IN	3 4
SHIELD_RFFE3_SDATA_SDR	IO	3 4
SHIELD_RFFE8_SCLK_SDR	IN	2 3
SHIELD_RFFE8_SDATA_SDR	IO	2 3

LB PAD

50_RX_XCVR_PRX6_LB_A_RX0	OUT	3
50_RX_XCVR_PRX10_LB_PRX_OUT2	OUT	3
50_TX_IN_XCVR_TX1_LB_JB	IN	3
50_TX_IN_XCVR_TX0_LB	IN	3
50_TRX_IN_LMB_PAD_2G_LB_OUT_M	IN	3
50_TRX_LB_PORTB_RX1_M	OUT	3
50_TRX_LB_PORTB_TX_M	IO	3

UHB PA (LAT)

50_RX_XCVR_PRX14_N79_RX_OUT1	OUT	4
50_RX_XCVR_PRX15_N79_RX_OUT2	OUT	4
50_RX_XCVR_PRX16_UHB_RX_OUT1	OUT	4
50_RX_XCVR_PRX17_UHB_RX_OUT2	OUT	4
50_TX_IN_TX2_UHB_PAD_TX_N79_IN	IN	4
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	IN	4
50_UHB_L_CPLR_OUT	IN	4
50_TRX_UHB_PAD_PORTB_TX_M	OUT	4
50_TRX_UHB_PAD_N79_PORTB_TX_M	OUT	4

LAT

50_TRX_HB_PAD_ANT1	IO	5
50_CPLR_L_CPL1_LAT_OUT	IN	5
50_TRX_L5_LNA_IN	OUT	6
50_TRX_ANT1_LB_LMB_MB_HB	IO	5
50_TRX_ANT3_MB_HB_WLAN24	IO	6
50_TRX_ANT7_UHB_N79	IO	7
50_TRX_ANT9_UHB_N79	IO	8
50_TRX_HB_PAD_ANT2_M	IO	5

LAA

50_TRX_WLAN_G_BT_ANT3_NPLXR	IO	6

UAT

50_TRX_ANT8_R1_UHB_N79	IO	9
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	IO	9
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M	IO	9
50_TRX_R1_ANT2_CH5	IO	9
50_TRX_R1_ANT2_CH9	IO	9

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SCH #: 951-11456

FRONT PAGE

DRAWING TITLE	SCH,MLB,TOP,D54
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DISCRETE QET5100 1
LB ONLY

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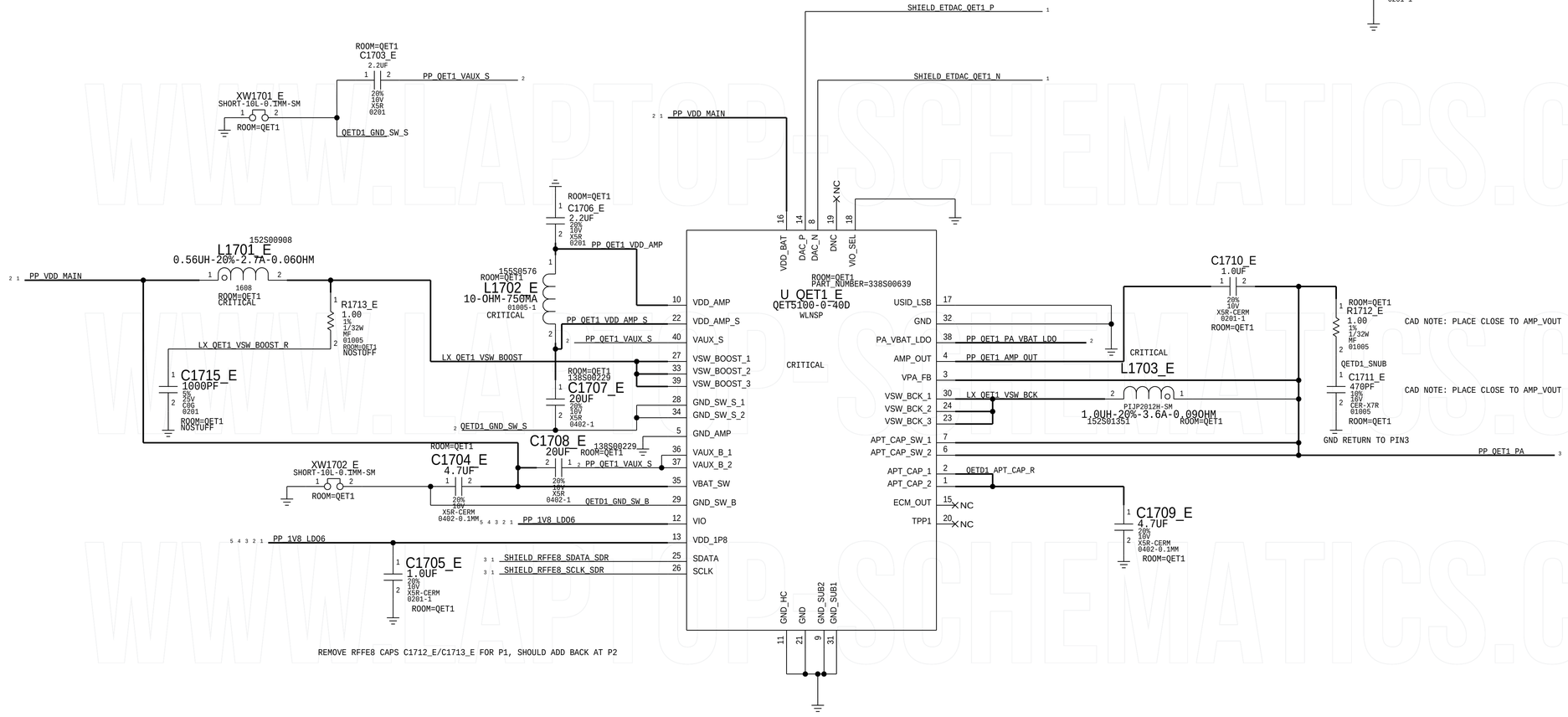

REMOVE RFFE8 CAPS C1712_E/C1713_E FOR P1, SHOULD ADD BACK AT P2

USID=0X4 WHEN UISD PIN IS GND
USID=0X5 WHEN UISD PIN IS HIGH

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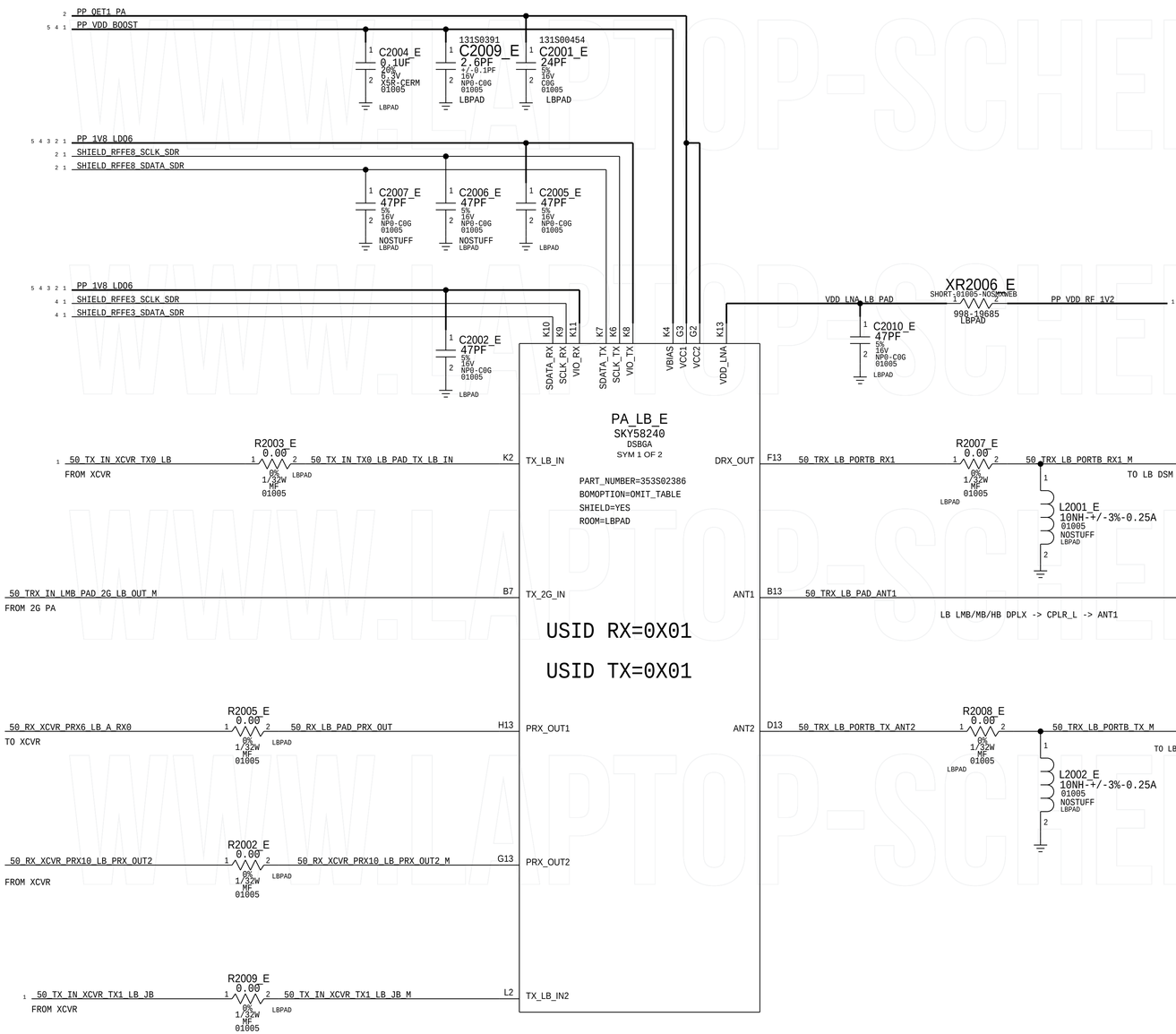
LB PAD

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02386	1	IC,LB PAD,SKY58240,WW,DSMBGA84	PA_LB_E	CRITICAL	RF_SKU:NAJP&RF_SKU:NAMM
353S02387	1	IC,LB PAD,SKY58241,ROW,DSMBGA84	PA_LB_E	CRITICAL	RF_SKU:ROW



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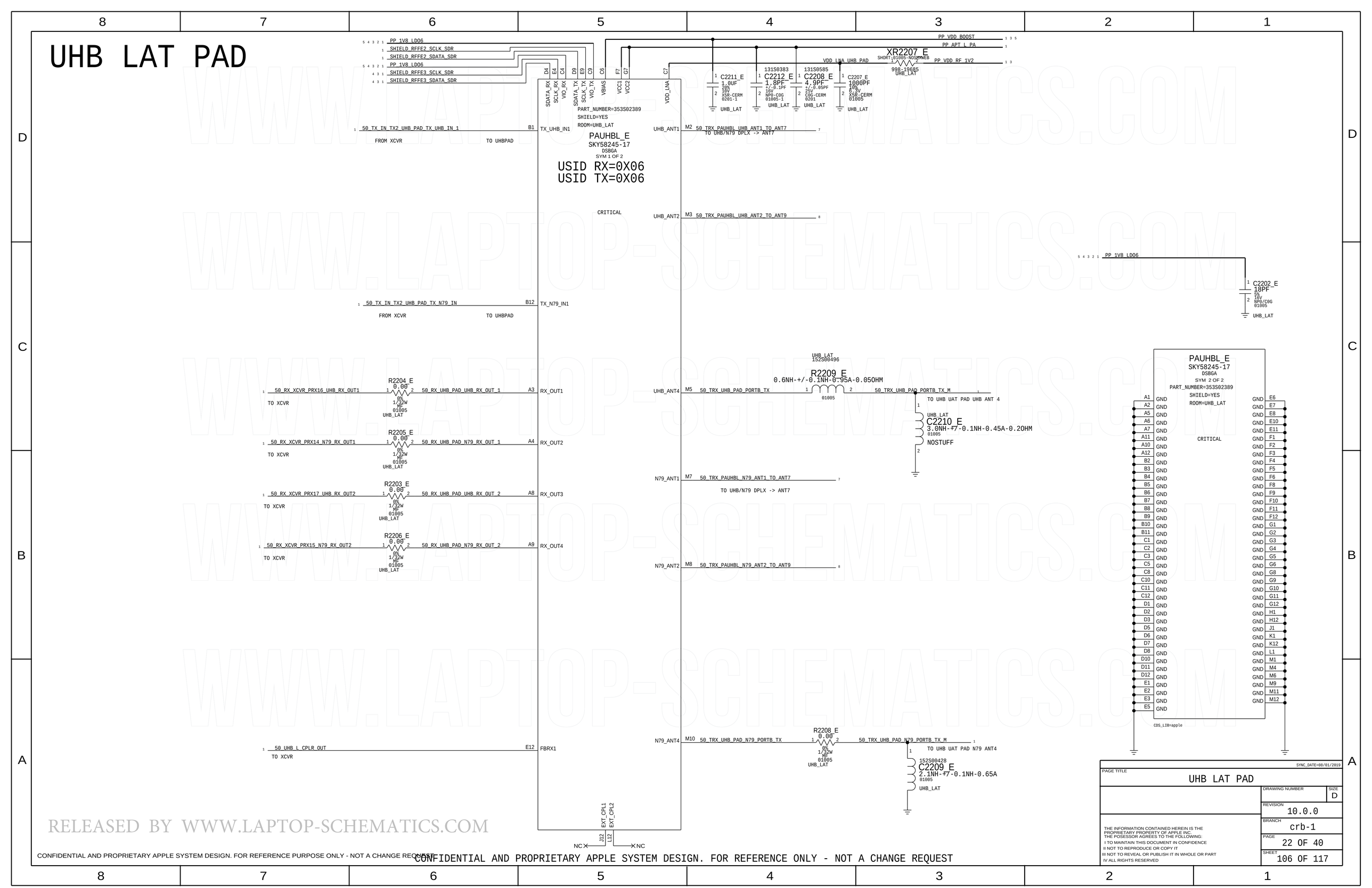
UHB LAT PAD



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LOWER COUPLER

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PP_1V8_LDO6

SHIELD_RFFE1_SCLK_SDR

SHIELD_RFFE1_SDATA_SDR

C3001_E 47PF 5% 16V NP0-C0G 01005 NOSTUFF CPLR_L

C3002_E 47PF 5% 16V NP0-C0G 01005 NOSTUFF CPLR_L

C3003_E 47PF 5% 16V NP0-C0G 01005 CPLR_L

PP_VDD_BOOST

C3004_E 47PF 5% 16V NP0-C0G 01005 CPLR_L

R3004_E 1.0NH-+/-0.1NH-0.9A-0.05OHM 01005 152S00492 ROOM=CPLR_L

50_TRX_LB_PAD_ANT1

LB LMB/MB/HB DPLX -> CPLR_L -> ANT1

50_TRX_LB_PAD_ANT1_M

L3001_E 10NH-+/-3%-0.25A 01005 NOSTUFF CPLR_L

TO LB LMB/MB/HB DPLX -> CPLR_L -> ANT1

R3003_E 1.0NH-+/-0.1NH-0.9A-0.05OHM 01005 152S00492 CPLR_L

50_TRX_HB_PAD_ANT1

50_TRX_HB_PAD_ANT1_M

C3007_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 CPLR_L NOSTUFF

PART_NUMBER=155S00619
ROOM=CPLR_L

DPLX1_E
LFD21788MPAKF237
LGA

LB
MLB_MB_HB
ANT
CRITICAL
GND

50_TRX_DPLX_LB_LMB_MB_HB_ANT1

R3005_E 0.4NH-+/-0.1NH-1.0A-0.030HM 01005 152S00498 ROOM=CPLR_L

50_TRX_CPLR_L_CPL1_IN_LB_LMB_MB_HB

C3008_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 CPLR_L NOSTUFF

C3009_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 CPLR_L NOSTUFF

50_TRX_HB_PAD_ANT2_M

SDATA SCLK VIO VDD USID

CPLR_L_E
MDFEXCGB-137
LGA
SYM 1 OF 2

PART_NUMBER=155S00618
ROOM=CPLR_L

CPL1_IN CRITICAL CPL2_IN

CPL1_ANT

50_TRX_CPLR_L_CPL1_ANT_LB_LMB_MB_HB

R3002_E 1.0NH-+/-0.1NH-0.9A-0.05OHM 01005 152S00492 ROOM=CPLR_L

50_TRX_ANT1_LB_LMB_MB_HB

C3005_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 CPLR_L NOSTUFF

C3006_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 CPLR_L NOSTUFF

TO LOWER ANT1

CPL2_ANT

50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB

TO WIFI/MBHB DPLX --> LOWER ANT3

CPL_OUT

50_CPLR_L_CPL1_LAT_OUT

TO SP3T

USID=0X08

PART_NUMBER=155S00618
ROOM=CPLR_L

CPLR_L_E
MDFEXCGB-137
LGA
SYM 2 OF 2

CRITICAL

GND 4 5 7 8 9 13 14 16 17 18

GND 19 20 21 22 23 24 25 26 27 30

USID=0X08

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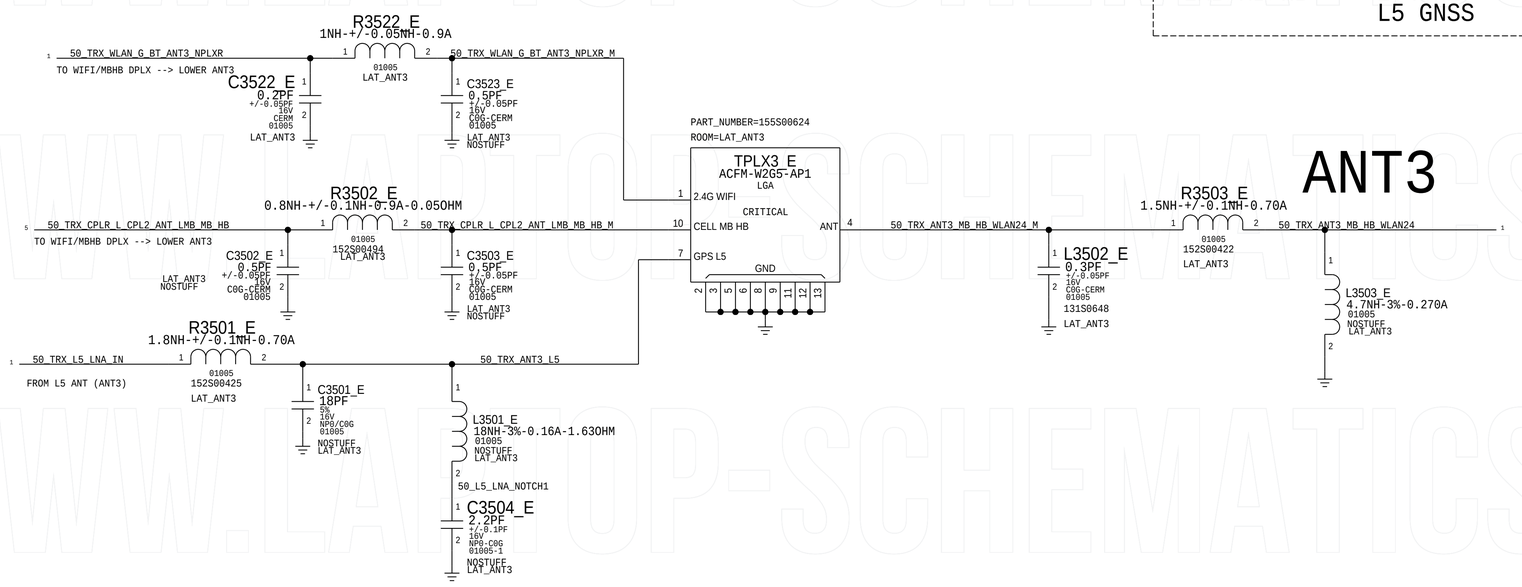
LOWER ANTENNA FEEDS: ANT3

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



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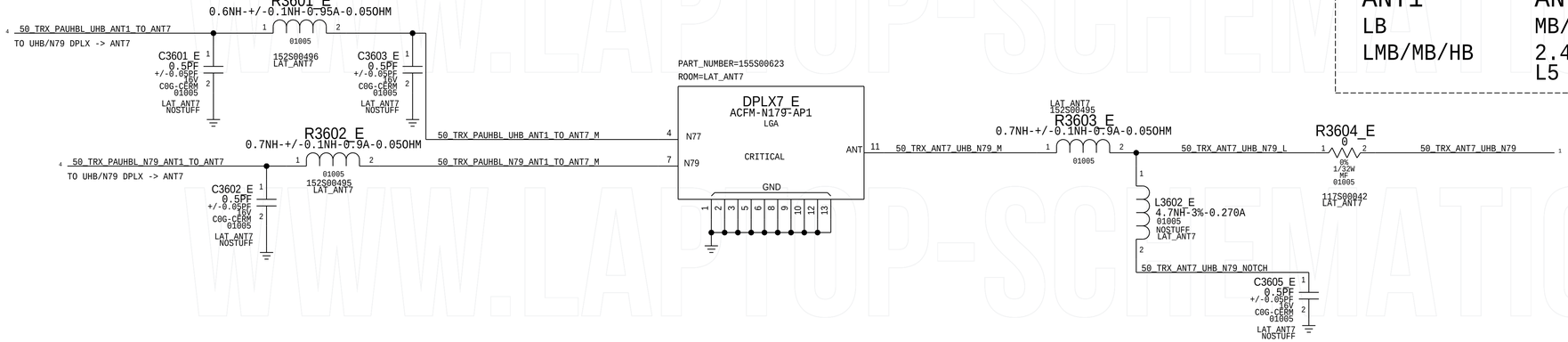
LOWER ANTENNA FEEDS: ANT7

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



ANT7

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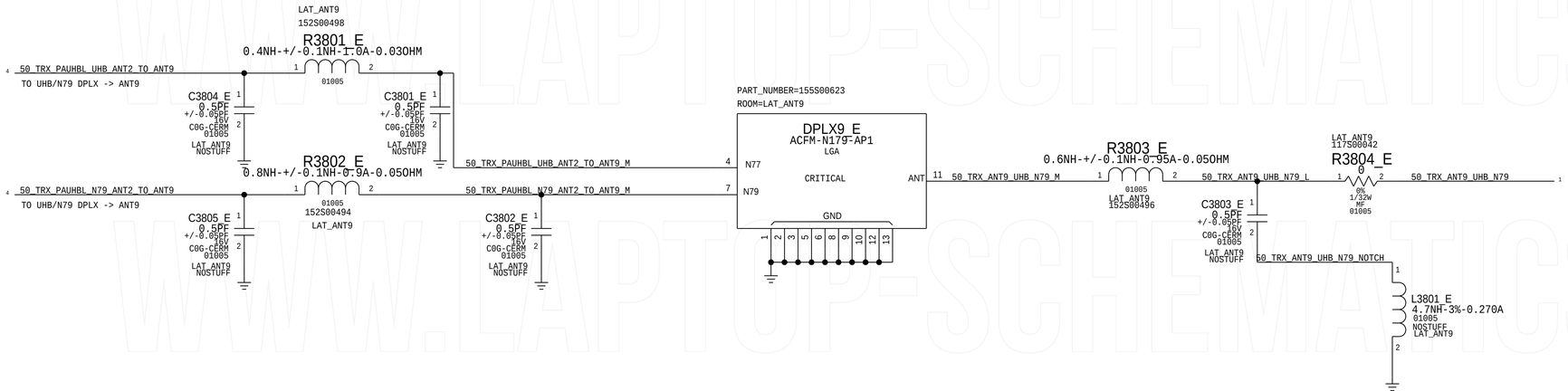
LOWER ANTENNA FEEDS: ANT9

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



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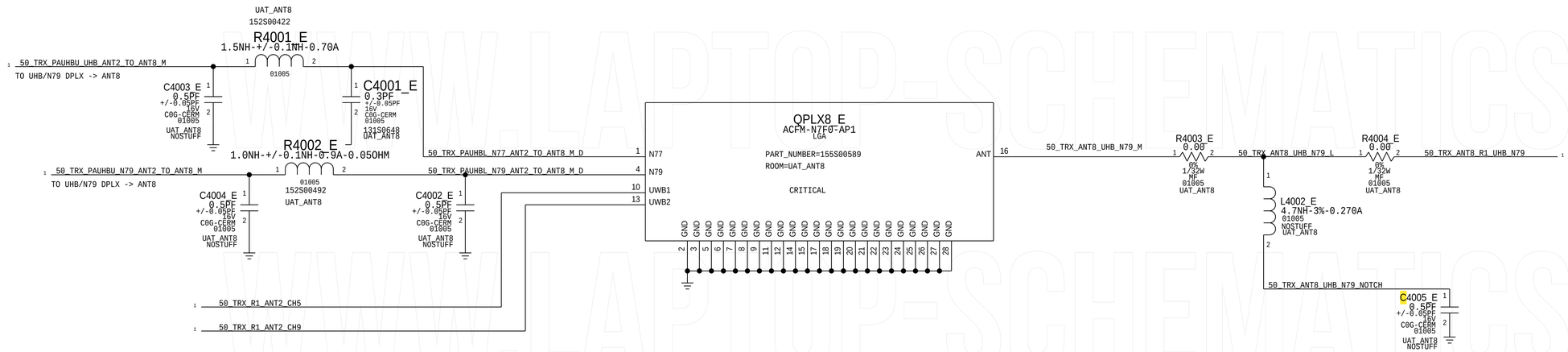
UPPER ANTENNA FEEDS: ANT8

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ L5 GNSS		N79	N79



ANT8

5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

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10	0024125573	ENGINEERING RELEASED	2020-07-01

HIER_NFC D54 TOP

LAST_MODIFICATION=Wed Jul 1 16:52:55 2020

PAGE	CSA	CONTENTS	SYNC	DATE
112	1	NFC: TABLE OF CONTENTS		
113	74	NFC_F		
114	75	NFC_P_CP		

D54 FURY MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00019	2	CAP,CER,C0G,150PF,2%, 50V,0201	C7510_I,C7513_I	?
131S0882	2	CAP,CER,C0G,390PF,2%25V,0201	C7550_I,C7551_I	?
152S01116	2	IND,82NH,2.5%,0.55A,0402	L7500_I,L7501_I	?
131S0825	2	CAP,CER,C0G,560PF,2%,25V,0201	C7515_I,C7543_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7514_I,C7542_I	?
131S0883	2	CAP,CER,C0G,220PF,2%,25V,0201	C7512_I,C7541_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7545_I,C7565_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7546_I,C7566_I	?
131S00026	2	CAP,CER,C0G,820PF,2%,25V,0201	C7547_I,C7567_I	?
131S00026	2	CAP,CER,C0G,820PF,2%,50V,0201	C7548_I,C7568_I	?

2 IN PP_VDD_MAIN VOLTAGE=3.8
2 IN PP1V8_S2 VOLTAGE=1.8
2 IN PP1V2_S2 VOLTAGE=1.2
2 NO PP1V2_NFC_S2

2 IO SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
2 IO SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA_NFC_F_R
IO NFC_P_ANT_POS
IO NFC_P_ANT_NEG
2 IO NFC_F_ANT_POS
2 IO NFC_F_ANT_NEG
2 IN GPIO_AOP_TO_NFC_IRONMAN_EN CPU到NFC的开启信号
IN CLK_BBPMU_TO_NFC_38M
OUT GPIO_NFC_TO_BBPMU_CLK_EN
IN ? NFC_F_TEST_OUT
IN ? GPIO_NFC_F_NFC_P_SYNC2
IN ? GPIO_NFC_F_NFC_P_SYNC1
IN ? NC_NFC_F_DEV_WAKE
2 IO ? 1 GPIO_PMU_NFC_TO_ARCAMP_RESET_L
2 IO ? 1 GPIO_PMU_NFC_TO_ARCAMP_TRIG
2 IO ? 1 I2C_R1_TO_NFC_SCL
2 IO ? 1 I2C_R1_TO_NFC_SDA
2 IO NTC_STOCKHOLM
2 IO ? 1 GPIO_SEQ_PMU_TO_NFC_EN
IN ? IO_TOUCH_TO_MANY_SCAN_ACTIVE

NFC: TABLE OF CONTENTS

DRAWING TITLE: SCH,MLB,TOP,D54
DRAWING NUMBER: 051-05170
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REVISION: 10.0.0
BRANCH: crb-1
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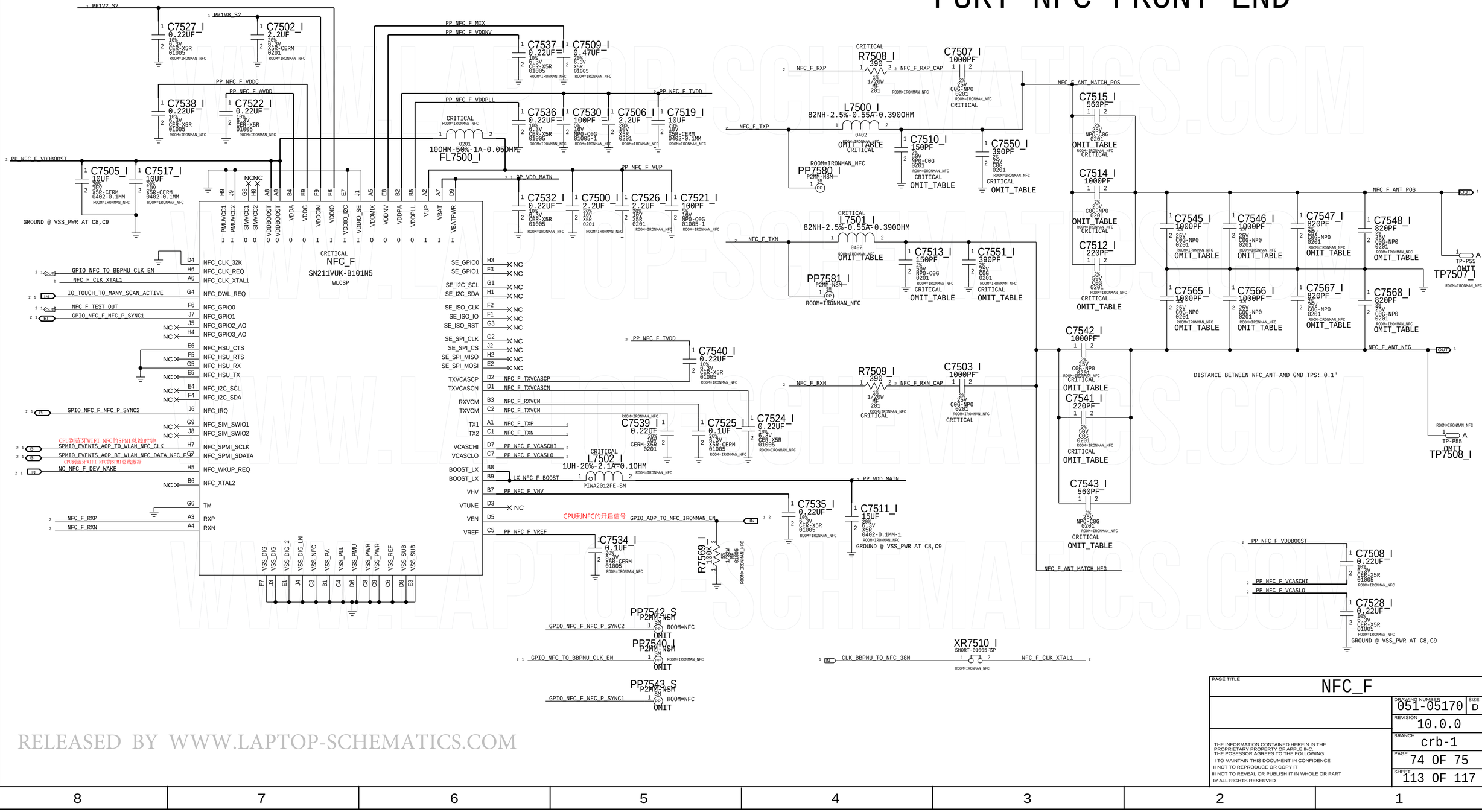
STOCKHOLM

FURY NFC CONTROLLER

FURY NFC FRONT END



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PAGE TITLE	NFC_F
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ROOM=NFC
PP7533_S
P2MM-NSM
SM
PP1V2_NFC_S2 1 PP
OMIT

PP7515_S
P2MM-NSM
SM
电源到振动芯片复位信号
GPIO_PMU_NFC_TO_ARCAMP_RESET_L 1 PP ROOM=NFC
OMIT

PP7516_S
P2MM-NSM
SM
GPIO_PMU_NFC_TO_ARCAMP_TRIG 1 PP ROOM=NFC
OMIT

PP7511_S
P2MM-NSM
SM
I2C_R1_TO_NFC_SCL 1 PP ROOM=NFC
CKPLUS_WAIVE=I2C_PULLUP
OMIT

PP7512_S
P2MM-NSM
SM
I2C_R1_TO_NFC_SDA 1 PP ROOM=NFC
CKPLUS_WAIVE=I2C_PULLUP
OMIT

PP7541_S
P2MM-NSM
SM
NTC_STOCKHOLM 1 PP ROOM=NFC
OMIT

P2MM-NSM
SM
GPIO_SEQ_PMU_TO_NFC_EN 1 PP PP7508_S ROOM=NFC
电源到NFC芯片开启信号
OMIT

NFC_P_ANT_POS
OUT 1
1
TP-P55 A
ROOM=NFC
OMIT
TP7507_S
PLACE CLOSE TO AUT! B2B

NFC_P_ANT_NEG
ROOM=NFC
1
TP-P55 A
OMIT
TP7508_S
PLACE CLOSE TO AUT2 B2B

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PAGE TITLE
NFC_P_CP

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

D54 / HIER_WIFI_TOP

LAST_MODIFICATION=Wed Jul 1 16:52:54 2020

PAGE	CSA	CONTENTS	SYNC	DATE
115	1	TABLE OF CONTENTS		05/08/2018
116	4	5G rFEM (UAT)	D52_WIFI_MASTER_0.17.0	
117	5	5G rFEM (LAT)	D52_WIFI_MASTER_0.17.0	

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	WIFI_MASTER	4,5	0.17.0	S	2019_09_04_14:14:04

WLAN SYMBOL IO PORTS

POWER

- IO PP_VDD_MAIN VOLTAGE=3.8
- IO PP1V8_S4 VOLTAGE=1.8
- IO PP_VDD_MAIN VOLTAGE=3.8
- IO PP1V8_S2 VOLTAGE=1.8

5GHz rFEM (UAT)

- IO 50_WLAN_A_C0_TXRX_FEM_M
- IO 50_LAA_RX_XCVR_DRX10
- IO SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
- IO SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
- IO RFFE_WLAN_TO_UAT_5G_FEM_RST_L
- IO GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
- IO SHIELD_RFFE5_SCLK_SDR
- IO SHIELD_RFFE5_SDATA_SDR
- IO PP_1V8_LDO6
- IO ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
- IO 50_TRX_ANT6_WLAN_A_LAA

5GHz rFEM (LAT)

- IO 50_WLAN_A_C1_TXRX_FEM_M
- IO 50_LAA_RX_XCVR_PRX12
- IO SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
- IO SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA
- IO RFFE_WLAN_TO_LAT_5G_FEM_RST_L
- IO GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN
- IO SHIELD_RFFE3_SCLK_SDR
- IO SHIELD_RFFE3_SDATA_SDR
- IO PP_1V8_LDO6
- IO ANALOG_LAT_5G_FEM_TO_WLAN_PDTS
- IO 50_TRX_ANT5_WLAN_A_LAA

SCHEMATIC APN: 951-10744

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SYNC_DATE=05/08/2018

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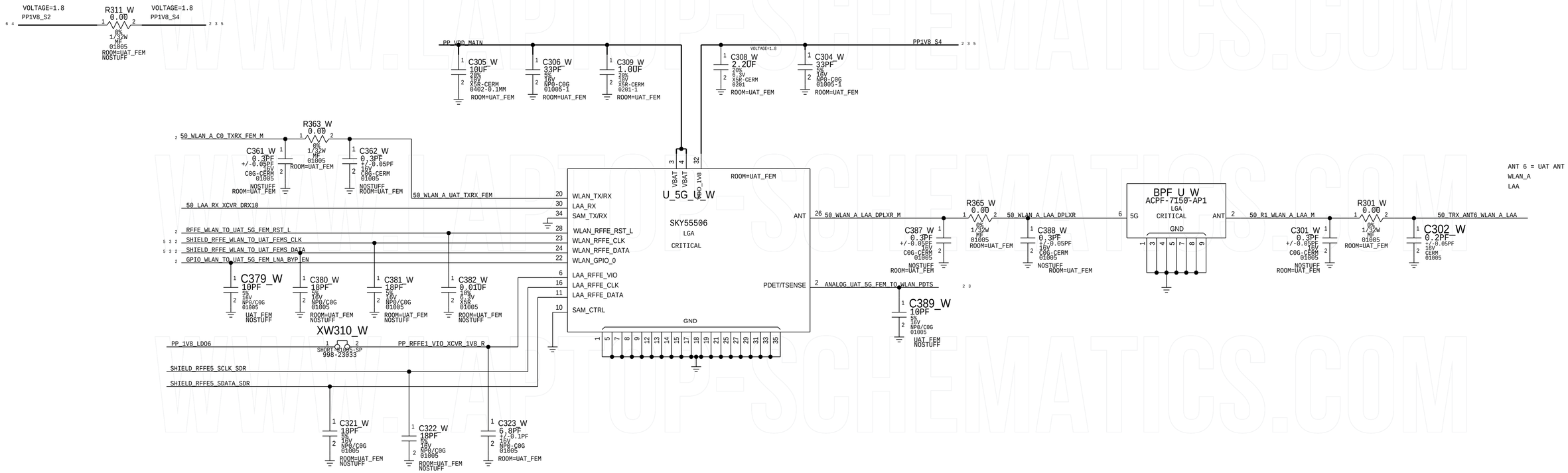
UAT 5GHZ RFEM



OMIT SM_PP209_W P2MM-NSM ROOM=WLAN — ANALOG_UAT_5G_FEM_TO_WLAN_PDTS

OMIT SM_PP218_W P2MM-NSM ROOM=WLAN — SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK

OMIT SM_PP219_W P2MM-NSM ROOM=WLAN — SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA

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PAGE TITLE: 5G rFEM (UAT)

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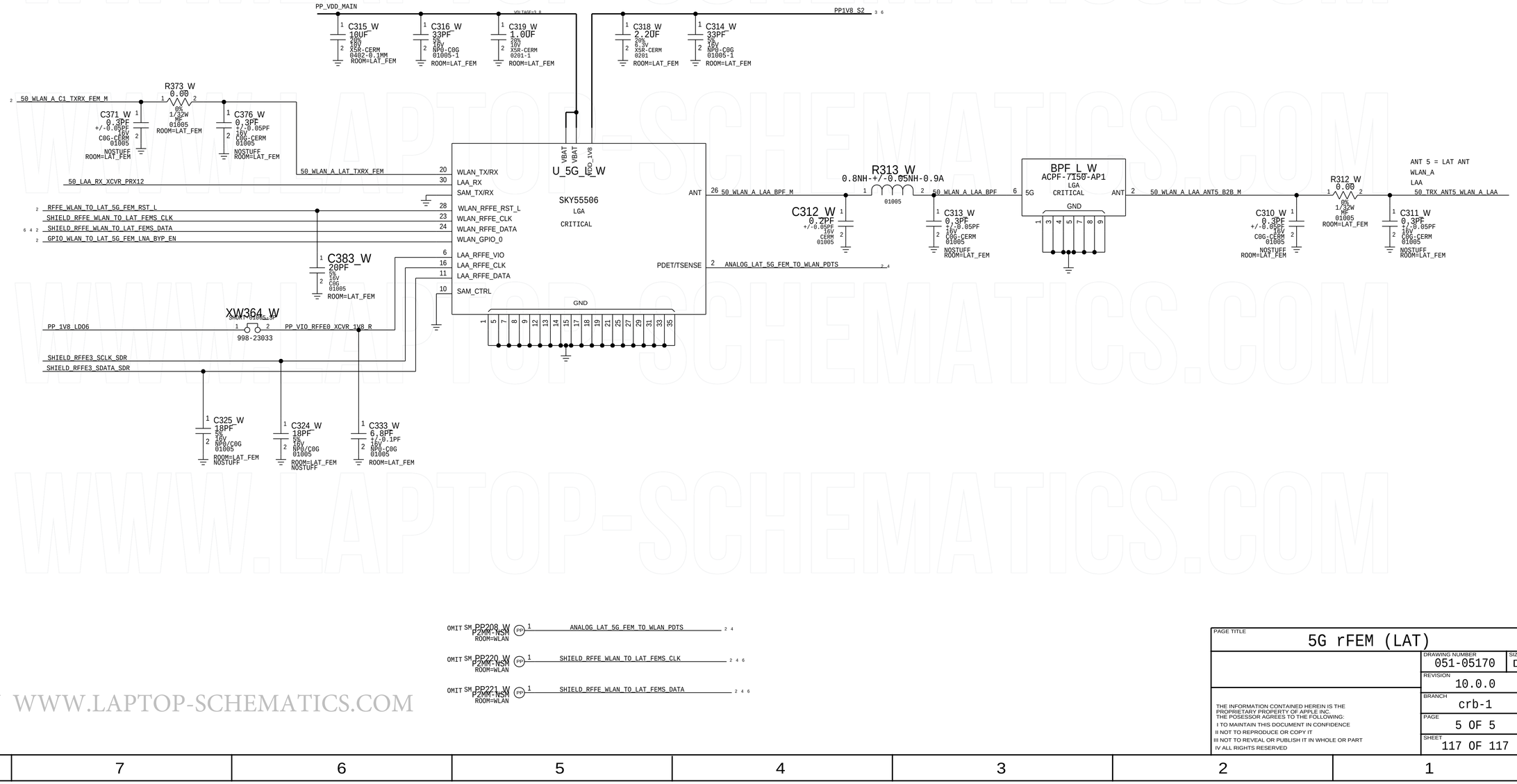
LAT 5GHZ RFEM



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D54 MLB BOT MAV

CRB

LAST_MODIFICATION=Wed Jul 1 15:22:42 2020

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	TABLE OF CONTENTS		
2	2	SYSTEM: BOM Tables	D52_AP_MASTER_0.117.0	11/06/2019
3	3	CONSTRAINTS: 90-Ohm and mmW	D52_AP_MASTER_0.107.0	07/02/2019
4	4	CONSTRAINTS: Power	D52_AP_MASTER_0.107.0	07/02/2019
5	5	CONSTRAINTS: Misc.		09/06/2019
6	6	CONSTRAINTS: 50-Ohm		06/21/2019
7	9	SYSTEM: Mechanical		07/22/2019
8	50	SYS PWR: NTCs (Bottom)	D52_AP_MASTER_tmp	
9	126	TESTING: Test Points		
10	128	TESTING: Probe Points		
11	130	INTERPOSER: Symbol (1/2)		08/15/2019
12	131	INTERPOSER: Symbol (2/2)		08/15/2019
13	132	INTERPOSER: Aliases (1/4)		08/15/2019
14	133	INTERPOSER: Aliases (2/4)		08/15/2019
15	134	INTERPOSER: Aliases (3/4)		08/15/2019
16	135	INTERPOSER: Aliases (4/4)		08/15/2019
17	138	HIERARCHIES: Radio + Primary NFC		
18	139	HIERARCHIES: WiFi		
19	1	FRONT PAGE		
20	2	BOMS AND CONSTRAINTS		08/01/2019
21	4	PMIC: BUCKs		08/01/2019
22	5	PMIC: LDOs		08/01/2019
23	6	PMIC: CLOCKS & CONTROL		08/01/2019
24	7	BB: POWER		08/01/2019
25	8	BB: GND		08/01/2019
26	9	BB: GPIOS & QLINK		08/01/2019
27	11	XCVR POWER_1		08/01/2019
28	12	XCVR POWER_2		08/01/2019
29	13	XCVR DIGITAL & GND		08/01/2019
30	14	XCVR RF		08/01/2019
31	16	QET_DISCRETE_0		08/01/2019
32	18	DCDC2		08/01/2019
33	19	DCDC1		08/01/2019
34	21	HB PAD		08/01/2019
35	23	LMB_2G_PAD		08/01/2019
36	25	LB DSM		08/01/2019
37	26	HB TXDSM		08/01/2019
38	27	UHB DSM		08/01/2019
39	28	MIMO DSM LOWER		08/01/2019
40	29	MIMO DSM UPPER		08/01/2019
41	31	COUPLER UPPER		08/01/2019
42	32	GNSS_L1		08/01/2019
43	33	GNSS_L5		08/01/2019
44	37	LOWER ANTENNA FEEDS_ANT8		08/01/2019
45	39	UPPER ANTENNA FEEDS_ANT4		08/01/2019
46	41	PSIM		08/01/2019
47	43	UAT SAWTOOTH		08/01/2019
48	44	LAT SAWTOOTH		08/01/2019
49	46	DEBUG & TEST POINTS		08/01/2019
50	57	MLB_ADJUSTABLES		08/01/2019
51	58	MMW		08/01/2019
52	59	TANGIER SIP		08/01/2019
53	60	BG1 ARRAY		08/01/2019
54	1	NFC: TABLE OF CONTENTS		
55	2	NFC_P		
56	3	NFC_P_FE		
57	1	Table of Contents_D52		
58	2	THELONIOUS	D52_WIFI_MASTER_0.21.0	
59	7	2G4 rFEM (UAT)	D52_WIFI_MASTER_0.17.0	
60	8	2G4 rFEM (LAT)	D52_WIFI_MASTER_0.17.0	

APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05263	1	SCH,MLB,BOT,MAV,D54	SCH	CRITICAL	?
820-01971	1	PCB,MLB,BOT,MAV,D54	PCB	CRITICAL	?

Sub-designs

Hierarchies

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/ SOFT	SYNC_DATE/TIME	FORCE SUBDESIGN
D54	HIER_RADIO_MAV_BOT	3.61.0	S	2020_06_26_15:43:07	N
D54	HIER_NFC_BOT	0.23.0	S	2020_06_26_12:24:47	N
D54	HIER_WIFI_BOT	0.12.0	S	2020_06_26_12:33:04	N

Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	AP_MASTER	50	tmp	S	2020_07_01_14:57:41

Packaging Options

PACK_OPTIONS TO INCLUDE IN NETLIST
D54

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SYNC_MASTER=doe_mlb_panini SYNC_DATE=05/15/2018

DRAWING TITLE: SCH,MLB,BOT,MAV,D54

DRAWING NUMBER: 051-05263 SIZE: D

REVISION: 9.0.0

BRANCH: crb-1

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Global Capacitors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1103	138S0719	?	ALL	CAP,X5R,4.7UF,20%,10V,0402,TAIYO

CRITICAL PART#	COMMENT
138S0719	CAP,X5R,4.7UF,20%,10V,0402,MURATA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00133	138S00128	?	ALL	CAP,X5R,0.47UF,20%,6.3V,01005,MURATA
138S00269	138S00128	?	ALL	CAP,X5R,0.47UF,20%,6.3V,01005,TAIYO
138S00269	138S00133	?	ALL	CAP,X5R,0.47UF,20%,6.3V,01005,TAIYO

CRITICAL PART#	COMMENT
138S00128	CAP,X5R,0.47UF,20%,6.3V,01005,KYOCERA
138S00133	CAP,X5R,0.47UF,20%,6.3V,01005,MURATA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	?	ALL	CAP,X5R,0.1UF,20%,6.3V,01005

CRITICAL PART#	COMMENT
132S0316	CAP,X5R,0.1UF,20%,6.3V,01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	ALL	CAP,X5R,15UF,20%,6.3V,0402,KYOCERA

CRITICAL PART#	COMMENT
138S00003	CAP,X5R,15UF,20%,6.3V,0402,MURATA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA

CRITICAL PART#	COMMENT
138S0706	CAP,X5R,1UF,20%,10V,0201

22uF, 0402 3T (WiFi)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00024	138S0986	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
138S0986	CAP,CER,3-TERM,7.5UF,20%,4V,0402

33PF, 0201 (NFC)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
131S00377	131S0823	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
131S0823	CAP,CER,NP0/C0G,33PF,+/-2%,25V,0201

MAV20 PDN Single-source

0.22uF, 01005

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Kyocera

CRITICAL PART#	COMMENT
132S00014	01005,0.22uF, 6.3V

(C706,E-C720,E-C723,E-C725,E-C727,S,C730,E-C731,E-C734,E-C736,E-C742,E-C744,E-C749,E-C751,S,C754,E-C760,E-C766,S,C767,E-C770,E-C772,E-C774,E-C776,E-C778,E-C780,E)
(C706,E-C720,E-C723,E-C725,E-C727,S,C730,E-C731,E,C734,E,C736,E-C742,E-C744,E,C749,E-C751,S,C754,E-C760,E-C766,S,C767,E,C770,E-C772,E,C774,E-C776,E,C778,E-C780,E)

2.2uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	[SEE BELOW]	CAP,CER,X5R,2.2UF,20%,6.3V,0201

CRITICAL PART#	COMMENT
138S0831	CAP,CER,X5R,2.2UF,20%,6.3V,0201

(C701,E,C702,E,C704,E,C721,E,C722,E,C726,E,C728,E,C729,E,C732,E,C733,E,C735,E,C743,E,C745,E,C748,E,C747,E,C748,E,C752,E,C768,E,C769,E,C773,E,C777,E,C789,E)

4uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

CRITICAL PART#	COMMENT
138S00071	CAP,X5R,4UF,20%,6.3V,0201,MURATA

(C435,E,C511,E-C518,E,C522,E,C524,E-C526,E,C702,E,C768,E,C769,E,C777,E,C787,E,C788,E,C1135,E-C1142,E,C1226,E,C1227,E,C5801,E-C5803,E,C5823,E,C5827,E,C5828,E)
(C435,E,C511,E-C518,E,C522,E,C524,E-C526,E,C702,E,C768,E,C769,E,C777,E,C787,E,C788,E,C1135,E-C1142,E,C1226,E,C1227,E,C5801,E-C5803,E,C5823,E,C5827,E,C5828,E)

22uF, 0201

All RefDes in ( ) are single-sourced from Samsung

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	?	ALL	CAP,X5R,22UF,0402,20%,4V,MURATA
138S00143	138S00279	?	[SEE BELOW]	CAP,X5R,22UF,0402,20%,4V,KYOCERA

CRITICAL PART#	COMMENT
138S00279	CAP,X5R,22UF,20%,4V,0402,SAMSUNG

(C449,E,C429,E-C434,E,C523,E)

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-08664	MVW3	CRITICAL	EEEE:08664
825-7691	1	EEEE FOR 639-10114	NY9L	CRITICAL	EEEE:10114
825-7691	1	EEEE FOR 639-10759	PP6P	CRITICAL	EEEE:10759

Global Inductors/Diodes

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00437	155S00402	?	ALL	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00400	155S00200	?	ALL	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
371S00062	371S00101	?	ALL	DIODE,SCHOTTKY,30V,250MW,0201
377S00061	377S0183	?	ALL	TVS,BIDIR,5.0V,0201
377S00173	377S0183	?	ALL	TVS,BIDIR,5.0V,0201
377S0168	377S00129	?	ALL	SUPRESS,TRANS,6.8V,100PF,AMOTECH,01005
152S00872	152S00918	?	ALL	TDK,IND,MLD,0.47UH,5.6A,20MO,2016
152S00847	152S00918	?	ALL	CYNTEC,IND,MLD,0.47UH,5.6A,20MO,2016

CRITICAL PART#	COMMENT
155S00402	FERR BD,33OHM,25%,1.5A,55MOHM DCR,0201
155S00200	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
371S00101	DIODE,SCHOTTKY,30V,100MA,250MW,0201
377S0183	TVS,BIDIR,5.0V,0201
CRITICAL PART#	COMMENT
377S00129	SUPRESS,TRANS,6.8V,100PF,01005

Thermistor

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0245	107S0244	?	ALL	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

CRITICAL PART#	COMMENT
107S0244	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

Multi-Vendor Criticals

CRITICAL PART#	COMMENT
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
197S0446	XTAL,24MHZ,30PPM,9.5PF,60 OHM MAX,1612
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
132S0664	CAP,CER,0.047UF,10%,25V,X5R,0201
132S0663	CAP,CER,X5R,1UF,10%,25V,0402
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S0396	CAP,CER,X5R,1000PF,10%,16V,01005

CRITICAL PART#	COMMENT
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S00093	CAP,X5R,0.022UF,20%,6.3V,01005
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S00008	CAP,CER,0.1UF,10%,50V,X7R,0402
131S0883	CAP,CER,NP0/C0G,220PF,2%,50V,0201
131S0804	CAP,CER,27PF,5%,C0G,25V,0201
131S0307	CAP,CER,NP0/C0G,100PF,5%,16V,01005
131S0225	CAP,CER,NP0/C0G,15PF,5%,16V,01005
131S0223	CAP,CER,NP0/C0G,27PF,5%,16V,01005
131S0220	CAP,CER,NP0/C0G,12PF,5%,16V,01005
131S0216	CAP,CER,NP0/C0G,47PF,5%,16V,01005

CRITICAL PART#	COMMENT
155S00341	FERR BD,240 OHM,25%,200MA,0.9 DCR,01005
131S00170	CAP,CER,C0G,220PF,5%,25V,01005
131S0215	CAP,CER,NP0/C0G,22PF,5%,16V,01005
131S0643	CAP,CER,NP0/C0G,56PF,5%,25V,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
117S0055	RES,MF,1/20W,2M OHM,5,0201,SMD
132S0296	CAP,CER,X5R,10000PF,10%,6.3V,01005
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
131S00053	CAP,CER,C0G,220PF,5%,10V,01005
131S00323	CAP,CER,NP0/C0G,56PF,5%,25V,01005
131S00303	CAP,CER,NP0/C0G,100PF,5%,16V,01005
131S00353	CAP,CER,NP0/C0G,10PF,5%,16V,01005

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SYSTEM: BOM Tables

DRAWING NUMBER 051-05263 | SIZE D

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90-ohm Diff Pair Constraints

Electrical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
QLINK (RF)	E_QLINK_SUB6	E	DIFF_PAIR_QLINK-SUB6	DP:DP_85_SUB6_QLINK_*	Y
	E_QLINK_MMW	E	DIFF_PAIR_QLINK-MMW	DP:DP_85_MMW_QLINK_*	Y
PCIe	E_PCIE_BB	E	DIFF_PAIR	DP:DP_90_PCIE_GP2_AP_*_BB_*	Y
	E_PCIE_WLAN	E	DIFF_PAIR	DP:DP_90_PCIE_GP1_AP_*_WLAN_*	Y
	E_USB_BB	E	DIFF_PAIR	DP:DP_90_USB_BB	Y

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
85-ohm	85_QLINK_SUB6	P	A_85_OHM_DIFF	DP:DP_85_SUB6_QLINK_*	Y
	85_QLINK_MMW	P	A_85_OHM_DIFF	DP:DP_85_MMW_QLINK_*	Y
	90_PCIE_BB	P	A_90_OHM_DIFF	DP:DP_90_PCIE_GP2_AP_*_BB_*	Y
90-ohm	90_PCIE_WLAN	P	A_90_OHM_DIFF	DP:DP_90_PCIE_GP1_AP_*_WLAN_*	Y
	90_USB_BB	P	A_90_OHM_DIFF	DP:DP_90_USB_BB	Y

Spacing

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
85-ohm	85_QLINK_SUB6	S	A_DIELECTRIC_3X	=	Y
	85_QLINK_MMW	S	A_DIELECTRIC_3X	=	Y
	90_PCIE_BB	S	A_DIELECTRIC_3X	=	Y
90-ohm	90_PCIE_WLAN	S	A_DIELECTRIC_3X	=	Y
	90_USB_BB	S	A_DIELECTRIC_3X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
90_PCIE_BB	GND	A_DIELECTRIC_2X
90_PCIE_WLAN	GND	A_DIELECTRIC_2X

Custom mmW Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
mmW IF	50_MMW_IF	P	50_OHM_MMW_IF_SE	50_MMW_*IFH*, 50_MMW_*IFV*	Y
mmW RF	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S1H_HPOL,50_MMW_SMR525_S1L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S2H_HPOL,50_MMW_SMR525_S2L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S5H_HPOL,50_MMW_SMR525_S5L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S6H_HPOL,50_MMW_SMR525_S6L_HPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S7H_HPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S7L_HPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S8H_HPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S8L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S9H_VPOL,50_MMW_SMR525_S9L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S10H_VPOL,50_MMW_SMR525_S10L_VPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S11H_VPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S11L_VPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S12H_VPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S12L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S13H_VPOL,50_MMW_SMR525_S13L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S14H_VPOL,50_MMW_SMR525_S14L_VPOL	Y

Spacing

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
mmW IF	50_MMW_IF	S	DIELECTRIC_4XV_50_MMW_IF_SE	=	Y
mmW RF	50_MMW_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y
	50_MMW_SMYRNA_HB_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y
	50_MMW_SMYRNA_LB_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_MMW_IF	GND	DIELECTRIC_2X_50_MMW_IF_SE
50_MMW_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SE
50_MMW_SMYRNA_HB_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SMYRNA_HB_SE
50_MMW_SMYRNA_LB_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SMYRNA_LB_SE

Spacing CSet Definitions

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_{N}X Calculates dielectric distance from stackup, shortest distance is used unless 'L' defined	EXAMPLE: 1,2.5,3,8; ea. 1mil 1.5,2,2.5,3,8
A_DIELECTRIC_{N}XD XV,XVL,X Calculates dielectric distance from Hybrid Table and stackup, shortest distance is used unless 'L' defined	EXAMPLE: 2 mils, default is used unless 'L' defined PLEASE USE HYBRID TABLE
A_DIELECTRIC_{N}XIN_{N}XOUT Calculates distance from stackup from defined shortest distance is used unless 'L' is defined	EXAMPLE: 1_4.5L_3L ?

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CONSTRAINTS: 90-Ohm and mmW

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AP Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LX/CX Nodes	PWR_SHAPE	P	PWR_SHAPE	LX*	Y
System-Wide	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_BOOST	Y
	PWR_200UM	P	PWR_200UM	PP1V8_S2	?
	PWR_200UM	P	PWR_200UM	PP1V8_S4	Y
	PWR_100UM	P	PWR_100UM	PP1V2_S2	Y
	PWR_100UM	P	PWR_100UM	PP1V2_S4	Y
	PWR_100UM	P	PWR_100UM	PP3V0_S2*	Y
	PWR_100UM	P	PWR_100UM	PP_VBUS1_E75	Y

RF Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
WiFi/Misc.	PWR_100UM	P	PWR_100UM	PP_VDD_BTPA3V3	Y
	PWR_100UM	P	PWR_100UM	PP1V8_LAT_2G_FEM	Y
	PWR_100UM	P	PWR_100UM	PP3V0_DEBUG	Y
SMPS 1/6	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS1_6	Y
SMPS 2	PWR_SHAPE	P	PWR_SHAPE	PP_1V22_SMPS2	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_1V24_SMPS2_SNS	Y
SMPS 3	PWR_SHAPE	P	PWR_SHAPE	PP_0V82_SMPS3	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V82_SMPS3_SNS	Y
SMPS 4	PWR_SHAPE	P	PWR_SHAPE	PP_1V9_SMPS4	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_1V9_SMPS4_SNS	Y
SMPS 5	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS5	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V75_SMPS5_SNS	Y
SMPS 7	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS7	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V75_SMPS7_SNS	Y
LDO1	PWR_SHAPE	P	PWR_SHAPE	PP_1V2_LDO1	Y
	PWR_500UM	P	PWR_500UM	PP_1V2_LDO1_SDR_VDDAM_RP, PP_1V2_LDO1_SDR_VDDAM_RX	Y
	PWR_300UM	P	PWR_300UM	PP_LDO1_SDR_VDDAM_BBRX_BOT_215	Y
	PWR_200UM	P	PWR_200UM	PP_1V2_LDO1_SDR_VDDAM_TX	Y
	PWR_200UM	P	PWR_200UM	PP_LDO1_SDR_VDDAM_RX0_171, PP_LDO1_SDR_VDDAM_RX5_138	Y
	PWR_100UM	P	PWR_100UM	PP_1V2_LDO1_SDR_VDDAM_TP, PP_LDO1_SDR_VDDAM_BBRX_TOP_97	Y
	PWR_80UM	P	PWR_80UM	PP_LDO1_SDR_VDDAM_RP*_57, PP_LDO1_SDR_VDDAM_TX*_40	Y
	PWR_50UM	P	PWR_50UM	PP_LDO1_SDR_VDDAM_*P*_30	Y
LDO2	PWR_500UM	P	PWR_500UM	PP_1V1_LDO2	Y
LDO3	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO3	Y
	PWR_500UM	P	PWR_500UM	PP_0V8_LDO3_SDR_VDDAL_DIG	Y
	PWR_500UM	P	PWR_500UM	PP_0V8_LDO3_SDR_VDDAL_RP*, PP_0V8_LDO3_SDR_VDDAL_RX_*	Y
	PWR_300UM	P	PWR_300UM	PP_LDO3_SDR_VDDAL_DIG1_171	Y
	PWR_200UM	P	PWR_200UM	PP_LDO3_SDR_VDDAL_DIG2_124	Y
	PWR_100UM	P	PWR_100UM	PP_0V8_LDO3_SDR_VDDAL_RXLO*	Y
	PWR_100UM	P	PWR_100UM	PP_0V8_LDO3_SDR_VDDAL_TP, PP_0V8_LDO3_SDR_VDDAL_TX	Y
	PWR_100UM	P	PWR_100UM	PP_LDO3_SDR_VDDAL_RP*_57	Y
	PWR_100UM	P	PWR_100UM	PP_LDO3_SDR_VDDAL_RX0_67, PP_LDO3_SDR_VDDAL_RX6_90	Y
	PWR_80UM	P	PWR_80UM	PP_0V8_LDO3_SDR_VDDAL_DIG_RP*	Y
	PWR_50UM	P	PWR_50UM	PP_0V8_LDO3_SDR_VDDAL_DIG_TP	Y
	PWR_50UM	P	PWR_50UM	PP_0V8_LDO3_SDR_VDDAL_ICON	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_DIG_*	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_FBRX_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_GNSS_40	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_ICON*	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_RX*_22	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_RXLO*_27	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_TP*_30	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_TX*_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_XO_18	Y
LDO4	PWR_SHAPE	P	PWR_SHAPE	PP_0V875_LDO4	Y
	PWR_200UM	P	PWR_200UM	PP_LDO4_SMR_*, PP_LDO4_VDD_*	Y
LDO5	PWR_300UM	P	PWR_300UM	PP_1V8_LDO5	Y
	PWR_200UM	P	PWR_200UM	PP_LDO5_SMR_VDDAH_2_*	Y
	PWR_50UM	P	PWR_50UM	PP_LDO5_SMR_VDDAH_1_*, PP_LDO5_SMR_VDDAH_3_*, PP_LDO5_SMR_VDDAH_4_*	Y
LDO6	PWR_300UM	P	PWR_300UM	PP_1V8_LDO6	Y
	PWR_50UM	P	PWR_50UM	PP_LDO6_SMR_VDD_PX_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO6_SDR_VDD_PX_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO6_SDR_VDD_PXM_20	Y
LDO7	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO7	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_LDO7_SMR_CX_*_300	Y
LDO8	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO8	Y
LDO9	PWR_500UM	P	PWR_500UM	PP_0V8_LDO9	Y
	PWR_200UM	P	PWR_200UM	PP_LDO9_SMR_VDDAL_3_140	Y
	PWR_100UM	P	PWR_100UM	PP_LDO9_SMR_VDDAL_4_90	Y
	PWR_80UM	P	PWR_80UM	PP_LDO9_SMR_VDDAL_1_50	Y
	PWR_50UM	P	PWR_50UM	PP_LDO9_SMR_VDDAL_*_10	Y
LDO10	PWR_100UM	P	PWR_100UM	PP_3V1_LDO10	Y
LDO11	PWR_100UM	P	PWR_100UM	PP_UIM1_LDO11	Y
LDO12	PWR_SHAPE	P	PWR_SHAPE	PP_1V2_LDO12	Y
	PWR_300UM	P	PWR_300UM	PP_LDO12_SMR_VDDAM_4_240	Y
	PWR_200UM	P	PWR_200UM	PP_LDO12_SMR_VDDAM_2_120	Y
	PWR_100UM	P	PWR_100UM	PP_LDO12_SMR_VDDAM_*_70	Y
	PWR_100UM	P	PWR_100UM	PP_LDO12_SMR_VDDAM_5_240	Y
LDO13	PWR_100UM	P	PWR_100UM	PP_UIM2_LDO13	Y
LDO14	PWR_500UM	P	PWR_500UM	PP_0V6_LDO14	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V6_LDO14_SNS	Y
LDO15	PWR_100UM	P	PWR_100UM	PP_1V2_LDO15	Y
	PWR_50UM	P	PWR_50UM	PP_LDO15_SDR_VDD_PX_20	Y
LDO16	PWR_750UM	P	PWR_750UM	PP_1V7_LDO16	Y
	PWR_200UM	P	PWR_200UM	PP_1V7_LDO16_SDR_VDDAH_RP	Y
	PWR_200UM	P	PWR_200UM	PP_1V7_LDO16_SDR_VDDAH_TX	Y
	PWR_100UM	P	PWR_100UM	PP_1V7_LDO16_SDR_VDDAH_TP	Y
	PWR_80UM	P	PWR_80UM	PP_1V7_LDO16_SDR_VDDAH_TXDAC	Y
	PWR_50UM	P	PWR_50UM	PP_LDO16_SDR_VDDAH_*	Y
BB PMK	PWR_80UM	P	PWR_80UM	PP_BBPMK_VREG_RF	Y
	PWR_80UM	P	PWR_80UM	PP_BBPMK_VREG_XO	Y
	PWR_80UM	P	PWR_80UM	PP_PMK_REF_BYP	Y

RF Physical (continued)

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
QET0	PWR_500UM	P	PWR_500UM	PP_QET0_PA	Y
	PWR_500UM	P	PWR_500UM	PP_QET0_2G_PA	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_PA_VBAT_LDO	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_AMP_OUT	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_VAUX_S	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_VDD_AMP	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_VDD_AMP_S	Y
APT (Lower)	PWR_500UM	P	PWR_500UM	PP_APT_L_PA	Y
	PWR_200UM	P	PWR_200UM	PP_APT_L_N*A*	Y
	PWR_200UM	P	PWR_200UM	PP_APT_L_LXA	Y
APT (Upper)	PWR_500UM	P	PWR_500UM	PP_APT_U_PA	Y
	PWR_200UM	P	PWR_200UM	PP_APT_U_N*A*	Y
	PWR_200UM	P	PWR_200UM	PP_APT_U_LXA	Y
PAD/DSM VDDs	PWR_50UM	P	PWR_50UM	VDD_HB_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_LB_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_LNA_HB_PAD	Y
	PWR_50UM	P	PWR_50UM	VDD_MIMO1_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_MIMO2_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_UHB_DSM	Y
Misc Radio	PWR_100UM	P	PWR_100UM	PP_PMX_VIO_OUT	Y
	PWR_300UM	P	PWR_300UM	PP_VDD_RF_1V2	Y
	PWR_50UM	P	PWR_50UM	PP_VDD_SIM_DETECT	Y
	PWR_80UM	P	PWR_80UM	PP_VIO_RFFE_1V8	Y
	PWR_100UM	P	PWR_100UM	PP_VREF_SDX	Y
	PWR_80UM	P	PWR_80UM	PP1V8_S4_UAT_BRIDGE_VIO	Y
	PWR_80UM	P	PWR_80UM	PP1V8_S2_LAT_BRIDGE_VIO	Y
WiFi	PWR_100UM	P	PWR_100UM	PP0V72_CBUCK*	Y
	PWR_100UM	P	PWR_100UM	PP1V02_ABUCK*	Y
	PWR_100UM	P	PWR_100UM	PP3V3_BTLDO	Y
Fez	PWR_SHAPE	P	PWR_SHAPE	PP_VBAT_FEZ	Y
	PWR_100UM	P	PWR_100UM	PP_1V85_FEZ	Y
NFC	PWR_80UM	P	PWR_80UM	PP1V2_NFC_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*VDDBOOST	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VDDC	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*MIX	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VDDNV	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*TVDD	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VDDPLL	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX,PP_NFC_*_VCASCHI,PP_NFC_*_VCASLO	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VREF	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*AVDD	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*VUP	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_P_ANT_POS,NFC_P_ANT_NEG,NFC_*_ANT_MATCH_*	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_*_TXP,NFC_*_TXN,NFC_*_BAL*,NFC_*_PROBE_*	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VHV	Y
	PWR_80UM	P	PWR_80UM	PP_SIMVCC1	Y

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	GND	S	MSAP_YIELD	GND	Y
Power	PWR_DEFAULT	S	DEFAULT	=	Y
	PWR_50UM	S	DEFAULT	=	Y
	PWR_80UM	S	DEFAULT	=	Y
	PWR_100UM	S	DEFAULT	=	Y
	PWR_200UM	S	DEFAULT	=	Y
	PWR_300UM	S	DEFAULT	=	Y
	PWR_500UM	S	DEFAULT	=	Y
	PWR_750UM	S	DEFAULT	=	Y
	PWR_SHAPE	S	DEFAULT	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_100UM	GND	100UM-249UM_SPACING
PWR_100UM	PWR_100UM	100UM-249UM_SPACING
PWR_100UM	PWR_200UM	100UM-249UM_SPACING
PWR_100UM	PWR_300UM	100UM-249UM_SPACING
PWR_100UM	PWR_500UM	100UM-249UM_SPACING
PWR_100UM	PWR_750UM	100UM-249UM_SPACING
PWR_100UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_200UM	GND	100UM-249UM_SPACING
PWR_200UM	PWR_200UM	100UM-249UM_SPACING
PWR_200UM	PWR_300UM	100UM-249UM_SPACING
PWR_200UM	PWR_500UM	100UM-249UM_SPACING
PWR_200UM	PWR_750UM	100UM-249UM_SPACING
PWR_200UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_300UM	GND	250UM+_SPACING
PWR_300UM	PWR_300UM	250UM+_SPACING
PWR_300UM	PWR_500UM	250UM+_SPACING
PWR_300UM	PWR_750UM	250UM+_SPACING
PWR_300UM	PWR_SHAPE	250UM+_SPACING
PWR_500UM	GND	250UM+_SPACING
PWR_500UM	PWR_500UM	250UM+_SPACING
PWR_500UM	PWR_750UM	250UM+_SPACING
PWR_500UM	PWR_SHAPE	250UM+_SPACING
PWR_750UM	GND	250UM+_SPACING
PWR_750UM	PWR_750UM	250UM+_SPACING
PWR_750UM	PWR_SHAPE	250UM+_SPACING
PWR_SHAPE	GND	250UM+_SPACING
PWR_SHAPE	PWR_SHAPE	250UM+_SPACING

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Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET0	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_VREG_S1_S6_SENSE	Y
E_DP_NTC	E	GENERIC_DP	DP:DP_NTC_*	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_ETDAC_QET0	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET0	Y
DP_ETDAC_QET1	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_VREG_S1_S6_SENSE	Y
DP_NTC	P	GENERIC_DP	DP:DP_NTC_*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_GENERIC	S	DEFAULT	=	Y
DP_NTC	S	A_DIELECTRIC_1.5X	=	Y
DP_ETDAC_QET0	S	A_DIELECTRIC_1.5X	=	Y
DP_ETDAC_QET1	S	A_DIELECTRIC_1.5X	=	Y

RF-Shield

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
SuBus	RF_SHIELD_SUBUS_WIDE	P	PWR_SUBUS	*SUBUS_UAT*	Y
	RF_SHIELD_SUBUS_DEFAULT	P	DEFAULT	*SUBUS_LAT*	Y
RFFE	RF_SHIELD_RFFE	P	DEFAULT	RFFE_WLAN_TO_LAT*	Y
	RF_SHIELD_RFFE	P	DEFAULT	RFFE_WLAN_TO_UAT*	Y
	RF_SHIELD_RFFE	P	DEFAULT	RFFE0_XCVR_TO_LAT_LAA_VIO_R	Y
	RF_SHIELD_RFFE	P	DEFAULT	SHIELD_RFFE*	Y
Clocks	RF_SHIELD_CLK	P	DEFAULT	SHIELD*38P4M*CLK*	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD*19P2M*CLK*	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD*SLEEP*CLK*	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD_*_CLK_32K	Y
Analog	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_ZQ	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_CAL	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_REXT	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_CAL_RES	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD_RFFE	S	DEFAULT	=	Y
RF_SHIELD_SUBUS_WIDE	S	DEFAULT	=	Y
RF_SHIELD_SUBUS_DEFAULT	S	DEFAULT	=	Y
RF_SHIELD_CLK	S	A_DIELECTRIC_3X	=	Y
RF_SHIELD_ANALOG	S	A_DIELECTRIC_3X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
RF_SHIELD_RFFE	PWR_DEFAULT	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_50UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_80UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_100UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_200UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_300UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_500UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_750UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_SHAPE	A_DIELECTRIC_3X
RF_SHIELD_RFFE	GND	DEFAULT
RF_SHIELD_CLK	GND	DEFAULT
RF_SHIELD_ANALOG	GND	DEFAULT
DP_ETDAC_QET0	GND	DEFAULT
DP_ETDAC_QET1	GND	DEFAULT
DP_NTC	GND	DEFAULT

Grouping Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	P	DEFAULT	GPIO*, IO_*	Y
GRP_I2C	P	DEFAULT	I2C*	Y
GRP_I2S	P	DEFAULT	I2S*LRCLK*, I2S*BCLK*, I2S*DOUT*, I2S*DIN*	Y
GRP_SPI	P	DEFAULT	SPI*MOSI*, SPI*MISO*, SPI*CS*	Y
GRP_UART	P	DEFAULT	UART*	Y
GRP_SWD	P	DEFAULT	SWD*	Y
GRP_SPMI_DATA	P	DEFAULT	SPMI*DATA*	Y
GRP_PCIE_SIDE	P	DEFAULT	PCIE*CLKREQ*, PCIE*PERST*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	S	DEFAULT	=	Y
GRP_I2C	S	DEFAULT	=	Y
GRP_I2S	S	DEFAULT	=	Y
GRP_SPI	S	DEFAULT	=	Y
GRP_UART	S	DEFAULT	=	Y
GRP_SWD	S	DEFAULT	=	Y
GRP_SPMI_DATA	S	DEFAULT	=	Y
GRP_PCIE_SIDE	S	DEFAULT	=	Y

BB XO

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
XTAL_OSC	S	A_DIELECTRIC_3X	XO_GND	Y
XTAL_OSC	S	A_DIELECTRIC_3X	XO_THERM	Y
XTAL_OSC	S	A_DIELECTRIC_3X	THERMAL_GNSS_XO_THERM	Y

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
XTAL_OSC	XTAL_OSC	DEFAULT

Clocks

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	P	DEFAULT	CLK_*	Y
CLK	P	DEFAULT	SPMI*CLK*	Y
CLK	P	DEFAULT	SPI*SCLK*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	S	A_DIELECTRIC_1.5X	=	Y

Sensitive Analog

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	P	DEFAULT	ANALOG*PDTS*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
ANALOG	GND	DEFAULT
CLK	GND	DEFAULT

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50 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.059
ISL3	ISL2,ISL4	50	0.029
ISL5	ISL4,ISL6	50	0.041
ISL7	ISL6,BOTTOM	50	0.029

50 Wide

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
TOP	ISL3	50	0.166
ISL6	ISL4,BOTTOM	50	0.089

50 Wide, Surface Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_SURFACE_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.059
ISL6	ISL4,BOTTOM	50	0.089

50 Wide, L3 and Surface Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_SURFACE_L3_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.059
ISL3	ISL2,ISL4	50	0.029
ISL6	ISL4,BOTTOM	50	0.089

50 Wide, L3 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_L3_THIN		ZONE NAME= PRIMARY	
TOP	ISL3	50	0.166
ISL3	ISL2,ISL4	50	0.029
ISL6	ISL4,BOTTOM	50	0.089

50-ohm (Wide) Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT2*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4_MB_HB_WLAN24	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4_MB_HB_WLAN24_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HB_PAD_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LBDSM_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_RX1_DRX_OUT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_RX1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_TX	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_TX_UAT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HBDSM_*	Y
GNSS	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_L*_LNA_IN*	Y
WiFi	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_WLAN_G_BT_ANT3*	Y
UHB PAD	50_TRX_UHB_PAD	P	A_50_WIDE_SE	50_TRX_UHB_PAD_*	Y
Direct Net	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_WLAN_G_BT_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_TPLX_ANT_LB_LMB_MB_HB_L1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_G_BT_LAT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_LMB_ANT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_MB_OUT_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_MB_OUT	Y
	50_TRX_PAUHBU	P	A_50_WIDE_SE	50_TRX_PAUHBU_N79_ANT1_TO_ANT4*	Y
	50_TRX_PAUHBU	P	A_50_WIDE_SE	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_RX1_ANT2	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_TX	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_G_BT_ANT4_NPLXR_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_TX_M	Y

Spacing

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Everything	50_TRX_WIDE	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y
	50_TRX_UHB_PAD	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y
	50_TRX_PAUHBU	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y

Class-Class Spacing

	CLASS TO CLASS SPACING		
	CLASS NAME	CLASS NAME	CONSTRAINT SET
GND	50_TRX_WIDE	GND	NA_DIELECTRIC_2X_50_WIDE_SE
	50_TRX_UHB_PAD	GND	NA_DIELECTRIC_2X_50_WIDE_SE
UHB PAD to Self	50_TRX_UHB_PAD	50_TRX_UHB_PAD	DIELECTRIC_4XV_50_WIDE_SE_UHB_PAD
	50_TRX_PAUHBU	GND	NA_DIELECTRIC_2X_50_WIDE_SE
PAUHBU to Self	50_TRX_PAUHBU	50_TRX_PAUHBU	DIELECTRIC_4XV_50_WIDE_SE_UHB_PAD

50-ohm (Hybrid) Constraints

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_FEM_M	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_BPF	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_BPF_R	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_IN_LMB_PAD_LMB_ANT_M	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB_M	Y
50_TRX_WIDE_SURFACE_L3_THIN	P	A_50_WIDE_SURFACE_L3_THIN_SE	50_TRX_PAUHBU_N79_ANT2_TO_ANT8*	Y
50_TRX_WIDE_SURFACE_L3_THIN	P	A_50_WIDE_SURFACE_L3_THIN_SE	50_WLAN_A_C1_TXRX	Y
50_TRX_WIDE_L3_THIN	P	A_50_WIDE_L3_THIN_SE	50_TRX_CPLR_U_CPL1_ANT_LB_LMB_MB_HB_L1	Y
50_TRX_WIDE_L3_THIN	P	A_50_WIDE_L3_THIN_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_HYBRID	S	NA_DIELECTRIC_4XV_50_WIDE_SURFACE_THIN_SE	=	Y
50_TRX_WIDE_SURFACE_L3_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_SURFACE_L3_THIN_SE	=	Y
50_TRX_WIDE_L3_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_L3_THIN_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_TRX_HYBRID	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_THIN_SE
50_TRX_WIDE_SURFACE_L3_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_L3_THIN_SE
50_TRX_WIDE_L3_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_L3_THIN_SE

50-ohm (Thin) Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Wildcards	50_TX0_THIN	P	A_50_THIN_SE	50_TX_IN_*TX0_*	Y
	50_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_*TX1_*	Y
	50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_*TX2_*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_HBDSM_RXOUT_DRX*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_XCVR_DRX*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_XCVR_PRX*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_HB_PAD_PRX_OUT*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_MIMO*_RXOUT_DRX*	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_A_C0*	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_C0*	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_C1*	Y
Direct Net	50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_XCVR_DRX10	Y
	50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_XCVR_PRX12	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LBDSM_RXOUT1	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LBDSM_RXOUT2	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_RX_OUT1	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_N79_RX_OUT1	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_RX_OUT2	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_N79_RX_OUT2	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT_M	Y
	50_THIN	P	A_50_THIN_SE	50_RX_GNSS_L1	Y
	50_THIN	P	A_50_THIN_SE	50_RX_GNSS_L5	Y
	50_THIN	P	A_50_THIN_SE	50_RX_L5_LNA_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_L5_LNA_NOTCH2	Y
	50_THIN	P	A_50_THIN_SE	50_RX_L1_LNA_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_L1_LNA_NOTCH2	Y
	50_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_FBRX_1	Y
	50_THIN	P	A_50_THIN_SE	50_CPLR_L_CPL1_LAT_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_UHB_L_CPLR_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_CPLR_U_CPL1_UHB_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_CPLR_U_CPL1_UAT_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_LAT_TXRX_FEM	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_UAT_TXRX_FEM	Y
	50_THIN	P	A_50_THIN_SE	50_TANGIER_TP11	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_A_C1_TXRX_MODULE	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_CPLR_U_CPL1_IN_LB_LMB_MB_HB_L1	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_LB_PORTB_RX1_M	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_ANT4_MB_HB_WLAN24_L	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_ANT4_MB_HB_WLAN24_NOTCH	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TX0_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX2_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_RX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y

Class-Class Spacing

	CLASS TO CLASS SPACING		
	CLASS NAME	CLASS NAME	CONSTRAINT SET
Same Class	50_TX0_THIN	50_TX0_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	50_TX1_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	50_TX2_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	50_RX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
GND	50_TX0_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE

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PAGE TITLE: CONSTRAINTS: 50-Ohm

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FEZ FIDUCIALS

FD0920 — P3MM SM 998-4642 ROOM=ASSEMBLY
FD0921 — P3MM SM 998-4642 ROOM=ASSEMBLY
FD0922 — P3MM SM 998-4642 ROOM=ASSEMBLY
FD0923 — P3MM SM 998-4642 ROOM=ASSEMBLY

SHIELDS

CRITICAL
SH0900 SM 806-23604
SHLD-TTS-SHORT-MLB-D52

CRITICAL
SH0901 SM 806-23497
SHLD-TTS-INTERNAL-MLB-NW-D54

CRITICAL
SH0902 SM 806-25905
SHLD-MLB-SOUTH-NARROW-D54

STIFFENER

CRITICAL
ST0900
STIFFENER-MLB-D54
SM 806-24036

FIDUCIALS

FD0900 FID 0P5SQ-CROSS-NSP 998-04808 ROOM=ASSEMBLY
FD0901 FID 0P5SQ-CROSS-NSP 998-04808 ROOM=ASSEMBLY
FD0902 FID 0P5SQ-CROSS-NSP 998-04808 ROOM=ASSEMBLY
FD0903 FID 0P5SQ-CROSS-NSP 998-04808 ROOM=ASSEMBLY
FD0904 FID 0P5SQ-CROSS-NSP 998-04808 ROOM=ASSEMBLY
FD0905 FID 0P5SQ-CROSS-NSP 998-04808 ROOM=ASSEMBLY
FD0910 FID 0P5SQ-SMP3SQ-NSP 998-00557 ROOM=ASSEMBLY
FD0911 FID 0P5SQ-SMP3SQ-NSP 998-00557 ROOM=ASSEMBLY
FD0912 FID 0P5SQ-SMP3SQ-NSP 998-00557 ROOM=ASSEMBLY
FD0913 FID 0P5SQ-SMP3SQ-NSP 998-00557 ROOM=ASSEMBLY
FD0914 FID 0P5SQ-SMP3SQ-NSP 998-00557 ROOM=ASSEMBLY
FD0915 FID 0P5SQ-SMP3SQ-NSP 998-00557 ROOM=ASSEMBLY

UF: NOSTUFF with Kolkata

BOMOPTION=NO-KOLKATA CKPLUS_WAIVE=TERMSHORTED
R0944 0.00 0% 1/32W MF 01005 ROOM=DFM
R0906 0.00 0% 1/32W MF 01005 ROOM=DFM

UF: Always stuff

CKPLUS_WAIVE=TERMSHORTED
R0910 0.00 0% 1/32W MF 01005 ROOM=DFM
R0911 0.00 0% 1/32W MF 01005 ROOM=DFM
R0900 0.00 0% 1/32W MF 01005 ROOM=DFM
R0956 0.00 0% 1/32W MF 01005 ROOM=DFM
R0903 0.00 0% 1/32W MF 01005 ROOM=DFM
R0907 0.00 0% 1/32W MF 01005 ROOM=DFM
R0908 0.00 0% 1/32W MF 01005 ROOM=DFM
R0977 0.00 0% 1/32W MF 01005 ROOM=DFM
R0978 0.00 0% 1/32W MF 01005 ROOM=DFM
R0979 0.00 0% 1/32W MF 01005 ROOM=DFM
R0960 0.00 0% 1/32W MF 01005 ROOM=DFM
R0961 0.00 0% 1/32W MF 01005 ROOM=DFM
R0962 0.00 0% 1/32W MF 01005 ROOM=DFM
R0963 0.00 0% 1/32W MF 01005 ROOM=DFM
R0948 0.00 0% 1/32W MF 01005 ROOM=DFM
R0964 0.00 0% 1/32W MF 01005 ROOM=DFM
R0965 0.00 0% 1/32W MF 01005 ROOM=DFM
R0959 0.00 0% 1/32W MF 01005 ROOM=DFM
R0972 0.00 0% 1/32W MF 01005 ROOM=DFM
R0973 0.00 0% 1/32W MF 01005 ROOM=DFM
R0974 0.00 0% 1/32W MF 01005 ROOM=DFM
R0975 0.00 0% 1/32W MF 01005 ROOM=DFM
R0976 0.00 0% 1/32W MF 01005 ROOM=DFM
R0909 0.00 0% 1/32W MF 01005 ROOM=DFM
R0924 0.00 0% 1/32W MF 01005 ROOM=DFM
R0942 0.00 0% 1/32W MF 01005 ROOM=DFM
R0943 0.00 0% 1/32W MF 01005 ROOM=DFM
R0957 0.00 0% 1/32W MF 01005 ROOM=DFM
R0958 0.00 0% 1/32W MF 01005 ROOM=DFM

UF: Stuff with Kolkata

BOMOPTION=RF_SKU:NAMM CKPLUS_WAIVE=TERMSHORTED
R0912 0.00 0% 1/32W MF 01005 ROOM=DFM
R0913 0.00 0% 1/32W MF 01005 ROOM=DFM
R0914 0.00 0% 1/32W MF 01005 ROOM=DFM
R0915 0.00 0% 1/32W MF 01005 ROOM=DFM
R0916 0.00 0% 1/32W MF 01005 ROOM=DFM
R0917 0.00 0% 1/32W MF 01005 ROOM=DFM
R0918 0.00 0% 1/32W MF 01005 ROOM=DFM
R0919 0.00 0% 1/32W MF 01005 ROOM=DFM
R0949 0.00 0% 1/32W MF 01005 ROOM=DFM
R0951 0.00 0% 1/32W MF 01005 ROOM=DFM
R0920 0.00 0% 1/32W MF 01005 ROOM=DFM
R0921 0.00 0% 1/32W MF 01005 ROOM=DFM
R0922 0.00 0% 1/32W MF 01005 ROOM=DFM
R0923 0.00 0% 1/32W MF 01005 ROOM=DFM
R0925 0.00 0% 1/32W MF 01005 ROOM=DFM
R0926 0.00 0% 1/32W MF 01005 ROOM=DFM
R0927 0.00 0% 1/32W MF 01005 ROOM=DFM
R0928 0.00 0% 1/32W MF 01005 ROOM=DFM
R0902 0.00 0% 1/32W MF 01005 ROOM=DFM
R0946 0.00 0% 1/32W MF 01005 ROOM=DFM
R0929 0.00 0% 1/32W MF 01005 ROOM=DFM
R0930 0.00 0% 1/32W MF 01005 ROOM=DFM
R0931 0.00 0% 1/32W MF 01005 ROOM=DFM
R0932 0.00 0% 1/32W MF 01005 ROOM=DFM
R0933 0.00 0% 1/32W MF 01005 ROOM=DFM
R0934 0.00 0% 1/32W MF 01005 ROOM=DFM
R0935 0.00 0% 1/32W MF 01005 ROOM=DFM
R0936 0.00 0% 1/32W MF 01005 ROOM=DFM
R0971 0.00 0% 1/32W MF 01005 ROOM=DFM
R0954 0.00 0% 1/32W MF 01005 ROOM=DFM
R0937 0.00 0% 1/32W MF 01005 ROOM=DFM
R0938 0.00 0% 1/32W MF 01005 ROOM=DFM
R0939 0.00 0% 1/32W MF 01005 ROOM=DFM
R0940 0.00 0% 1/32W MF 01005 ROOM=DFM
R0941 0.00 0% 1/32W MF 01005 ROOM=DFM
R0945 0.00 0% 1/32W MF 01005 ROOM=DFM
R0950 0.00 0% 1/32W MF 01005 ROOM=DFM
R0952 0.00 0% 1/32W MF 01005 ROOM=DFM
R0970 0.00 0% 1/32W MF 01005 ROOM=DFM
R0955 0.00 0% 1/32W MF 01005 ROOM=DFM
R0953 0.00 0% 1/32W MF 01005 ROOM=DFM
R0901 0.00 0% 1/32W MF 01005 ROOM=DFM
R0904 0.00 0% 1/32W MF 01005 ROOM=DFM
R0905 0.00 0% 1/32W MF 01005 ROOM=DFM
R0966 0.00 0% 1/32W MF 01005 ROOM=DFM
R0967 0.00 0% 1/32W MF 01005 ROOM=DFM
R0968 0.00 0% 1/32W MF 01005 ROOM=DFM
R0969 0.00 0% 1/32W MF 01005 ROOM=DFM

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PAGE TITLE: SYSTEM: Mechanical

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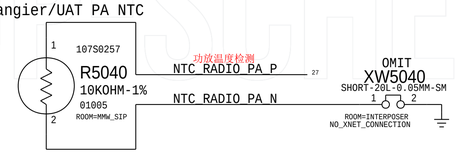
Bot MLB NTCs

Place NTC XWs near PMU, route P/N differentially

Baseband/BB PMU NTC

Tangier/UAT PA NTC



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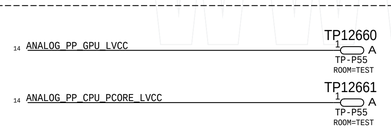
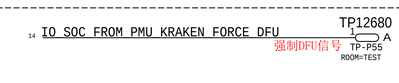
LVCC

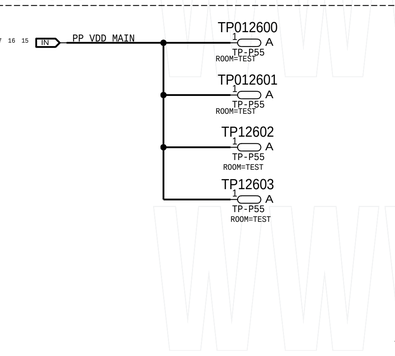


REL Bias

DFU

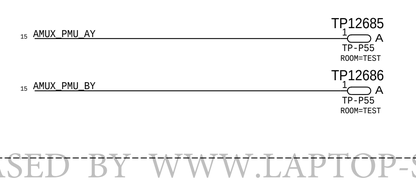


Power/GND



VBUS

AMUX



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J INT TOP

INTERPOSER-MLB-RF-TOP

SM

SYM 1 OF 4

998-22293

OMIT

13	GND	1	IO1	IO91	91	IO_BT_TO_R1_WAKE	13
13	GND	2	IO2	IO92	92	GPIO_R1_TO_BB_LAA_SW_CTRL	13
13	GND	3	IO3	IO93	93	GND	13
13	GPIO_CANARY_2C_TO_2D	4	IO4	IO94	94	GPIO_AP_FROM_WLAN_TIME_SYNC	13
13	NFC_P_ANT_NEG	5	IO5	IO95	95	GPIO_BB_TO_R1_COEX	13
13	GND	6	IO6	IO96	96	GND	13
13	NFC_P_ANT_NEG	7	IO7	IO97	97	GND	13
13	GND	8	IO8	IO98	98	IO_BT_TO_R1_TIME_SYNC	13
13	NFC_P_ANT_NEG	9	IO9	IO99	99	GPIO_R1_TO_WLAN_COEX	13
13	GND	10	IO10	IO100	100	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	13
13	NFC_P_ANT_NEG	11	IO11	IO101	101	GND	13
13	GPIO_NFC_F_NFC_P_SYNC2	12	IO12	IO102	102	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	13
13	GND	13	IO13	IO103	103	GPIO_WLAN_TO_R1_COEX	13
13	GND	14	IO14	IO104	104	GND	13
13	50_TRX_ANT4_MB_HB_WLAN24	15	IO15	IO105	105	GND	13
13	GND	16	IO16	IO106	106	NFC_P_ANT_POS	13
13	GND	17	IO17	IO107	107	GND	13
13	PCIE_GP1_AP_TO_WLAN_PERST_L	18	IO18	IO108	108	NFC_P_ANT_POS	13
13	GPIO_AP_TO_BB_PEAK_PWR_IND	19	IO19	IO109	109	GND	13
13	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	20	IO20	IO110	110	NFC_P_ANT_POS	13
13	SWD_AP_BI_BB_SWDIO CPU到基带的SWD总线数据	21	IO21	IO111	111	GND	13
13	NTC_STOCKHOLM	22	IO22	IO112	112	NFC_P_ANT_POS	13
13	GPIO_R1_TO_BB_CH9_COEX	23	IO23	IO113	113	GND	13
13	GPIO_NFC_F_NFC_P_SYNC1	24	IO24	IO114	114	CLK_BBPMU_TO_DOTARA_38M4	13
13	GND	25	IO25	IO115	115	GND	13
13	GND	26	IO26	IO116	116	GND	13
13	PP1V2_S4	27	IO27	IO117	117	GND	13
13	GND	28	IO28	IO118	118	GND	13
13	I2C_R1_TO_NFC_SCL	29	IO29	IO119	119	50_WLAN_A_C0_TXRX_FEM_M	13
13	GND	30	IO30	IO120	120	GND	13
13	I2C_R1_TO_NFC_SDA	31	IO31	IO121	121	GND	13
13	GND	32	IO32	IO122	122	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	13
13	NFC_P_TEST_OUT	33	IO33	IO123	123	GND	13
13	GND	34	IO34	IO124	124	GND	13
13	GND	35	IO35	IO125	125	50_TRX_ANT2_LB_LMB_MB_HB_L1	13
13	GND	36	IO36	IO126	126	GND	13
13	GND	37	IO37	IO127	127	GND	13
13	GND	38	IO38	IO128	128	50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M	13
13	GND	39	IO39	IO129	129	GND	13
13	GND	40	IO40	IO130	130	GND	13
13	GND	41	IO41	IO131	131	50_LAA_RX_XCVR_DRX10	13
13	GND	42	IO42	IO132	132	GND	13
13	GND	43	IO43	IO133	133	GND	13
13	GND	44	IO44	IO134	134	GND	13
13	GND	45	IO45	IO135	135	IO_TOUCH_TO_MANY_SCAN_ACTIVE_U	13
13	GND	46	IO46	IO136	136	GPIO_CANARY_1C_TO_1D	13
13	GND	47	IO47	IO137	137	GND	13
13	GND	48	IO48	IO138	138	GND	13
13	GND	49	IO49	IO139	139	GPIO_CANARY_1C_TO_1D	13
13	GND	50	IO50	IO140	140	GND	13
13	GND	51	IO51	IO141	141	GND	13
13	GND	52	IO52	IO142	142	GND	13
13	GND	53	IO53	IO143	143	GND	13
13	GND	54	IO54	IO144	144	GND	13
13	GND	55	IO55	IO145	145	GND	13
13	GND	56	IO56	IO146	146	GND	13
13	GND	57	IO57				
13	GND	58	IO58				
13	GND	59	IO59	IO149	149	GND	13
13	GND	60	IO60	IO150	150	GND	13
13	GND	61	IO61	IO151	151	GND	13
13	GND	62	IO62	IO152	152	GND	13
13	GND	63	IO63	IO153	153	GND	13
13	GND	64	IO64	IO154	154	GND	13
13	GND	65	IO65	IO155	155	GND	13
13	GND	66	IO66	IO156	156	GND	13
13	GND	67	IO67	IO157	157	GND	13
13	GND	68	IO68	IO158	158	GND	13
13	GND	69	IO69	IO159	159	GND	13
13	GND	70	IO70	IO160	160	GND	13
13	GND	71	IO71	IO161	161	GND	13
13	GND	72	IO72	IO162	162	GND	13
13	GND	73	IO73	IO163	163	GND	13
13	GND	74	IO74	IO164	164	GND	13
13	GND	75	IO75	IO165	165	GND	13
13	GND	76	IO76	IO166	166	GND	13
13	GND	77	IO77	IO167	167	GND	13
13	GND	78	IO78	IO168	168	GND	13
13	GND	79	IO79	IO169	169	GND	13
13	GND	80	IO80	IO170	170	GND	13
13	GND	81	IO81	IO171	171	GND	13
13	GND	82	IO82	IO172	172	GPIO_CANARY_1A_TO_1B	13
13	GND	83	IO83	IO173	173	GND	13
13	GND	84	IO84	IO174	174	GND	13
13	GND	85	IO85	IO175	175	GND	13
13	GPIO_BB_TO_R1_CH9_REQ	86	IO86	IO176	176	SHIELD_RFFE5_SCLK_SDR	13
13	GND	87	IO87	IO177	177	GND	13
13	SWD_AP_TO_MANY_SWCLK CPU输出的SWD总线时钟	88	IO88	IO178	178	SHIELD_RFFE5_SDATA_SDR	13
13	GND	89	IO89	IO179	179	GND	13
13	UAT_TUNER_TO_R1_STATE	90	IO90	IO180	180	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	13

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14	GPIO_CANARY_1A_TO_1B	181	IO181	IO271	271	GPIO_S4_PMU_TO_WLAN_REG_ON	14
14	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	182	IO182	IO272	272	GND	14
14	GND	183	IO183	IO273	273	GND	14
14	CLK_BBPMU_TO_NFC_38M	184	IO184	IO274	274	GPIO_PMU_FROM_WLAN_HOST_WAKE	14
14	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	185	IO185	IO275	275	GND	14
14	GND	186	IO186	IO276	276	PP1V8_S4	14
14	GND	187	IO187	IO277	277	PP_1V8_LDO6	14
14	I2S2_AP_TO_BB_DOUT	188	IO188	IO278	278	GND	14
14	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	189	IO189	IO279	279	PP_APT_L_PA	14
14	I2S2_AP_FROM_BB_DIN	190	IO190	IO280	280	GND	14
14	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	191	IO191	IO281	281	PP_APT_L_PA	14
14	I2S2_AP_FROM_BB_BCLK	192	IO192	IO282	282	IO_TOUCH_TO_MANY_SCAN_ACTIVE	14
14	GND	193	IO193	IO283	283	GND	14
14	I2S2_AP_FROM_BB_LRCLK	194	IO194	IO284	284	GND	14
14	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	195	IO195	IO285	285	SHIELD_ETDAC_QET1_N	14
14	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	196	IO196	IO286	286	GND	14
14	GPIO_NFC_TO_BBPMU_CLK_EN	197	IO197	IO287	287	SHIELD_ETDAC_QET1_P	14
14	GND	198	IO198	IO288	288	GND	14
14	GND	199	IO199	IO289	289	SUBUS_LAT_A	14
14	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	200	IO200	IO290	290	GND	14
14	GND	201	IO201	IO291	291	SHIELD_RFFE8_SCLK_SDR	14
14	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	202	IO202	IO292	292	GND	14
14	GND	203	IO203	IO293	293	SHIELD_RFFE8_SDATA_SDR	14
14	GND	204	IO204	IO294	294	GND	14
14	GND	205	IO205	IO295	295	GND	14
14	90_PCIE_GP2_AP_TO_BB_REFCLK_N	206	IO206	IO296	296	GND	14
14	GND	207	IO207	IO297	297	GND	14
14	90_PCIE_GP2_AP_TO_BB_REFCLK_P	208	IO208	IO298	298	GND	14
14	GND	209	IO209	IO299	299	GND	14
14	GND	210	IO210	IO300	300	GND	14
14	GND	211	IO211	IO301	301	GND	14
14	GND	212	IO212	IO302	302	GND	14
14	GND	213	IO213	IO303	303	GND	14
14	GND	214	IO214	IO304	304	GND	14
14	GND	215	IO215	IO305	305	GND	14
14	GND	216	IO216	IO306	306	50_RX_XCVR_PRX14_N79_RX_OUT1	14
14	GND	217	IO217	IO307	307	GND	14
14	GND	218	IO218	IO308	308	GND	14
14	GND	219	IO219	IO309	309	50_RX_XCVR_PRX16_UHB_RX_OUT1	14
14	GND	220	IO220	IO310	310	GND	14
14	GND	221	IO221	IO311	311	GND	14
14	GND	222	IO222	IO312	312	50_TRX_UHB_PAD_PORTB_TX_M	14
14	90_PCIE_GP1_AP_FROM_WLAN_RX_N	223	IO223	IO313	313	GND	14
14	GND	224	IO224	IO314	314	GND	14
14	90_PCIE_GP1_AP_FROM_WLAN_RX_P	225	IO225	IO315	315	50_TRX_UHB_PAD_N79_PORTB_TX_M	14
14	GND	226	IO226	IO316	316	GND	14
14	GND	227	IO227	IO317	317	GND	14
14	GND	228	IO228	IO318	318	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	14
14	90_PCIE_GP1_AP_TO_WLAN_TX_P	229	IO229	IO319	319	GND	14
14	GND	230	IO230	IO320	320	GND	14
14	90_PCIE_GP1_AP_TO_WLAN_TX_N	231	IO231	IO321	321	50_RX_XCVR_PRX15_N79_RX_OUT2	14
14	GND	232	IO232	IO322	322	GND	14
14	GND	233	IO233	IO323	323	GND	14
14	GND	234	IO234	IO324	324	50_TX_IN_XCVR_TX1_LB_JB	14
14	90_PCIE_GP2_AP_FROM_BB_RX_N	235	IO235	IO325	325	50_TX_IN_XCVR_TX0_LB	14
14	GND	236	IO236	IO326	326	GND	14
14	90_PCIE_GP2_AP_FROM_BB_RX_P	237	IO237	IO327	327	GND	14
14	GND	238	IO238	IO328	328	50_RX_XCVR_PRX6_LB_A_RX0	14
14	GND	239	IO239	IO329	329	50_RX_XCVR_PRX10_LB_PRX_OUT2	14
14	GND	240	IO240	IO330	330	GND	14
14	90_PCIE_GP2_AP_TO_BB_TX_P	241	IO241	IO331	331	GND	14
14	GND	242	IO242	IO332	332	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	14
14	90_PCIE_GP2_AP_TO_BB_TX_N	243	IO243	IO333	333	GND	14
14	GND	244	IO244	IO334	334	GND	14
14	GND	245	IO245	IO335	335	50_RX_XCVR_PRX17_UHB_RX_OUT2	14
14	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	246	IO246	IO336	336	GND	14
14	GND	247	IO247	IO337	337	GND	14
14	GND	248	IO248	IO338	338	50_UHB_L_CPLR_OUT	14
14	GPIO_AOP_TO_WLAN_CONTEXT_A	249	IO249	IO339	339	GND	14
14	GPIO_AOP_TO_BB_FORCE_PWM	250	IO250	IO340	340	GND	14
14	GPIO_AOP_TO_WLAN_CONTEXT_B	251	IO251	IO341	341	GND	14
14	GND	252	IO252	IO342	342	GND	14
14	ANALOG_PP_GPU_LVCC	253	IO253	IO343	343	GND	14
14	IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	254	IO254	IO344	344	GND	14
14	GND	255	IO255	IO345	345	GND	14
14	GND	256	IO256	IO346	346	GND	14
14	SUBUS_UAT_B	257	IO257	IO347	347	GND	14
14	ANALOG_PP_CPU_PCORE_LVCC	258	IO258	IO348	348	GND	14
14	SUBUS_UAT_A	259	IO259	IO349	349	GND	14
14	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	260	IO260	IO350	350	GND	14
14	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	261	IO261	IO351	351	GND	14
14	GND	262	IO262	IO352	352	GND	14
14	GND	263	IO263	IO353	353	GND	14
14	GND	264	IO264	IO354	354	GND	14
14	GND	265	IO265	IO355	355	GND	14
14	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	266	IO266	IO356	356	GND	14
14	GND	267	IO267	IO357	357	GND	14
14	GND	268	IO268	IO358	358	GND	14
14	GND	269	IO269	IO359	359	GND	14
14	PP1V2_S2	270	IO270	IO360	360	GND	14

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15	GND	361	IO361	451	SHIELD_RFFE3_SCLK_SDR
15	GND	362	IO362	452	GND
15	GND	363	IO363	453	SHIELD_RFFE3_SDATA_SDR
15	GND	364	IO364	454	GND
15	GND	365	IO365	455	SHIELD_RFFE2_SCLK_SDR
15	GND	366	IO366	456	GND
15	GND	367	IO367	457	SHIELD_RFFE2_SDATA_SDR
15	GND	368	IO368	458	GND
15	GND	369	IO369	459	GND
15	GND	370	IO370	460	GND
15	GND	371	IO371	461	GND
15	GND	372	IO372	462	PP_VBUS1_E75
15	GND	373	IO373	463	PP_VBUS1_E75
15	GND	374	IO374	464	GND
15	GND	375	IO375	465	PP_UIM1_LDO11
15	GND	376	IO376	466	IO_BB_FROM_SIM2_DETECT
15	GND	377	IO377	467	PP_UIM2_LDO13
15	GND	378	IO378	468	GND
15	GND	379	IO379	469	IO_BB_TO_SIM2_CLK
15	GND	380	IO380	470	IO_BB_TO_SIM2_RESET
15	GND	381	IO381	471	IO_BB_BI_SIM2_DATA
15	50_TRX_LB_PORTB_RX1_M	382	IO382	472	GND
15	GND	383	IO383	473	GND
15	GND	384	IO384	474	GND
15	50_TRX_LB_PORTB_TX_M	385	IO385	475	GND
15	GND	386	IO386	476	GND
15	GND	387	IO387	477	IO_BB_FROM_SIM1_DETECT
15	PP_VDD_RF_1V2	388	IO388	478	IO_BB_TO_SIM1_RESET
15	SUBUS_LAT_C	389	IO389	479	IO_BB_BI_SIM1_DATA
15	GND	390	IO390	480	GND
15	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	391	IO391	481	IO_BB_TO_SIM1_CLK
15	SUBUS_LAT_B	392	IO392	482	GPIO_SEQ_PMU_TO_NFC_EN
15	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	393	IO393	483	GND
15	GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN	394	IO394	484	GND
15	GND	395	IO395	485	AMUX_PMU_BY
15	GND	396	IO396	486	AMUX_PMU_AY
15	50_TRX_L5_LNA_IN	397	IO397	487	NTC_RADIO_BB_P
15	GND	398	IO398	488	GND
15	GND	399	IO399	489	NTC_RADIO_PA_P
15	GND	400	IO400	490	PP1V2_NFC_S2
15	50_TRX_WLAN_G_BT_ANT3_NPLXR	401	IO401	491	GND
15	GND	402	IO402	492	GND
15	GND	403	IO403	493	GND
15	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	404	IO404	494	GPIO_SEQ_PMU_TO_BBPMU_RESET_L
15	GND	405	IO405	495	GND
15	GND	406	IO406	496	GND
15	50_WLAN_A_C1_TXRX_FEM_M	407	IO407	497	GND
15	GND	408	IO408		
15	GND	409	IO409	499	GND
15	50_LAA_RX_XCVR_PRX12	410	IO410	500	GND
15	GND	411	IO411	501	GND
15	GND	412	IO412	502	GND
15	50_TRX_HB_PAD_ANT1	413	IO413	503	GND
15	RFFE_WLAN_TO_LAT_5G_FEM_RST_L	414	IO414	504	GND
15	GND	415	IO415	505	GND
15	GND	416	IO416	506	PP3V0_S2
15	SHIELD_RFFE1_SCLK_SDR	417	IO417	507	UART1_AOP_FROM_BB_RXD
15	GND	418	IO418	508	GND
15	SHIELD_RFFE1_SDATA_SDR	419	IO419	509	GND
15	GND	420	IO420	510	GPIO_NFC_TO_ARCAMP_RESET_L
15	GND	421	IO421	511	UART1_AOP_TO_BB_TXD
15	GND	422	IO422	512	GND
15	GND	423	IO423	513	GPIO_AP_TO_BB_TIME_MARK
15	GND	424	IO424	514	GPIO_NFC_TO_ARCAMP_TRIG
15	GND	425	IO425	515	GPIO_AP_FROM_BT_AUDIO_SYNC
15	GND	426	IO426	516	GND
15	GND	427	IO427	517	PP1V8_S2
15	GND	428	IO428	518	GPIO_AP_TO_BB_COREDUMP
15	PP_VDD_BOOST	429	IO429	519	GPIO_BT_TO_BOT_SPKR_TRIG
15	GND	430	IO430	520	GND
15	GND	431	IO431	521	GND
15	GND	432	IO432	522	GND
15	50_TRX_HB_PAD_ANT2_M	433	IO433	523	PP_VDD_MAIN
15	GND	434	IO434	524	GND
15	GND	435	IO435	525	PP_VDD_MAIN
15	GND	436	IO436	526	GND
15	GND	437	IO437	527	PP_VDD_MAIN
15	GND	438	IO438	528	GND
15	50_CPLR_L_CPL1_LAT_OUT	439	IO439	529	PP_VDD_MAIN
15	GND	440	IO440	530	GND
15	GND	441	IO441	531	PP_VDD_MAIN
15	GND	442	IO442	532	GND
15	GND	443	IO443	533	GND
15	GND	444	IO444	534	GND
15	GND	445	IO445	535	PP_VDD_MAIN
15	GND	446	IO446	536	GND
15	GND	447	IO447	537	PP_VDD_MAIN
15	GND	448	IO448	538	GND
15	GND	449	IO449	539	PP_VDD_MAIN
15	GND	450	IO450	540	GND

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16	PP_VDD_MAIN	541	IO541
16	GND	542	IO542
16	PP_VDD_MAIN	543	IO543
16	GPIO_CANARY_2A_TO_2B	544	IO544
16	GND	545	IO545
16	GND	546	IO546
16	PP_VDD_MAIN	547	IO547
16	GND	548	IO548
16	GND	549	IO549
16	GND	550	IO550
16	GND	551	IO551
16	GND	552	IO552
16	GND	553	IO553
16	GND	554	IO554
16	GND	555	IO555
16	GND	556	IO556
16	GND	557	IO557
16	GND	558	IO558
16	GND	559	IO559
16	GND	560	IO560
16	GND	561	IO561
16	GPIO_CANARY_2A_TO_2B	562	IO562
16	GND	563	IO563
16	GND	564	IO564
16	GND	565	IO565
16	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	566	IO566
16	GND	567	IO567
16	GPIO_AP_FROM_BB_RESET_DETECT_L	568	IO568
16	GND	569	IO569
16	PCIE_GP2_AP_TO_BB_PERST_L	570	IO570
16	GND	571	IO571
16	GND	572	IO572
16	GND	573	IO573
16	PCIE_GP2_AP_BI_BB_CLKREQ_L	574	IO574
16	GND	575	IO575
16	GND	576	IO576
16	GND	577	IO577
16	GPIO_CANARY_2C_TO_2D	578	IO578
16	GND	579	IO579
16	GND	580	IO580
16	GND	581	IO581
16	GND	582	IO582
16	GND	583	IO583
16	GND	584	IO584
16	GND	585	IO585
16	GND	586	IO586
16	GND	587	IO587
16	GND	588	IO588
16	GND	589	IO589
16	GND	590	IO590
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16	GND	609	IO609
16	GND	610	IO610
16	GND	611	IO611
16	GND	612	IO612
16	GND	613	IO613
16	GND	614	IO614
16	GND	615	IO615
16	GND	616	IO616

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GND			
GND			
GND			
GPIO_CANARY_2C_TO_2D	GPIO_CANARY_2C_TO_2D CKPLUS_WAIVE=SINGLE_COMP_NET	MAKE_BASE=TRUE	16
NFC_P_ANT_NEG	NFC_P_ANT_NEG	MAKE_BASE=TRUE	13 17
GND			
NFC_P_ANT_NEG	NFC_P_ANT_NEG	MAKE_BASE=TRUE	13 17
GND			
NFC_P_ANT_NEG	NFC_P_ANT_NEG	MAKE_BASE=TRUE	13 17
GND			
NFC_P_ANT_NEG	NFC_P_ANT_NEG	MAKE_BASE=TRUE	13 17
GPIO_NFC_F_NFC_P_SYNC2	GPIO_NFC_F_NFC_P_SYNC2	MAKE_BASE=TRUE	17
GND			
GND			
50_TRX_ANT4_MB_HB_WLAN24	50_TRX_ANT4_MB_HB_WLAN24	MAKE_BASE=TRUE	17
GND			
GND			
PCIE_GP1_AP_TO_WLAN_PERST_L	PCIE_GP1_AP_TO_WLAN_PERST_L	MAKE_BASE=TRUE	18
GPIO_AP_TO_BB_PEAK_PWR_IND	GPIO_AP_TO_BB_PEAK_PWR_IND	MAKE_BASE=TRUE	17
PCIE_GP1_AP_BI_WLAN_CLKREQ_L	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	MAKE_BASE=TRUE	18
SWD_AP_BI_BB_SWDIO CPU到基带的SWD总线数据	SWD_AP_BI_BB_SWDIO	MAKE_BASE=TRUE	17
NTC_STOCKHOLM	NTC_STOCKHOLM	MAKE_BASE=TRUE	17
GPIO_R1_TO_BB_CH9_COEX	GPIO_R1_TO_BB_CH9_COEX	MAKE_BASE=TRUE	17
GPIO_NFC_F_NFC_P_SYNC1	GPIO_NFC_F_NFC_P_SYNC1	MAKE_BASE=TRUE	17
GND			
GND			
PP1V2_S4	PP1V2_S4	MAKE_BASE=TRUE	17 18
GND			
I2C_R1_TO_NFC_SCL	I2C_R1_TO_NFC_SCL	MAKE_BASE=TRUE	17
GND			
I2C_R1_TO_NFC_SDA	I2C_R1_TO_NFC_SDA	MAKE_BASE=TRUE	17
GND			
NFC_P_TEST_OUT	NFC_P_TEST_OUT	MAKE_BASE=TRUE	17
GND			
GND			
GND		

Interposer: Symbol 2 Aliases

LEFT SIDE

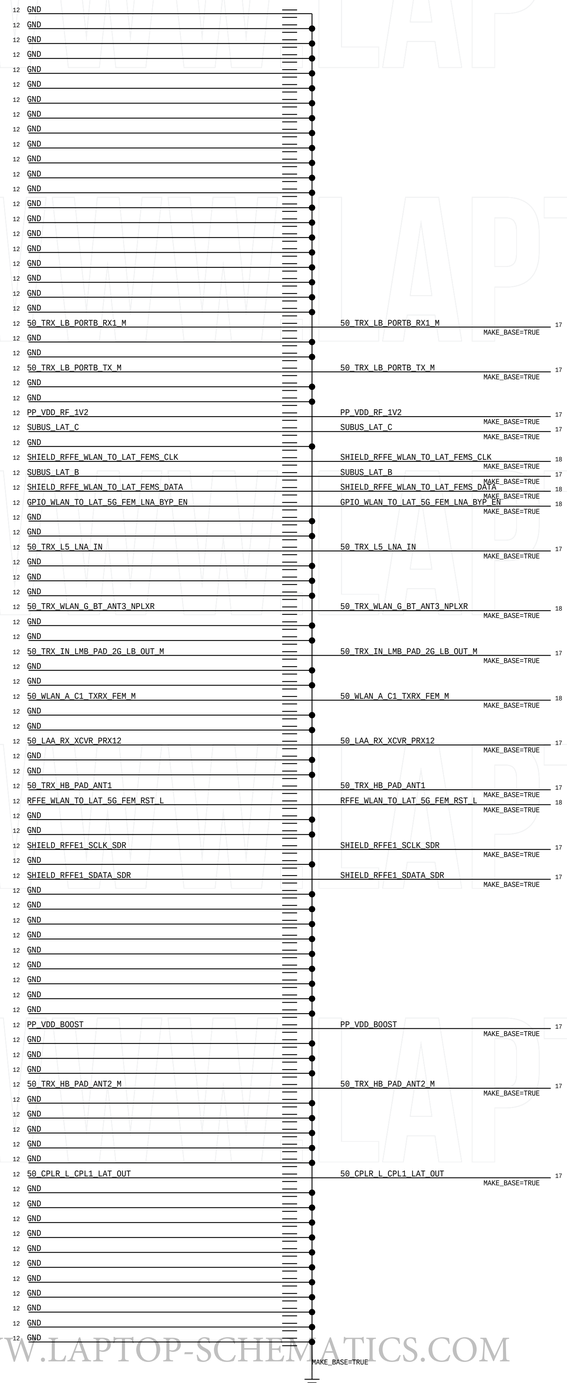
11	GPIO_CANARY_1A_TO_1B	GPIO_CANARY_1A_TO_1B	MAKE_BASE=TRUE 13
11	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	17 18
11	GND		MAKE_BASE=TRUE
11	CLK_BBPMU_TO_NFC_38M	CLK_BBPMU_TO_NFC_38M	17
11	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE 18
11	GND		MAKE_BASE=TRUE
11	GND		
11	I2S2_AP_TO_BB_DOUT	I2S2_AP_TO_BB_DOUT	17
11	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	MAKE_BASE=TRUE 18
11	I2S2_AP_FROM_BB_DIN	I2S2_AP_FROM_BB_DIN	MAKE_BASE=TRUE 17
11	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	MAKE_BASE=TRUE 18
11	I2S2_AP_FROM_BB_BCLK	I2S2_AP_FROM_BB_BCLK	MAKE_BASE=TRUE 17
11	GND		MAKE_BASE=TRUE
11	I2S2_AP_FROM_BB_LRCLK	I2S2_AP_FROM_BB_LRCLK	MAKE_BASE=TRUE 17
11	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	MAKE_BASE=TRUE 17
11	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	MAKE_BASE=TRUE 18
11	GPIO_NFC_TO_BBPMU_CLK_EN	GPIO_NFC_TO_BBPMU_CLK_EN	MAKE_BASE=TRUE 17
11	GND		MAKE_BASE=TRUE
11	GND		
11	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	MAKE_BASE=TRUE 18
11	GND		
11	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	MAKE_BASE=TRUE 18
11	GND		
11	GND		
11	GND		
11	90_PCIE_GP2_AP_TO_BB_REFCLK_N	90_PCIE_GP2_AP_TO_BB_REFCLK_N	MAKE_BASE=TRUE 17
11	GND		
11	90_PCIE_GP2_AP_TO_BB_REFCLK_P	90_PCIE_GP2_AP_TO_BB_REFCLK_P	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	90_PCIE_GP1_AP_FROM_WLAN_RX_N	90_PCIE_GP1_AP_FROM_WLAN_RX_N	MAKE_BASE=TRUE 18
11	GND		
11	90_PCIE_GP1_AP_FROM_WLAN_RX_P	90_PCIE_GP1_AP_FROM_WLAN_RX_P	MAKE_BASE=TRUE 18
11	GND		
11	GND		
11	GND		
11	90_PCIE_GP1_AP_TO_WLAN_TX_P	90_PCIE_GP1_AP_TO_WLAN_TX_P	MAKE_BASE=TRUE 18
11	GND		
11	90_PCIE_GP1_AP_TO_WLAN_TX_N	90_PCIE_GP1_AP_TO_WLAN_TX_N	MAKE_BASE=TRUE 18
11	GND		
11	GND		
11	GND		
11	90_PCIE_GP2_AP_FROM_BB_RX_N	90_PCIE_GP2_AP_FROM_BB_RX_N	MAKE_BASE=TRUE 17
11	GND		
11	90_PCIE_GP2_AP_FROM_BB_RX_P	90_PCIE_GP2_AP_FROM_BB_RX_P	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GND		
11	90_PCIE_GP2_AP_TO_BB_TX_P	90_PCIE_GP2_AP_TO_BB_TX_P	MAKE_BASE=TRUE 17
11	GND		
11	90_PCIE_GP2_AP_TO_BB_TX_N	90_PCIE_GP2_AP_TO_BB_TX_N	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A	MAKE_BASE=TRUE 18
11	GPIO_AOP_TO_BB_FORCE_PWM	GPIO_AOP_TO_BB_FORCE_PWM	MAKE_BASE=TRUE 17
11	GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B	MAKE_BASE=TRUE 18
11	GND		MAKE_BASE=TRUE
11	ANALOG_PP_GPU_LVCC	ANALOG_PP_GPU_LVCC	MAKE_BASE=TRUE 9
11	IO_PMU_TO_SYSTEM_RESET_L 电源到CPU的主复位	IO_PMU_TO_SYSTEM_RESET_L	MAKE_BASE=TRUE 9
11	GND		
11	GND		
11	SUBUS_UAT_B	SUBUS_UAT_B	MAKE_BASE=TRUE 17
11	ANALOG_PP_CPU_PCORE_LVCC	ANALOG_PP_CPU_PCORE_LVCC	MAKE_BASE=TRUE 9
11	SUBUS_UAT_A	SUBUS_UAT_A	MAKE_BASE=TRUE 17
11	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 强制DFU信号	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	MAKE_BASE=TRUE 9
11	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	MAKE_BASE=TRUE 18
11	GND		
11	GND		
11	GND		
11	GND		
11	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GND		
11	PP1V2_S2	PP1V2_S2	MAKE_BASE=TRUE 17

RIGHT SIDE

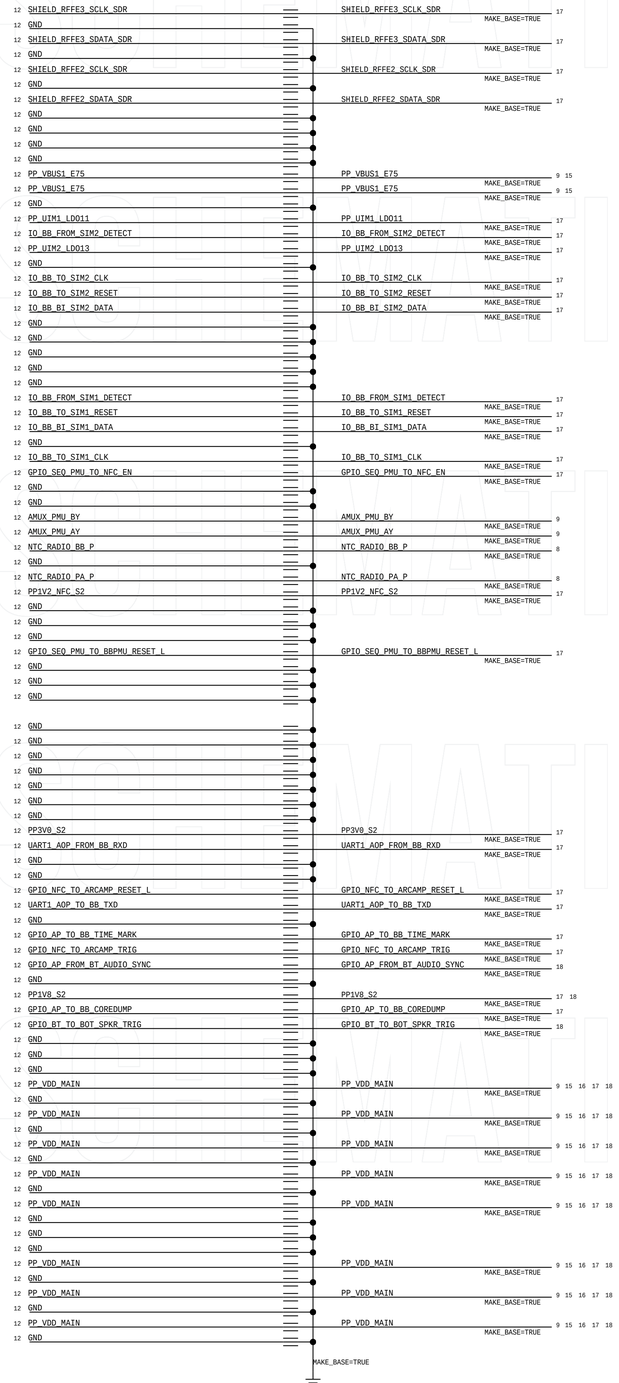
11	GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO_S4_PMU_TO_WLAN_REG_ON	MAKE_BASE=TRUE 18
11	GND		
11	GND		
11	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE	MAKE_BASE=TRUE 18
11	GND		
11	PP1V8_S4	PP1V8_S4	MAKE_BASE=TRUE 17 18
11	PP_1V8_LDO6	PP_1V8_LDO6	MAKE_BASE=TRUE 17
11	GND		
11	PP_APT_L_PA	PP_APT_L_PA	MAKE_BASE=TRUE 14 17
11	GND		
11	PP_APT_L_PA	PP_APT_L_PA	MAKE_BASE=TRUE 14 17
11	IO_TOUCH_TO_MANY_SCAN_ACTIVE	IO_TOUCH_TO_MANY_SCAN_ACTIVE	MAKE_BASE=TRUE 17
11	GND		MAKE_BASE=TRUE
11	GND		
11	SHIELD_ETDAC_QET1_N	SHIELD_ETDAC_QET1_N	MAKE_BASE=TRUE 17
11	GND		
11	SHIELD_ETDAC_QET1_P	SHIELD_ETDAC_QET1_P	MAKE_BASE=TRUE 17
11	GND		
11	SUBUS_LAT_A	SUBUS_LAT_A	MAKE_BASE=TRUE 17
11	GND		
11	SHIELD_RFFE8_SCLK_SDR	SHIELD_RFFE8_SCLK_SDR	MAKE_BASE=TRUE 17
11	GND		
11	SHIELD_RFFE8_SDATA_SDR	SHIELD_RFFE8_SDATA_SDR	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	50_RX_XCVR_PRX14_N79_RX_OUT1	50_RX_XCVR_PRX14_N79_RX_OUT1	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_RX_XCVR_PRX16_UHB_RX_OUT1	50_RX_XCVR_PRX16_UHB_RX_OUT1	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_TRX_UHB_PAD_PORTB_TX_M	50_TRX_UHB_PAD_PORTB_TX_M	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_TRX_UHB_PAD_N79_PORTB_TX_M	50_TRX_UHB_PAD_N79_PORTB_TX_M	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_TRX_UHB_PAD_N79_PORTB_TX_M	50_TRX_UHB_PAD_N79_PORTB_TX_M	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_RX_XCVR_PRX15_N79_RX_OUT2	50_RX_XCVR_PRX15_N79_RX_OUT2	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_TX_IN_XCVR_TX1_LB_JB	50_TX_IN_XCVR_TX1_LB_JB	MAKE_BASE=TRUE 17
11	50_TX_IN_XCVR_TX0_LB	50_TX_IN_XCVR_TX0_LB	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_RX_XCVR_PRX6_LB_A_RX0	50_RX_XCVR_PRX6_LB_A_RX0	MAKE_BASE=TRUE 17
11	50_RX_XCVR_PRX10_LB_PRX_OUT2	50_RX_XCVR_PRX10_LB_PRX_OUT2	MAKE_BASE=TRUE 17
11	GND		MAKE_BASE=TRUE
11	GND		
11	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_RX_XCVR_PRX17_UHB_RX_OUT2	50_RX_XCVR_PRX17_UHB_RX_OUT2	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	50_UHB_L_CPLR_OUT	50_UHB_L_CPLR_OUT	MAKE_BASE=TRUE 17
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND		
11	GND	

Interposer: Symbol 3 Aliases

LEFT SIDE



RIGHT SIDE



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Interposer: Symbol 4 Aliases

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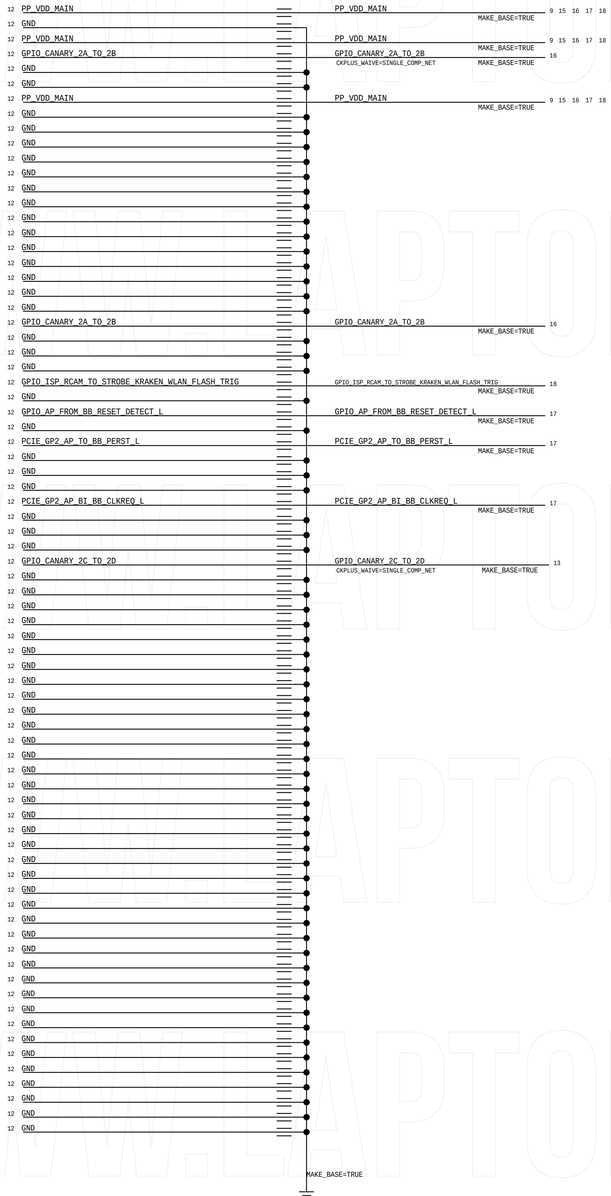
12 PP_VDD_MAIN
12 GND
12 PP_VDD_MAIN
12 GPIO_CANARY_2A_TO_2B
12 GND
12 GND
12 PP_VDD_MAIN
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GND
12 GPIO_CANARY_2A_TO_2B
12 GND
12 GND
12 GND
12 GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG
12 GND
12 GPIO_AP_FROM_BB_RESET_DETECT_L
12 GND
12 PCIE_GP2_AP_TO_BB_PERST_L
12 GND
12 GND
12 GND
12 PCIE_GP2_AP_BI_BB_CLKREQ_L
12 GND
12 GND
12 GND
12 GPIO_CANARY_2C_TO_2D
12 GND
12 GND
12 GND
12 GND
12 GND
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12 GND
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12 GND
12 GND
12 GND
12 GND

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POWER

55 21 18 17 16 15 9 PP_VDD_MAIN
22 15 PP_VDD_BOOST
26 14 PP1V2_S2
55 47 18 17 13 PP1V2_S4
48 18 15 PP1V8_S2
55 47 18 17 14 PP1V8_S4
30 15 PP3V0_S2
22 15 PP_VDD_RF_1V2
31 14 PP_1V8_LDO6
22 15 PP_UIM1_LDO11
22 15 PP_UIM2_LDO13

PCIE

26 14 90_PCIE_GP2_AP_TO_BB_TX_N
26 14 90_PCIE_GP2_AP_TO_BB_TX_P
26 14 90_PCIE_GP2_AP_FROM_BB_RX_N
26 14 90_PCIE_GP2_AP_FROM_BB_RX_P
26 14 90_PCIE_GP2_AP_TO_BB_REFCLK_N
26 14 90_PCIE_GP2_AP_TO_BB_REFCLK_P
26 14 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L
26 16 PCIE_GP2_AP_BI_BB_CLKREQ_L
26 16 PCIE_GP2_AP_TO_BB_PERST_L

I2S

26 14 I2S2_AP_TO_BB_DOUT
26 14 I2S2_AP_FROM_BB_DIN
26 14 I2S2_AP_FROM_BB_BCLK
26 14 I2S2_AP_FROM_BB_LRCLK

CONTROL

26 15 GPIO_AP_TO_BB_COREDUMP
23 15 GPIO_SEQ_PMU_TO_BBPMU_RESET_L
26 15 GPIO_AP_TO_BB_TIME_MARK CPU到基带时间标记信号
26 13 GPIO_AP_TO_BB_PEAK_PWR_IND
23 14 IO_TOUCH_TO_MANY_SCAN_ACTIVE
23 14 GPIO_AOP_TO_BB_FORCE_PWM CPU到基带强制调节信号
26 14 GPIO_BB_TO_ALS_GSM_BURST_IND_1V8
26 16 GPIO_AP_FROM_BB_RESET_DETECT_L

R13810
13 CLK_BBPMU_TO_DOTARA_38M4 — 1 33.2 2 — CLK_BBPMU_TO_DOTARA_38M4_R 17 23
1% 1/32W MF 01005
ROOM=BBPMU

SWD

26 13 SWD_AP_TO_MANY_SWCLK CPU输出的SWD总线时钟
26 13 SWD_AP_BI_BB_SWDIO CPU到基带的SWD总线数据

DOTARA

23 14 GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA
23 17 CLK_BBPMU_TO_DOTARA_38M4_R

AOP UART

26 15 UART1_AOP_TO_BB_TXD
26 15 UART1_AOP_FROM_BB_RXD

WLAN UART/RFFE

26 18 UART_BB_TO_WLAN_RX
26 18 UART_BB_TO_WLAN_TX
47 18 14 SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
47 18 13 SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA

R1

26 13 GPIO_BB_TO_R1_CH9_REQ
26 13 GPIO_BB_TO_R1_COEX
26 13 GPIO_R1_TO_BB_CH9_COEX
26 13 GPIO_R1_TO_BB_LAA_SW_CTRL

NFC

23 14 CLK_BBPMU_TO_NFC_38M
23 14 GPIO_NFC_TO_BBPMU_CLK_EN

SIM

26 15 IO_BB_TO_SIM1_CLK
26 15 IO_BB_BI_SIM1_DATA
26 15 IO_BB_FROM_SIM1_DETECT
26 15 IO_BB_TO_SIM1_RESET
26 15 IO_BB_TO_SIM2_CLK
26 15 IO_BB_BI_SIM2_DATA
26 15 IO_BB_FROM_SIM2_DETECT
26 15 IO_BB_TO_SIM2_RESET

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ET/APT IC

PP_APT_L_PA — PP_APT_L_PA 14 33
SHIELD_ETDAC_QET1_P — SHIELD_ETDAC_QET1_P 14 29
SHIELD_ETDAC_QET1_N — SHIELD_ETDAC_QET1_N 14 29

RF RFFE

SHIELD_RFFE1_SCLK_SDR — SHIELD_RFFE1_SCLK_SDR 15 30
SHIELD_RFFE1_SDATA_SDR — SHIELD_RFFE1_SDATA_SDR 15 30
SHIELD_RFFE2_SCLK_SDR — SHIELD_RFFE2_SCLK_SDR 15 30
SHIELD_RFFE2_SDATA_SDR — SHIELD_RFFE2_SDATA_SDR 15 30
SHIELD_RFFE3_SCLK_SDR — SHIELD_RFFE3_SCLK_SDR 15 30
SHIELD_RFFE3_SDATA_SDR — SHIELD_RFFE3_SDATA_SDR 15 30
SHIELD_RFFE5_SCLK_SDR — SHIELD_RFFE5_SCLK_SDR 13 30
SHIELD_RFFE5_SDATA_SDR — SHIELD_RFFE5_SDATA_SDR 13 30
SHIELD_RFFE8_SCLK_SDR — SHIELD_RFFE8_SCLK_SDR 14 30
SHIELD_RFFE8_SDATA_SDR — SHIELD_RFFE8_SDATA_SDR 14 30

LB PAD

50_TX_IN_XCVR_TX1_LB_JB — 50_TX_IN_XCVR_TX1_LB_JB 14 30
50_TX_IN_XCVR_TX0_LB — 50_TX_IN_XCVR_TX0_LB 14 30
50_RX_XCVR_PRX6_LB_A_RX0 — 50_RX_XCVR_PRX6_LB_A_RX0 14 30
50_RX_XCVR_PRX10_LB_PRX_OUT2 — 50_RX_XCVR_PRX10_LB_PRX_OUT2 14 30
50_TRX_LB_PORTB_RX1_M — 50_TRX_LB_PORTB_RX1_M 15 36
50_TRX_LB_PORTB_TX_M — 50_TRX_LB_PORTB_TX_M 15 36
50_TRX_IN_LMB_PAD_2G_LB_OUT_M — 50_TRX_IN_LMB_PAD_2G_LB_OUT_M 15 35

UHB PA

50_RX_XCVR_PRX14_N79_RX_OUT1 — 50_RX_XCVR_PRX14_N79_RX_OUT1 14 30
50_RX_XCVR_PRX15_N79_RX_OUT2 — 50_RX_XCVR_PRX15_N79_RX_OUT2 14 30
50_RX_XCVR_PRX16_UHB_RX_OUT1 — 50_RX_XCVR_PRX16_UHB_RX_OUT1 14 30
50_RX_XCVR_PRX17_UHB_RX_OUT2 — 50_RX_XCVR_PRX17_UHB_RX_OUT2 14 30
50_TX_IN_TX2_UHB_PAD_TX_N79_IN — 50_TX_IN_TX2_UHB_PAD_TX_N79_IN 14 30
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 — 50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 14 30
50_UHB_L_CPLR_OUT — 50_UHB_L_CPLR_OUT 14 30

LAA

50_TRX_WLAN_G_BT_ANT4_NPLXR — 50_TRX_WLAN_G_BT_ANT4_NPLXR 18 45
50_LAA_RX_XCVR_DRX10 — 50_LAA_RX_XCVR_DRX10 13 30
50_LAA_RX_XCVR_PRX12 — 50_LAA_RX_XCVR_PRX12 15 30

LAT

LAT_SUBUS_A — SUBUS_LAT_A 14 48
LAT_SUBUS_B — SUBUS_LAT_B 15 48
LAT_SUBUS_C — SUBUS_LAT_C 15 48
50_CPLR_L_CPL1_LAT_OUT — 50_CPLR_L_CPL1_LAT_OUT 15 30
50_TRX_HB_PAD_ANT1 — 50_TRX_HB_PAD_ANT1 15 34
50_TRX_HB_PAD_ANT2_M — 50_TRX_HB_PAD_ANT2_M 15 34
50_TRX_L5_LNA_IN — 50_TRX_L5_LNA_IN 15 43

UAT

UAT_SUBUS_A — SUBUS_UAT_A 14 47
UAT_SUBUS_B — SUBUS_UAT_B 14 47
UAT_TUNER_TO_R1_STATE — UAT_TUNER_TO_R1_STATE 13 47
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M — 50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M 13 44
50_TRX_ANT2_LB_LMB_MB_HB_L1 — 50_TRX_ANT2_LB_LMB_MB_HB_L1
50_TRX_ANT4_MB_HB_WLAN24 — 50_TRX_ANT4_MB_HB_WLAN24 13 45
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M — 50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M 13 38
50_TRX_UHB_PAD_N79_PORTB_TX_M — 50_TRX_UHB_PAD_N79_PORTB_TX_M 14 38
50_TRX_UHB_PAD_PORTB_TX_M — 50_TRX_UHB_PAD_PORTB_TX_M 14 38

POWER

55 21 18 17 16 15 9 PP_VDD_MAIN
55 47 18 17 14 PP1V8_S4
55 47 18 17 13 PP1V2_S4
55 15 PP1V2_NFC_S2

CONTROL

55 15 GPIO_SEQ_PMU_TO_NFC_EN

NFC I2C

55 13 I2C_R1_TO_NFC_SCL
55 13 I2C_R1_TO_NFC_SDA
55 18 I2C_BT_TO_NFC_SCL
55 18 I2C_BT_TO_NFC_SDA

NFC RF

56 13 NFC_P_ANT_POS
56 13 NFC_P_ANT_NEG

NFC SPMI

55 18 13 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
55 17 SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R

MISC

55 18 GPIO_SE_TO_BT_PKT_RDY
55 13 NTC_STOCKHOLM
NC
55 15 GPIO_NFC_TO_ARCAMP_RESET_L
55 15 GPIO_NFC_TO_ARCAMP_TRIG
55 13 NFC_P_TEST_OUT
55 13 GPIO_NFC_F_NFC_P_SYNC1
55 13 GPIO_NFC_F_NFC_P_SYNC2
55 13 IO_TOUCH_TO_MANY_SCAN_ACTIVE_U

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POWER

PP_VDD_MAIN
PP1V8_S4
PP1V2_S4
PP1V2_NFC_P_S2

CONTROL

PMU_TO_NFC_P_EN

NFC I2C

I2C_R1_TO_SE_SCL
I2C_R1_TO_SE_SDA
I2C_BT_TO_NFC_P_SCL
I2C_BT_TO_NFC_P_SDA

NFC RF

NFC_P_ANT_POS
NFC_P_ANT_NEG

NFC SPMI

SPMI_AOP_TO_RADIOS_CLK
SPMI_AOP_TO_RADIOS_DATA

MISC

IO_SE_TO_BT_PKT_READY
NFC_P_THERMISTOR_UAT2
NFC_P_THERMISTOR_UAT4
NFC_P_TO_ARC_RESET_L
NFC_P_TO_ARC_TRIG
NFC_P_TEST_OUT
NFC_F_TO_NFC_P_COEX
NFC_P_TO_NFC_F_COEX
TOUCH_TO_NFC_SCAN_ACTIVE

ROOM=NFC
18 13 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA — R13800 33.2 1% 1/32W MF 01005 — SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R 17 55
CPU到基带NFC的SPMI总线数据

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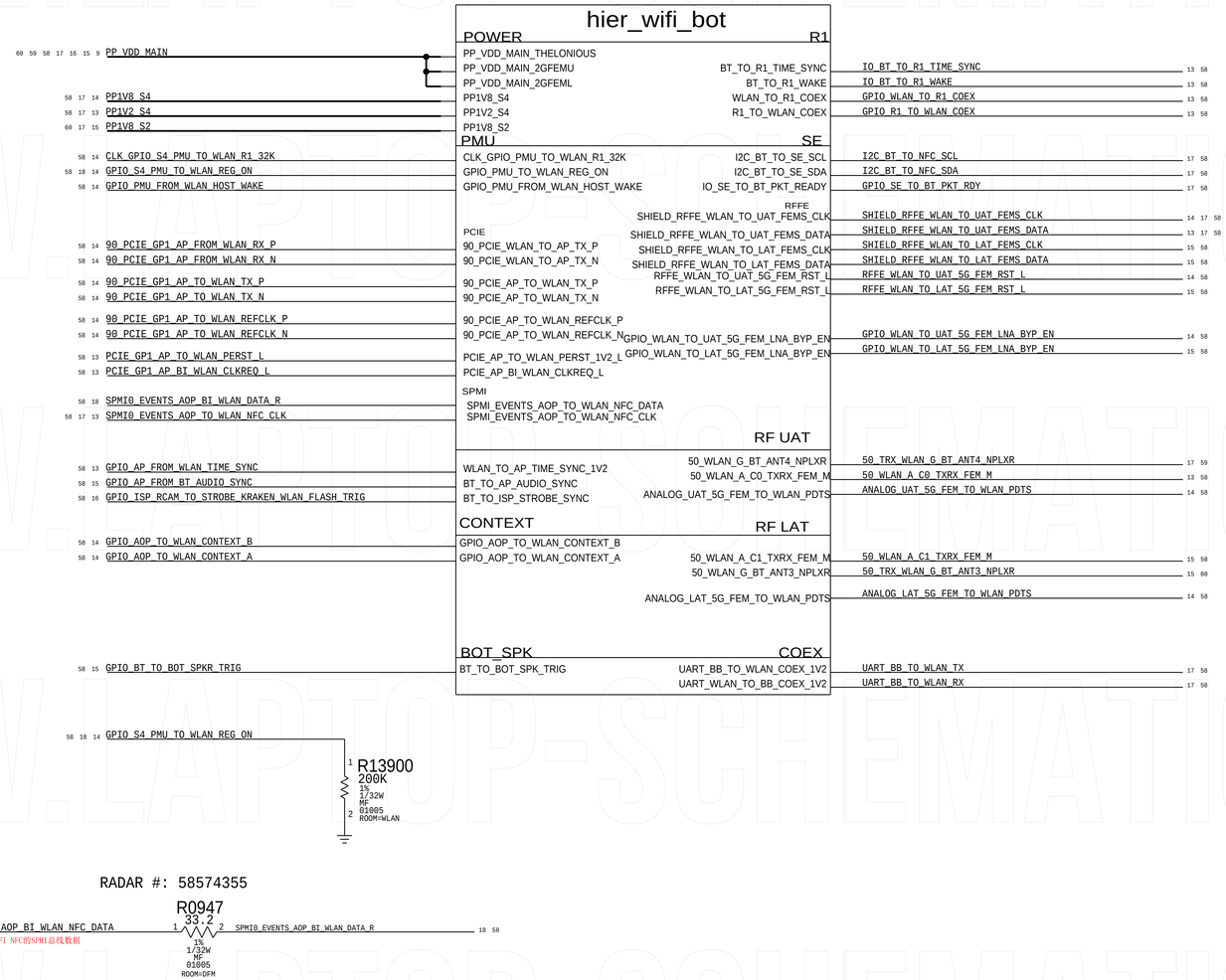
HIERARCHIES



60 59 58 17 16 15 9 PP_VDD_MAIN

58 17 14 PP1V8_S4
58 17 13 PP1V2_S4
60 17 15 PP1V8_S2

58 14 CLK_GPIO_S4_PMU_TO_WLAN_R1_32K
58 18 14 GPIO_S4_PMU_TO_WLAN_REG_ON
58 14 GPIO_PMU_FROM_WLAN_HOST_WAKE

58 14 90_PCIE_GP1_AP_FROM_WLAN_RX_P
58 14 90_PCIE_GP1_AP_FROM_WLAN_RX_N

58 14 90_PCIE_GP1_AP_TO_WLAN_TX_P
58 14 90_PCIE_GP1_AP_TO_WLAN_TX_N

58 14 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
58 14 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N

58 13 PCIE_GP1_AP_TO_WLAN_PERST_L
58 13 PCIE_GP1_AP_BI_WLAN_CLKREQ_L

58 18 SPMI0_EVENTS_AOP_BI_WLAN_DATA_R
58 17 13 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK

58 13 GPIO_AP_FROM_WLAN_TIME_SYNC
58 15 GPIO_AP_FROM_BT_AUDIO_SYNC
58 16 GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG

58 14 GPIO_AOP_TO_WLAN_CONTEXT_B
58 14 GPIO_AOP_TO_WLAN_CONTEXT_A

58 15 GPIO_BT_TO_BOT_SPKR_TRIG

BT_TO_R1_TIME_SYNC — IO_BT_TO_R1_TIME_SYNC 13 58
BT_TO_R1_WAKE — IO_BT_TO_R1_WAKE 13 58
WLAN_TO_R1_COEX — GPIO_WLAN_TO_R1_COEX 13 58
R1_TO_WLAN_COEX — GPIO_R1_TO_WLAN_COEX 13 58

I2C_BT_TO_SE_SCL — I2C_BT_TO_NFC_SCL 17 58
I2C_BT_TO_SE_SDA — I2C_BT_TO_NFC_SDA 17 58
IO_SE_TO_BT_PKT_READY — GPIO_SE_TO_BT_PKT_RDY 17 58

SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK — SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK 14 17 58
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA — SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA 13 17 58
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK — SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK 15 58
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA — SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA 15 58
RFFE_WLAN_TO_UAT_5G_FEM_RST_L — RFFE_WLAN_TO_UAT_5G_FEM_RST_L 14 58
RFFE_WLAN_TO_LAT_5G_FEM_RST_L — RFFE_WLAN_TO_LAT_5G_FEM_RST_L 15 58

GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN — GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN 14 58
GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN — GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN 15 58

50_WLAN_G_BT_ANT4_NPLXR — 50_TRX_WLAN_G_BT_ANT4_NPLXR 17 59
50_WLAN_A_C0_TXRX_FEM_M — 50_WLAN_A_C0_TXRX_FEM_M 13 58
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS — ANALOG_UAT_5G_FEM_TO_WLAN_PDTS 14 58

50_WLAN_A_C1_TXRX_FEM_M — 50_WLAN_A_C1_TXRX_FEM_M 15 58
50_WLAN_G_BT_ANT3_NPLXR — 50_TRX_WLAN_G_BT_ANT3_NPLXR 15 60
ANALOG_LAT_5G_FEM_TO_WLAN_PDTS — ANALOG_LAT_5G_FEM_TO_WLAN_PDTS 14 58

UART_BB_TO_WLAN_COEX_1V2 — UART_BB_TO_WLAN_TX 17 58
UART_WLAN_TO_BB_COEX_1V2 — UART_BB_TO_WLAN_RX 17 58

58 18 14 GPIO_S4_PMU_TO_WLAN_REG_ON

R13900
200K
1%
1/32W
MF
01005
ROOM=WLAN

RADAR #: 58574355

17 13 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA

R0947
33.2
1%
1/32W
MF
01005
ROOM=DFM

CPU到蓝牙WIFI NFC的SPMI总线数据

SPMI0_EVENTS_AOP_BI_WLAN_DATA_R 18 58

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

MAV20 HIER_RADIO_MAV_BOT

LAST_MODIFICATION=Wed Jul 1 15:22:37 2020

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POWER

PP_VDD_MAIN IN 3 5 13 14 15 31 32 34
PP_VDD_BOOST VOLTAGE=4.5 IN 4 16 17 19 20 23 31 32
PP1V2_S2 IN 8
PP1V2_S4 IN 29
PP1V8_S2 IN 30 32
PP1V8_S4 IN 29
PP3V0_S2 IN 12 31 32
PP_1V8_LDO6 OUT 4 13 14 15 16 17 18 19 20 21 22 29
PP_VDD_RF_1V2 OUT 4 16 17 18 19 20 21 22 24 25

PCIE

GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L OUT 8 31 32
PCIE_GP2_AP_TO_BB_PERST_L IN 8 31
PCIE_GP2_AP_BI_BB_CLKREQ_L IO 8 31 32
90_PCIE_GP2_AP_FROM_BB_RX_P OUT 8 31
90_PCIE_GP2_AP_FROM_BB_RX_N OUT 8 31
90_PCIE_GP2_AP_TO_BB_TX_P IN 8 31
90_PCIE_GP2_AP_TO_BB_TX_N IN 8 31
90_PCIE_GP2_AP_TO_BB_REFCLK_P OUT 8 31
90_PCIE_GP2_AP_TO_BB_REFCLK_N OUT 8 31

SIM

PP_UIM1_LDO11 OUT 4 6 28 31
IO_BB_TO_SIM1_RESET OUT 8 31
IO_BB_BI_SIM1_DATA IO 8 28 31
IO_BB_TO_SIM1_CLK OUT 8 31
IO_BB_FROM_SIM1_DETECT OUT 8 28 31

PP_UIM2_LDO13 OUT 4 6 28 31
IO_BB_TO_SIM2_RESET OUT 8
IO_BB_BI_SIM2_DATA IO 8 28
IO_BB_TO_SIM2_CLK OUT 8
IO_BB_FROM_SIM2_DETECT OUT 8 28

I2S

I2S2_AP_FROM_BB_DIN OUT 8 31
I2S2_AP_TO_BB_DOUT IN 8 31
I2S2_AP_FROM_BB_BCLK OUT 8 31
I2S2_AP_FROM_BB_LRCLK OUT 8 31

CONTROL

GPIO_AP_FROM_BB_RESET_DETECT_L OUT 8 31
GPIO_SEQ_PMU_TO_BBPMU_RESET_L IN 5 31 32
GPIO_AP_TO_BB_COREDUMP IN 8 31
GPIO_BB_TO_ALS_GSM_BURST_IND_1V8 OUT 8 31
IO_TOUCH_TO_MANY_SCAN_ACTIVE IN 5 31
GPIO_AOP_TO_BB_FORCE_PWM IN 5 31
GPIO_AP_TO_BB_TIME_MARK IN 8 31
GPIO_AP_TO_BB_PEAK_PWR_IND IN 8 31

SWD

SWD_AP_TO_MANY_SWCLK CPU输出的SWD总线时钟 IO 29
SWD_AP_BI_BB_SWDIO CPU到基带的SWD总线数据 IO 29

DOTARA

GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA IN 5 31
CLK_BBPMU_TO_DOTARA_38M4_R OUT 5 31

AOP UART

UART1_AOP_TO_BB_TXD IN 8 31
UART1_AOP_FROM_BB_RXD OUT 8 31

WLAN UART/RFFE

UART_BB_TO_WLAN_TX OUT 8 31
UART_BB_TO_WLAN_RX IN 8 31
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK IN 29
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA IO 29

R1

GPIO_BB_TO_R1_COEX OUT 8 31
GPIO_BB_TO_R1_CH9_REQ OUT 8 31
GPIO_R1_TO_BB_CH9_COEX IN 8 31
GPIO_R1_TO_BB_LAA_SW_CTRL IN 8 31

NFC

CLK_BBPMU_TO_NFC_38M OUT 5 31
GPIO_NFC_TO_BBPMU_CLK_EN IN 5 31

ET/APT IC

SHIELD_ETDAC_QET1_P OUT 11
SHIELD_ETDAC_QET1_N OUT 11
SHIELD_RFFE8_SDATA_SDR IO 1 12 31
SHIELD_RFFE8_SCLK_SDR OUT 1 12 31
PP_APT_L_PA VOLTAGE=5.5 OUT 15

RF RFFE

SHIELD_RFFE1_SCLK_SDR OUT 12 13 16 17 31
SHIELD_RFFE1_SDATA_SDR IO 12 13 16 17 31
SHIELD_RFFE2_SCLK_SDR OUT 12 15 31
SHIELD_RFFE2_SDATA_SDR IO 12 15 31
SHIELD_RFFE3_SCLK_SDR OUT 12 16 17 21 31
SHIELD_RFFE3_SDATA_SDR IO 12 16 17 21 31
SHIELD_RFFE5_SCLK_SDR OUT 12 18 19 20 22 31
SHIELD_RFFE5_SDATA_SDR IO 12 18 19 20 22 31
SHIELD_RFFE8_SDATA_SDR IO 1 12 31
SHIELD_RFFE8_SCLK_SDR OUT 1 12 31

LB PAD

50_TX_IN_XCVR_TX1_LB_JB OUT 12
50_TX_IN_XCVR_TX0_LB OUT 12
50_RX_XCVR_PRX6_LB_A_RX0 IN 12
50_RX_XCVR_PRX10_LB_PRX_OUT2 IN 12
50_TRX_LB_PORTB_RX1_M IN 18
50_TRX_LB_PORTB_TX_M IO 18
50_TRX_IN_LMB_PAD_2G_LB_OUT_M IO 17

UHB PA (LAT)

50_RX_XCVR_PRX14_N79_RX_OUT1 IN 12
50_RX_XCVR_PRX15_N79_RX_OUT2 IN 12
50_RX_XCVR_PRX16_UHB_RX_OUT1 IN 12
50_RX_XCVR_PRX17_UHB_RX_OUT2 IN 12
50_TX_IN_TX2_UHB_PAD_TX_N79_IN OUT 12
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 OUT 12
50_UHB_L_CPLR_OUT IN 12
50_TRX_UHB_PAD_PORTB_TX_M OUT 20
50_TRX_UHB_PAD_N79_PORTB_TX_M OUT 20

LAA

50_TRX_WLAN_G_BT_ANT4_NPLXR IO 27
50_LAA_RX_XCVR_DRX10 IN 12
50_LAA_RX_XCVR_PRX12 IN 12

LAT

SUBUS_LAT_A OUT 30
SUBUS_LAT_B OUT 30
SUBUS_LAT_C OUT 30

50_TRX_HB_PAD_ANT1 OUT 16
50_CPLR_L_CPL1_LAT_OUT IN 12
50_TRX_L5_LNA_IN IN 25
50_TRX_HB_PAD_ANT2_M OUT 16

UAT

SUBUS_UAT_A OUT 29
SUBUS_UAT_B OUT 29

UAT_TUNER_TO_R1_STATE OUT 29

50_TRX_ANT2_LB_LMB_MB_HB_L1 OUT 23
50_TRX_ANT4_MB_HB_WLAN24 OUT 27
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M IO 26
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M IO 20

SCH #: 951-11455

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BOM TABLES AND CONSTRAINTS

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ALT TABLES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00250	197S00249	?	Y601_E	TXC,38.4MHZ,8PF,1612

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01228	152S01120	?	L405_E	SEMCO,1.0UH,3.4A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00013	335S0894	?	EEPROM_E	EEPROM,8KBIT,I2C

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339M00113	339S00112	?	U_TAN_E	MODULE,ES2.3,U,LGA388

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339M00115	339M00116	?	U_BG1_E	ANT,ES3.1,USI,LGA376

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00050	1	RES,MF,5.6K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:WW+KOLKATA
118S0730	1	RES,MF,12K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:NAJP
118S00088	1	RES,MF,19.1K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:ROW
118S00122	1	RES,MF,27K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:NAMM
353S02396	1	IC,LB DSM,WW,MCD,LMRXFNJB-K79,DSLGA20	DSM_LB_E	CRITICAL	RF_SKU:NAJP&RF_SKU:NAMM
353S02397	1	IC,LB DSM,ROW,MCD,LMRXFNJB-K83,DSLGA20	DSM_LB_E	CRITICAL	RF_SKU:ROW
353S02393	1	IC,2G-LMB PAD,SKYS8232,DSBGA79	PA_LMB_E	CRITICAL	RF_SKU:NAJP
353S02401	1	IC,2G-LMB PAD,ROW,SKYS8242,DSBGA79	PA_LMB_E	CRITICAL	RF_SKU:ROW&RF_SKU:NAMM
353S02391	1	IC,HB TX DSM,WW,HFQTWLQFA-580,DSLGA61	DSM_HB_E	CRITICAL	RF_SKU:NAJP
353S02392	1	IC,HB TX DSM,ROW,HFQTWLQFA-583,DSLGA61	DSM_HB_E	CRITICAL	RF_SKU:ROW&RF_SKU:NAMM
118S00122	1	RES,MF,27K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:PROTO2
118S00193	1	RES,MF,36.5K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:EVT
118S0868	1	RES,MF,47.5K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:CRB
118S00136	1	RES,TK,60.4K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:DVT
118S0768	1	RES,MF,75K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:PVT
118S0688	1	RES,MF,143K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:EVT_DOE

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BB PMU: SMPS

SMPS INPUT CAPS

PP_VDD_MAIN
MAKE_BASE=TRUE

C401_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU — GND
C406_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU — MAKE_BASE=TRUE
C402_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU — GND, MAKE_BASE=TRUE
C405_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU — GND, MAKE_BASE=TRUE
C412_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU — GND, MAKE_BASE=TRUE
C407_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU — GND, MAKE_BASE=TRUE
C427_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU — GND
C403_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BBPMU — MAKE_BASE=TRUE
C404_E 2.2UF 20% 6.3V X5R-CERM — GND, MAKE_BASE=TRUE

SHARE S7 INPUT POWER ROUTES WITH S5 CAP

C411_E 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=BBPMU

PART_NUMBER=338S00620
ROOM=BBPMU

UBBPMU_E
PMX55-0
FOWPSP
SYM 3 OF 6
CRITICAL

GND	112	GND_S1	
GND	121	GND_S1	
GND	42	GND_S2	
GND	43	GND_S2	
GND	119	GND_S3	
GND	127	GND_S3	
GND	110	GND_S4	
GND	111	GND_S4	
GND	27	GND_S5	
GND	28	GND_S5	
GND	103	GND_S6	
GND	104	GND_S6	
GND	13	GND_S7	
	21	GND_S7	
	35	GND_S8	
	36	GND_S8	
	47	CMN_GND	
	56	CMN_GND	
	64	CMN_GND	
	65	CMN_GND	
	73	CMN_GND	
	81	CMN_GND	
	82	CMN_GND	
	90	CMN_GND	
VREG_S1_S6_SENSE_N	96	RMT_GND_S1	
	88	RMT_GND_S6	
	79	RMT_GND_S8	
	108	AVDD_BYP	AVDD_BYP_PMIC
	116	DVDD_BYP	DVDD_BYP_PMIC

C408_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BBPMU — DVDD_BYP_GND
C410_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BBPMU — AVDD_BYP_GND
XW408_E SHORT-10L-0.1MM-SM ROOM=BBPMU
XW406_E SHORT-10L-0.1MM-SM ROOM=BBPMU

PMX_REF_BYP — C509_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=BBPMU — PMX_REF_BYP_GND
XW407_E SHORT-10L-0.1MM-SM ROOM=BBPMU

PART_NUMBER=338S00620
ROOM=BBPMU

UBBPMU_E
PMX55-0
FOWPSP
SYM 5 OF 6
VREG1
CRITICAL

	32	REF_BYP	PMX_REF_BYP
	49	REF_GND	PMX_REF_BYP_GND
PP_VDD_MAIN	137	VDD_S1	
	138		
PP_VDD_MAIN	59	VDD_S2	
	68		
PP_VDD_MAIN	144	VDD_S3	
	145		
PP_VDD_MAIN	76	VDD_S4	
	77		
	85		
PP_VDD_MAIN	1	VDD_S5	
	10		
PP_VDD_MAIN	78	VDD_S6	
	87		
PP_VDD_MAIN	3	VDD_S7	
	11		
NC	61	VDD_S8	
NC	69		

VSW_S1	120	VSW_SMPS1	L401_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM ROOM=BBPMU — VOLTAGE=0.752V IPEAK: 7.8A — PP_0V75_SMPS1_6
	129		
VFB_S1	70	VREG_S1_S6_SENSE_P	REMOTE SENSE CONNECT TO LOAD
VSW_S2	51	VSW_SMPS2	L402_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM ROOM=BBPMU — VOLTAGE=1.224V IPEAK: 3.19A — PP_1V22_SMPS2
	60		
VFB_S2	34	PP_1V24_SMPS2_SNS	XW404_E SHORT-10L-0.1MM-SM ROOM=BBPMU — C429_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BBPMU — GND
VSW_S3	128	VSW_SMPS3	L403_E 152S01273 0.47UH-20%-4.8A-0.027OHM MCFE2016-SM-1 ROOM=BBPMU — VOLTAGE=0.824V IPEAK: 3.59A — PP_0V82_SMPS3 — 基带电源输出的0.82V S3供电
	136		
VFB_S3	126	PP_0V82_SMPS3_SNS	XW402_E SHORT-10L-0.1MM-SM ROOM=BBPMU — C430_E 20UF 20% 4V X5R 0402-0.1MM — C434_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BBPMU — GND
VSW_S4	93	VSW_SMPS4	L404_E 152S01120 1.0UH-3.4A-0.053OHM PIJF2016FE-SM ROOM=BBPMU — VOLTAGE=1.88V IPEAK: 0.903A — PP_1V9_SMPS4 — 基带电源输出的1.9V S4供电
	94		
	102		
VFB_S4	135	PP_1V9_SMPS4_SNS	XW403_E SHORT-10L-0.1MM-SM ROOM=BBPMU — C431_E 20UF 20% 4V X5R 0402-0.1MM — C409_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BBPMU — GND
VSW_S5	18	VSW_SMPS5	L405_E 152S01120 1.0UH-3.4A-0.053OHM PIJF2016FE-SM ROOM=BBPMU — VOLTAGE=0.752V IPEAK: 2.39A — PP_0V75_SMPS5 — 基带电源输出的0.75V S5供电
	19		
VFB_S5	45	PP_0V75_SMPS5_SNS	XW405_E SHORT-10L-0.1MM-SM ROOM=BBPMU — C432_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BBPMU — GND
VSW_S6	86	VSW_SMPS6	L406_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM ROOM=BBPMU — PP_0V75_SMPS1_6
	95		
VFB_S6	62	VREG_S1_S6_SENSE_P	REMOTE SENSE CONNECT TO LOAD
VSW_S7	4	VSW_SMPS7	L407_E 152S01273 0.47UH-20%-4.8A-0.027OHM MCFE2016-SM-1 ROOM=BBPMU — VOLTAGE=0.752V IPEAK: 3.05A — PP_0V75_SMPS7 — 基带电源输出的0.75V S7供电
	12		
VFB_S7	20	PP_0V75_SMPS7_SNS	XW401_E SHORT-10L-0.1MM-SM ROOM=BBPMU — C433_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BBPMU — C435_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BBPMU — GND
VSW_S8	44	NC	
	52	NC	
VFB_S8	53	NC	

S8 FOR BACKUP ONLY
NOT ENOUGH ROOM ON MLB

1-Main (Alimentacion)
2-PMU to PMURF (encendido)
Reset L

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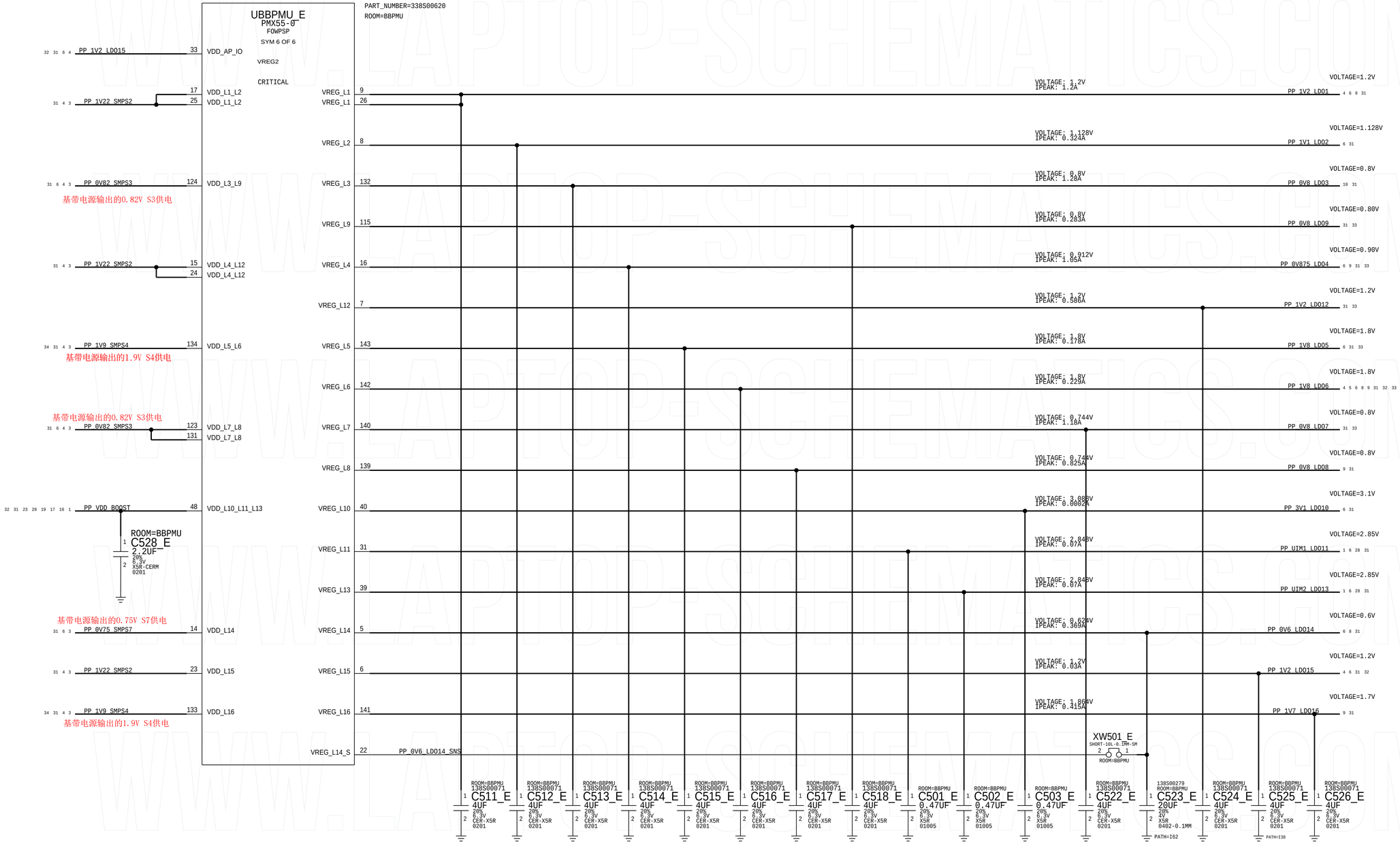
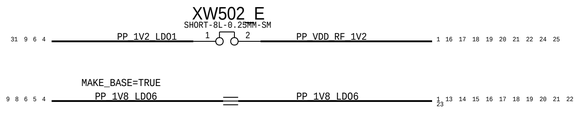
BB PMU: LDOS





PMX55 LDO CAPACITOR TABLE
N1200 (L1, L2, L3, L4, L7, L8, L9, L12, L14, L15) 4.7UF MIN, 22UF MAX N1200 (L14) 2X10UF OR 1X22UF MIN, 44UF MAX
MVP150 (L10, L11, L13) 0.47UF MIN, 5UF MAX
LVP600 (L5, L6, L16) 4.7UF MIN, 23.5UF MAX

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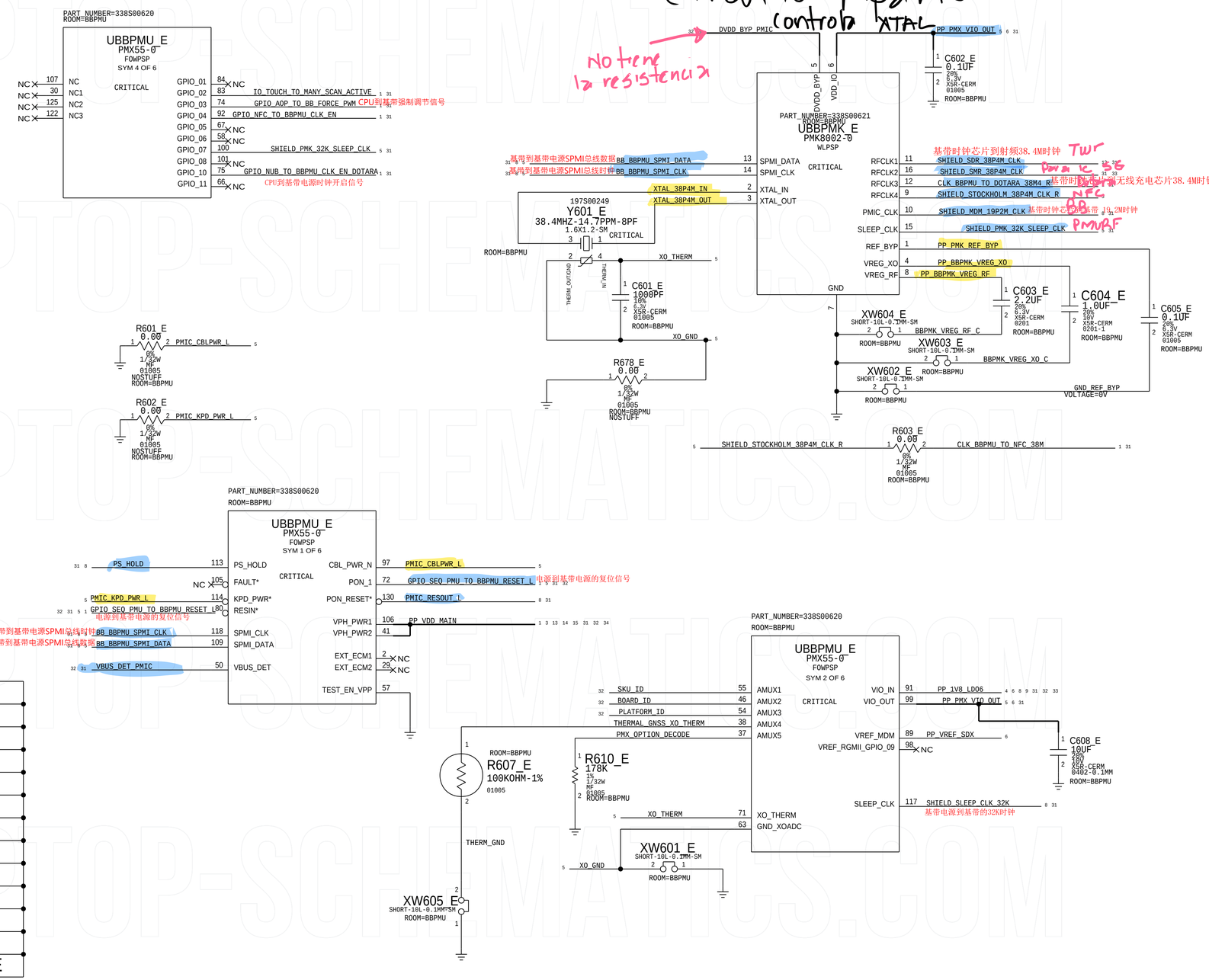
BB PMU: XTAL, CLK, ANALOG, IO

BOARD_ID	APN	R631_E	MLB/RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	PROTO0/DEV1	0X01
0.15V-0.25V	118S0730	12.0K	PROTO1/DEV2	0X02
0.25V-0.35V	118S00088	19.1K	PROTO1.5/DEV3	0X03
0.35V-0.45V	118S00122	27.0K	PROTO2/DEV4	0X04
0.45V-0.55V	118S00193	36.5K	EVT/DEV5	0X05
0.55V-0.65V	118S0868	47.5K	CARRIER/DEV6	0X06
0.65V-0.75V	118S0136	60.4K	DVT/DEV7	0X07
0.75V-0.85V	118S0768	75.0K	PVT	0X08
0.85V-0.95V	118S0626	100K	SPARE	0X09
0.95V-1.05V	118S0737	124K	SPARE	0X0A
1.05V-1.15V	118S0688	143K	EVT_DOE	0X0B
1.15V-1.25V	TBD	TBD	SPARE	SPARE

PLATFORM_ID	APN	R632_E	MLB/RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	RADIO_DEV	0X1
0.15V-0.25V	118S0730	12.0K	DARWIN_FX	0X2
0.25V-0.35V	118S00088	19.1K	DARWIN_PG	0X3
0.35V-0.45V	118S00122	27.0K	RESERVED	0X4
0.45V-0.55V	118S00193	36.5K	MAV20.1	0X5
0.55V-0.65V	118S0868	47.5K	MAV20.2	0X6
0.65V-0.75V	118S0136	60.4K	RESERVED	0X7
0.75V-0.85V	118S0768	75.0K	RESERVED	0X8
0.85V-0.95V	118S0626	100K	RESERVED	0X9
0.95V-1.05V	118S0737	124K	RESERVED	0XA
1.05V-1.15V	118S0688	143K	DEV_BEERPONG	0XB
1.15V-1.25V	TBD	TBD	SPARE	SPARE

SKU_ID	APN	R630_E	MLB/RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	WW+KOLKATA	0X1
0.15V-0.25V	118S0730	12.0K	NAJP	0X2
0.25V-0.35V	118S00088	19.1K	ROW	0X3
0.35V-0.45V	118S00122	27.0K	NAMM	0X4
0.45V-0.55V	118S00193	36.5K	SPARE	0X5
0.55V-0.65V	118S0868	47.5K	SPARE	0X6
0.65V-0.75V	118S0136	60.4K	SPARE	0X7
0.75V-0.85V	118S0768	75.0K	SPARE	0X8
0.85V-0.95V	118S0626	100K	SPARE	0X9
0.95V-1.05V	118S0737	124K	SPARE	0XA
1.05V-1.15V	118S0688	143K	SPARE	0XB
1.15V-1.25V	TBD	TBD	SPARE	SPARE



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BB: PDN

PART_NUMBER=337S00865 ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 5 OF 8
PWR
CRITICAL

基带电源输出的0.75V S5供电
31 6 3 PP_0V75_SMPS5

VDDCX: AA29 AB12 AB14 AB16 AC11 AC13 AC15 AC17 AC19 AC21 AC23 AC25 AC27 AC29 AC9 AD18 AD20 AD22 AD26 W29

基带电源输出的0.75V S7供电
31 6 4 3 PP_0V75_SMPS7

VDDMX: AB10 AB22 AB24 AB8 AD24 AE25 G23 G25 G27 H10 H8 K16 K18 L25 L27 M8 P28 P8 R19 R21 T14 T16 T28 T8 U21 U23 W13 W15 W19 W21

VDD_MODEM: AA19 AA27 G21 H12 H14 H16 H18 H20 H22 H24 H26 H28 J11 J9 L11 L13 L15 L17 L19 L21 L23 L9 M10 M12 M14 M16 M18 M20 M22 M24 M26 M28 R11 R13 R15 R17 R23 R25 R27 R9 T10 T12 T18 T20 T22 T24 T26 W11 W17 W23 W25 W27 W5 W9 Y10 Y12 Y14 Y16 Y18 Y20 Y22 Y24 Y26 Y28 Y4 Y6 Y8

3 PP_0V75_SMPS1_6

C761_E 20UF 20% 4V X5R 0402-0.1MM
C762_E 20UF 20% 4V X5R 0402-0.1MM
C763_E 20UF 20% 4V X5R 0402-0.1MM
C764_E 20UF 20% 4V X5R 0402-0.1MM
138S00279 ROOM=BASEBAND

XW701_E SHORT-10L-0.1MM-SM 2 1 VREG_S1_S6_SENSE_P 3
XW702_E SHORT-10L-0.1MM-SM 2 1 VREG_S1_S6_SENSE_N 3

NOSTUFF

PART_NUMBER=337S00865 ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 6 OF 8
PWR
CRITICAL

33 32 31 9 8 6 5 4 PP_1V8_LDO6
31 4 PP_1V1_LDO2
33 32 31 9 8 6 5 4 PP_1V8_LDO6
31 5 PP_PMX_VIO_OUT
31 28 4 1 PP_UIM1_LDO11
31 28 4 1 PP_UIM2_LDO13
31 9 6 4 PP_1V2_LDO1
33 32 31 9 8 6 5 4 PP_1V8_LDO6
32 31 4 PP_1V2_LDO15
5 PP_VREF_SDX
31 8 6 4 PP_0V6_LDO14
31 4 3 PP_0V82_SMPS3
33 32 31 9 8 6 5 4 PP_1V8_LDO6
33 31 9 6 4 PP_0V875_LDO4

VDD1: AC37 G37
VDD2: AA37 C37 K36 L37 R37 U37
VDDPX_3: AE37 AH2 AK22 AK34 B36 C1 R1
VDDPX_0: AG1
VDDPX_4: V2
VDDPX_5: W1
VDDPX_11: AF6
VDDPX_12: J1
VDDPX_71: AJ33
VDDPX_72: AG37
VDDPX_73: AJ21
VDDPX_74: AH4
VDDPX_VBIAS_UIM: V6
VDDQ: D36 F36 H36 M36 T36 V36 Y36
VDD_ILDO_NAV: F32
VDD_QFPROM: AE29
VDD_USB_HS_DVDD: AF12

C719_E C724_E C729_E 2.2UF C733_E 2.2UF C739_E C741_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C720_E C725_E C730_E C734_E C737_E C740_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C738_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C789_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C735_E C732_E C726_E C722_E C728_E C721_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C765_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BASEBAND
C767_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C723_E C727_E C731_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
132S00014 C736_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

PART_NUMBER=337S00865 ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 6 OF 8
PWR
CRITICAL

VDDA_DDRSS: L29 N29 R29 U29
VDDA_DDRSS_CC: V30
VDDA_DDRSS_HV: P32
VDDA_DDRSS_PLL_HV: W31
VDDA_PCIE_0P9: AF10
VDDA_PCIE_0P9: AG11
VDDA_PCIE_1P2: AF8
VDDA_QREF_0P9: G9
VDDA_QREF_0P9: AC7
VDDA_QREF_1P8: AE7
VDDA_USB_HS_1P8: AE13
VDDA_USB_HS_3P3: AG13
VDDA_USB_SS_0P9: AF14
VDDA_USB_SS_1P2: AE15
VDDA_QLINK0_HV: G19
VDDA_QLINK0_LV: F20
VDDA_QLINK0_LV: G17
VDDA_QLINK0_LV_CK: F18
VDDA_QLINK1_HV: G13
VDDA_QLINK1_LV: G11
VDDA_QLINK1_LV: G15
VDDA_QLINK1_LV_CK: F12
VDDA_QLINK1_LV_CK: F14
VDDIO_DDRSS: J31
VDDIO_DDRSS: L31
VDDIO_DDRSS: N31
VDDIO_DDRSS: U31
VDDIO_DDRSS_CK: R31

基带电源输出的0.75V S7供电
PP_0V75_SMPS7

C749_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C768_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C769_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND

PP_1V2_LDO1 4 6 9 31
PP_0V875_LDO4 4 6 9 31 33
PP_0V875_LDO4 4 6 9 31 33
PP_1V2_LDO1 4 6 9 31
PP_1V8_LDO5 4 6 31 33

C742_E C744_E C745_E 2.2UF C752_E 2.2UF C758_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

PP_1V8_LDO5 4 6 31 33
PP_3V1_LDO10 4 31
PP_0V875_LDO4 4 6 9 31 33
PP_1V2_LDO1 4 6 9 31
PP_1V2_LDO1 4 6 9 31

C759_E C755_E C766_E C746_E 2.2UF C750_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

PP_0V875_LDO4 4 6 9 31 33

C747_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C751_E C756_E C760_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

PP_0V6_LDO14 4 6 8 31

C743_E C748_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C770_E C771_E C772_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C773_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C774_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

VDD_CX
31 6 3 PP_0V75_SMPS5 基带电源输出的0.75V S5供电

C701_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C704_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
132S00014 C706_E C709_E C712_E C715_E C754_E C757_E C775_E C776_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

VDD_MX
31 6 4 3 PP_0V75_SMPS7 基带电源输出的0.75V S7供电

C702_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C705_E C707_E C710_E C713_E C716_E C718_E C779_E C781_E C783_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

VDD_MODEM
31 6 3 PP_0V75_SMPS1_6

138S00071 C777_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C787_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C788_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C708_E C711_E C714_E C717_E C778_E C780_E C782_E C784_E C785_E C786_E 0.47UF 20% 6.3V X5R 01005-1 138S00133 ROOM=BASEBAND

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PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 7 OF 8

GND

CRITICAL

A1	GND	GND	AF24
A11	GND	GND	AF26
A15	GND	GND	AF28
A19	GND	GND	AG15
A23	GND	GND	AG5
A27	GND	GND	AG7
A3	GND	GND	AH10
A31	GND	GND	AH14
A35	GND	GND	AH18
A37	GND	GND	AH20
A7	GND	GND	AH8
AA11	GND	GND	AJ1
AA13	GND	GND	AJ17
AA15	GND	GND	AJ37
AA17	GND	GND	AK10
AA21	GND	GND	AK14
AA23	GND	GND	AK2
AA25	GND	GND	AK32
AA31	GND	GND	AK36
AA5	GND	GND	AK4
AA9	GND	GND	AK8
AB18	GND	GND	C3
AB20	GND	GND	C35
AB26	GND	GND	D10
AB28	GND	GND	D14
AB30	GND	GND	D18
AB36	GND	GND	D22
AB4	GND	GND	D26
AB6	GND	GND	D30
AD10	GND	GND	D34
AD12	GND	GND	D4
AD14	GND	GND	D6
AD16	GND	GND	E11
AD28	GND	GND	E13
AD30	GND	GND	E15
AD36	GND	GND	E17
AD8	GND	GND	E19
AE1	GND	GND	E21
AE11	GND	GND	E23
AE17	GND	GND	E25
AE19	GND	GND	E27
AE21	GND	GND	E29
AE23	GND	GND	E31
AE27	GND	GND	E33
AE5	GND	GND	E35
AE9	GND	GND	E37
AF16	GND	GND	E7
AF18	GND	GND	E9
AF20	GND	GND	F10
AF22	GND	GND	F16

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 8 OF 8

GND

CRITICAL

F22	GND	GND	N23
F24	GND	GND	N25
F26	GND	GND	N27
F28	GND	GND	N33
F30	GND	GND	N35
F34	GND	GND	N9
F8	GND	GND	P10
G29	GND	GND	P12
G31	GND	GND	P14
G33	GND	GND	P16
G35	GND	GND	P18
H30	GND	GND	P20
H32	GND	GND	P22
H34	GND	GND	P24
J13	GND	GND	P26
J15	GND	GND	P30
J17	GND	GND	R33
J19	GND	GND	R35
J21	GND	GND	T30
J23	GND	GND	T32
J25	GND	GND	T34
J27	GND	GND	U1
J29	GND	GND	U11
J33	GND	GND	U13
J35	GND	GND	U15
J37	GND	GND	U17
K10	GND	GND	U19
K12	GND	GND	U25
K14	GND	GND	U27
K20	GND	GND	U33
K22	GND	GND	U35
K24	GND	GND	U9
K26	GND	GND	V10
K28	GND	GND	V12
K30	GND	GND	V14
K32	GND	GND	V16
K34	GND	GND	V18
K8	GND	GND	V20
L1	GND	GND	V22
L33	GND	GND	V24
L35	GND	GND	V26
M30	GND	GND	V28
M32	GND	GND	V32
M34	GND	GND	V34
N11	GND	GND	V8
N13	GND	GND	W33
N15	GND	GND	W35
N17	GND	GND	W37
N19	GND	GND	Y30
N21	GND		

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BB:IO,MEM,SERDES,EEPROM

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PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 2 OF 8
QLINK
CRITICAL

85_SUB6_QLINK_L0_P	C29	QLINK0_L0_P	QLINK1_L0_P	C11	85_MMW_QLINK_L0_P
85_SUB6_QLINK_L0_N	B28	QLINK0_L0_M	QLINK1_L0_M	D12	85_MMW_QLINK_L0_N
85_SUB6_QLINK_L1_P	D32	QLINK0_L1_P	QLINK1_L1_P	B14	85_MMW_QLINK_L1_P
85_SUB6_QLINK_L1_N	C31	QLINK0_L1_M	QLINK1_L1_M	A13	85_MMW_QLINK_L1_N
85_SUB6_QLINK_L2_P	C33	QLINK0_L2_P	QLINK1_L2_P	B18	85_MMW_QLINK_L2_P
85_SUB6_QLINK_L2_N	B32	QLINK0_L2_M	QLINK1_L2_M	A17	85_MMW_QLINK_L2_N
85_SUB6_QLINK_L3_P	D24	QLINK0_L3_P	QLINK1_L3_P	B8	85_MMW_QLINK_L3_P
85_SUB6_QLINK_L3_N	C23	QLINK0_L3_M	QLINK1_L3_M	C9	85_MMW_QLINK_L3_N
85_SUB6_QLINK_L4_P	D28	QLINK0_L4_P	QLINK1_L4_P	B6	85_MMW_QLINK_L4_P
85_SUB6_QLINK_L4_N	C27	QLINK0_L4_M	QLINK1_L4_M	A5	85_MMW_QLINK_L4_N
85_SUB6_QLINK_L5_P	C25	QLINK0_L5_P	QLINK1_L5_P	C17	85_MMW_QLINK_L5_P
85_SUB6_QLINK_L5_N	B24	QLINK0_L5_M	QLINK1_L5_N	B16	85_MMW_QLINK_L5_N
85_SUB6_QLINK_L6_P	B26	QLINK0_L6_P	QLINK1_L6_P	B20	85_MMW_QLINK_L6_P
85_SUB6_QLINK_L6_N	A25	QLINK0_L6_M	QLINK1_L6_M	C21	85_MMW_QLINK_L6_N
85_SUB6_QLINK_L7_P	B34	QLINK0_L7_P	QLINK1_L7_P	B12	85_MMW_QLINK_L7_P
85_SUB6_QLINK_L7_N	A33	QLINK0_L7_M	QLINK1_L7_M	C13	85_MMW_QLINK_L7_N
85_SUB6_QLINK_CLK_P	A29	QLINK0_CLK_P	QLINK1_L8_P	B10	85_MMW_QLINK_L8_P
85_SUB6_QLINK_CLK_N	B30	QLINK0_CLK_M	QLINK1_L8_M	A9	85_MMW_QLINK_L8_N
			QLINK1_L9_P	D8	85_MMW_QLINK_L9_P
			QLINK1_L9_M	C7	85_MMW_QLINK_L9_N
			QLINK1_L10_P	B22	85_MMW_QLINK_L10_P
			QLINK1_L10_M	A21	85_MMW_QLINK_L10_N
			QLINK1_L11_P	C19	85_MMW_QLINK_L11_P
			QLINK1_L11_M	D20	85_MMW_QLINK_L11_N
			QLINK1_L12_P	B4	85_MMW_QLINK_L12_P
			QLINK1_L12_M	C5	85_MMW_QLINK_L12_N
			QLINK1_CLK_P	C15	85_MMW_QLINK_CLK_P
			QLINK1_CLK_M	D16	85_MMW_QLINK_CLK_N

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 3 OF 8
GPIO
CRITICAL

IO_BB_BI_SIM2_DATA	AA3	GPIO_0	H2 NC
IO_BB_FROM_SIM2_DETECT	AA1	GPIO_1	H4 NC
IO_BB_TO_SIM2_RESET	AB2	GPIO_2	AK28 NC
IO_BB_TO_SIM2_CLK	Y2	GPIO_3	Y32 NC
	T6 NC	GPIO_4	AJ23 UART_BB_TO_WLAN_TX
	U3 NC	GPIO_5	AK24 UART_BB_TO_WLAN_RX
	V4 NC	GPIO_6	AC33 NC
	U5 NC	GPIO_7	AA35 GPIO_AP_FROM_BB_RESET_DETECT_L
UART1_AOP_FROM_BB_RXD CPU到基带的UART1总线数据接收	AK26	GPIO_8 BB_TX	AJ35 GPIO_AP_TO_BB_COREDUMP
UART1_AOP_TO_BB_TXD CPU到基带的UART1总线数据发射	AJ25	GPIO_9 BB_RX	AH36 NC
BB_EEPROM_I2C_SDA	AH26	GPIO_10	AG35 NC
BB_EEPROM_I2C_SCL	AG25	GPIO_11	AF36 NC
I2S2_AP_FROM_BB_LRCLK 基带到CPU的I2S1总线帧时钟	AF30	GPIO_12	AC31 NC
I2S2_AP_TO_BB_DOUT CPU到基带的I2S2总线数据	AF32	GPIO_13	AE33 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L
I2S2_AP_FROM_BB_DIN 基带到CPU的I2S2总线数据	AG31	GPIO_14	AE35 NC
I2S2_AP_FROM_BB_BCLK 基带到CPU的I2S1总线串行时钟	AH30	GPIO_15	AD34 NC
	AK30 NC	GPIO_16	AF34 PCIE_GP2_AP_BI_BB_CLKREQ_L
	AG33 NC	GPIO_17	AE31 PCIE_GP2_AP_TO_BB_PERST_L
	AH32 NC	GPIO_18	AB34 BOOT_CFG1
BB_TO_DOTARA_COEX_1V2:NOT USED	AJ31 NC	GPIO_19	AC35 NC
GPIO_R1_TO_BB_CH9_COEX	AG27	GPIO_20	AB37 NC
GPIO_R1_TO_BB_LAA_SW_CTRL	AG27	GPIO_21	GPIO_60_RESERVED_FOR_VFR_IRQ
	AJ29 NC	GPIO_22	GPIO_AP_TO_BB_PEAK_PWR_IND AD32
	AJ28 NC	GPIO_23	AG29 NC
BOOT_CFG2	AA33	GPIO_24	K6 NC
	Y34 NC	GPIO_25	L3 NC
	K2 NC	GPIO_26	L5 NC
	K4 NC	GPIO_27	M4 NC
BB_TO_SDR_WMSS_RESET_L	E1	GPIO_28	AD2 IO_BB_BI_SIM1_DATA
SHIELD_RFFE4_SCLK_BB	G3	GPIO_29	AC1 IO_BB_FROM_SIM1_DETECT
SHIELD_RFFE4_SDATA_BB	F4	GPIO_30	AD4 IO_BB_TO_SIM1_RESET
GPIO_AP_TO_BB_TIME_MARK CPU到基带时间标记信号	AH24	GPIO_31	AC3 IO_BB_TO_SIM1_CLK
GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	G1	GPIO_32	AH34 NC
QLINK_EN_BB_TO_SDR	F2	GPIO_33	E3 QLINK_EN_BB_TO_SMR
QLINK_REQ_SDR_TO_BB	E5	GPIO_34	D2 QLINK_REQ_SMR_TO_BB
SHIELD_RFFE0_SDATA_BB	J5	GPIO_35	B2 BB_TO_SMR_WMSS_RESET_L
SHIELD_RFFE0_SCLK_BB	J3	GPIO_36	AH22 GPIO_BB_TO_R1_COEX
SHIELD_RFFE1_SDATA_BB	G5	GPIO_37	AG21 GPIO_BB_TO_R1_CH9_REQ
SHIELD_RFFE1_SCLK_BB	H6	GPIO_38	F6 NC
		GPIO_39	AF3 NC
		GPIO_78	AG1 NC
		GPIO_79	

MUXED WITH UART (FOR WCI-2 BB-WLAN COEX)

NOTE: TYPO IN SPEC

CPU到基带的复位检测

CPU到基带的纠错信号

电源到基带的PCIE总线唤醒信号

AP_TO_BB_DEV_WAKE : NOT USED
WAKE O/P WHEN BB IS END POINT

基带到CPU的PCIE总线时钟请求

CPU到基带的PCIE总线复位

C906_E 33PF 5% 16V NP0-C0G 01005-1 ROOM=BASEBAND
NOSTUFF
131S00292

NOTE:

ENSURE THAT THERE ARE NO UNINTENTIONAL EXTERNAL PULL-UPS ON THE FOLLOWING GPIOS AND THESE GPIOS ARE NOT LOGIC HIGH UNINTENTIONALLY BEFORE SDX55M COMES OUT OF RESET

(I.E. BEFORE SDX_RESOUT_N DE-ASSERTS TO LOGIC HIGH): GPIO_24, 54, 58, 59, AND 75.
SEE BOOT CONFIGURATION GPIOS PAGE OF SDX55M DESIGN GUIDELINES (80-PK565-5BM) FOR DETAILS.

BB EEPROM

PP_1V8_LDO6
R908_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND
C901_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BASEBAND
R909_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND
EEPROM_E CAT24C08C4A WLCSP ROOM=BASEBAND CRITICAL
A1 VCC
B1 SCL
SDA B2
A2
VSS
BB_EEPROM_I2C_SCL
BB_EEPROM_I2C_SDA

DUAL-VOLTAGE IO PADS

VDD_PX71: GPIO8,9,12-23
VDD_PX72: GPIO46-57,59-61,71
VDD_PX73: GPIO31-32,44-45, 75-76
VDD_PX74: GPIO78-79

PP1V8_Always PP1V8_IO PP1V8_S2 PP1V8_SDRAM PP1V8_S4

DUAL PSIM: SHORT SIM1_DET WITH SIM2_DET
PSIM AND ESIM: SIM2_DET STUFF PU

PP_1V8_LDO6
R905_E 100K 5% 1/32W MF 01005 ROOM=BASEBAND
R907_E 100K 5% 1/32W MF 01005 ROOM=BASEBAND
IO_BB_FROM_SIM1_DETECT
IO_BB_FROM_SIM2_DETECT
NOSTUFF
R906_E 100K 5% 1/32W MF 01005 ROOM=BASEBAND

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 1 OF 8
CONTROL
CRITICAL

SHIELD_SLEEP_CLK_32K	W3	SLEEP_CLK	EBI_ZQ P36 SHIELD_BB_BDM_ZQ
SHIELD_CXO_REXT	AJ3	QREFS_CXO_REXT	EBI_CA_CAL N37 SHIELD_BB_EBI1_CAL
SHIELD_MDM_19P2M_CLK	AD6	CXO	
BB_JTAG_RST_L	P6	SRST*	RESOUT* T2 NC
PMIC_RESOUT_L	AC5	RESIN*	PS_HOLD T4 PS_HOLD
	N3 NC	MODE_0	DNC AG19 NC
	M4 NC	MODE_1	DNC M6 NC
BB_JTAG_TCK_SWD_CLK_1V8_R	N1	TCK	DNC N5 NC
BB_JTAG_TRST_L	P2	TRST*	DNC P34 NC
BB_JTAG_TMS_SWD_IO_1V8_R	R3	TMS	REFGEN_REXT AK20 SHIELD_PCIE_CAL_RES
BB_JTAG_TDI	R5	TDI	
BB_JTAG_TDO	P4	TDO	PMIC_SPMI_CLK AF2 BB_BBPMU_SPMI_CLK 基带到基带电源SPMI总线时钟
			PMIC_SPMI_DATA AE3 BB_BBPMU_SPMI_DATA 基带到基带电源SPMI总线数据

基带电源到基带的32K时钟
基带时钟芯片到基带 19.2MHz 时钟

R904_E 3.0K 1% 1/32W MF 01005 ROOM=BASEBAND
R902_E 240 1% 1/32W MF 01005 ROOM=BASEBAND
R903_E 240 1% 1/32W MF 01005 ROOM=BASEBAND
PP_0V6_LDO14
R901_E 100 1% 1/32W MF 01005 ROOM=BASEBAND
131S00353
C904_E 10PF 5% 16V NP0/C0G 01005 BASEBAND
131S00353
C905_E 10PF 5% 16V NP0/C0G 01005 BASEBAND

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 4 OF 8
USB_PCIE
CRITICAL

		PCIE_REFCLK_P	AJ9 90_PCIE_GP2_AP_TO_BB_REFCLK_P
		PCIE_REFCLK_M	AG9 90_PCIE_GP2_AP_TO_BB_REFCLK_N
90_USB_BB_P	AJ15	USB_HS_DP	PCIE_TX0_P AJ13 90_PCIE_BB_TO_AP_RX_SDX_P
90_USB_BB_N	AK16	USB_HS_DM	PCIE_TX0_M AH12 90_PCIE_BB_TO_AP_RX_SDX_N
	AG17 NC	USB_SS_TX_P	PCIE_TX1_P AJ11 NC
	AJ16 NC	USB_SS_TX_M	PCIE_TX1_M AK12 NC
	AK18 NC	USB_SS_RX_P	PCIE_RX0_P AJ5 90_PCIE_GP2_AP_TO_BB_TX_P
	AJ19 NC	USB_SS_RX_M	PCIE_RX0_M AK6 90_PCIE_GP2_AP_TO_BB_TX_N
			PCIE_RX1_P AH6 NC
			PCIE_RX1_M AJ7 NC

CPU到基带的PCIE总线时钟P
CPU到基带的PCIE总线时钟N

132S00014
C903_E 0.22UF 10% 6.3V CER-X5R 01005
C902_E 0.22UF 10% 6.3V CER-X5R 01005
132S00014

CPU到基带的PCIE总线数据接收P
CPU到基带的PCIE总线数据接收N
CPU到基带的PCIE总线数据发射P
CPU到基带的PCIE总线数据发射N

PP1V2_S2
C907_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=BASEBAND
R910_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND
VCCA VCCB ROOM=BASEBAND
SWD_E NVT020ZJK X2SON CRITICAL
SWD_OE OE
A1
A2
GND
R911_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND NOSTUFF
PP_1V8_LDO6
C908_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=BASEBAND

CPU输出的SWD总线时钟
CPU到基带的SWD总线数据

XW912_E SHORT-01005-SP 998-23033 BASEBAND
XW914_E SHORT-01005-SP 998-23033 BASEBAND
XW913_E SHORT-01005-SP 998-23033 BASEBAND

SWD_AP_TO_MANY_SWCLK
SWD_AP_BI_BB_SWDIO
BB_JTAG_TMS_SWD_IO_R
BB_JTAG_TCK_SWD_CLK_1V8
BB_JTAG_TMS_SWD_IO_1V8
BB_JTAG_TCK_SWD_CLK_1V8_R
BB_JTAG_TMS_SWD_IO_1V8_R

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NOTE: 4UF BULK COULD BE FURTHER AWAY AND MAKE SURE THE STAR ROUTING IS FROM 4UF.
NOTE: 1UF SHOULD BE AS CLOSE AS POSSIBLE TO CORRESPONDING PIN ON SDR

PP_1V2_LDO1 → C1135_E 4UF 20% 6.3V CER-X5R 0201 (ROOM=SUB6_XCVR) ; C1136_E 4UF 20% 6.3V CER-X5R 0201 (ROOM=SUB6_XCVR)

STAR ROUTE

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 6 OF 8
CRITICAL

A24	VDDAM_TP0	VDDAH_TP0	B25
AG26	VDDAM_TP1	VDDAH_TP1	AF25
B29	VDDAM_TX0	VDDAH_TX0	A30
AF29	VDDAM_TX1	VDDAH_TX1	AF31
AF23	VDDAM_TX2	VDDAH_TX2	AG22
E2	VDDAM_RP0	VDDAH_RP0	C2
F1	VDDAM_RP1	VDDAH_RP1	G2
P1	VDDAM_RP2	VDDAH_RP2	M1
V1	VDDAM_RP3	VDDAH_RP3	Y1
AB1	VDDAM_RP4	VDDAH_RP4	AG4
AF15	VDDAM_RP5	VDDAH_RP5	AF9
		VDDAH_RP5_2	AF13
A16	VDDAM_RX0	VDDAH_RX0	A18
AG10	VDDAM_RX5		
D21	VDDAM_BBRX_TOP	VDDAH_TXDAC0	J32
AA22	VDDAM_BBRX_BOT	VDDAH_TXDAC1	W30
		VDDAH_LVDS	T21
V35	VDD_CX		
W36	VDD_CX		
L36	VDD_CX		
J34	VDD_MX0		
V33	VDD_MX1		
L34	VDD_PHY		
K35	VDD_PX		
K33	VDD_PXM		

Left-side rails

PP_1V2_LDO1 (31 9 6 4) → XW1181_E (SHORT-8L-0.1MM-SM) → PP_1V2_LDO1_SDR_VDDAM_TP
- XW1101_E → PP_LDO1_SDR_VDDAM_TP0_30
- XW1102_E → PP_LDO1_SDR_VDDAM_TP1_30
- C1101_E 0.1UF, C1108_E 0.1UF

XW1186_E (SHORT-8L-0.25MM-SM) → PP_1V2_LDO1_SDR_VDDAM_TX
- XW1103_E → PP_LDO1_SDR_VDDAM_TX0_40
- XW1104_E → PP_LDO1_SDR_VDDAM_TX1_40
- XW1105_E → PP_LDO1_SDR_VDDAM_TX2_40
- C1113_E 0.1UF, C1109_E 0.1UF, C1102_E 0.1UF

XW1187_E (SHORT-8L-0.5MM-SM) → PP_1V2_LDO1_SDR_VDDAM_RP
- XW1106_E → PP_LDO1_SDR_VDDAM_RP0_57
- XW1107_E → PP_LDO1_SDR_VDDAM_RP1_57
- XW1108_E → PP_LDO1_SDR_VDDAM_RP2_57
- C1114_E 0.1UF, C1110_E 0.1UF, C1103_E 0.1UF

- XW1109_E → PP_LDO1_SDR_VDDAM_RP3_57
- XW1110_E → PP_LDO1_SDR_VDDAM_RP4_57
- XW1111_E → PP_LDO1_SDR_VDDAM_RP5_30
- C1115_E 0.1UF, C1111_E 0.1UF, C1104_E 0.1UF

XW1185_E (SHORT-8L-0.5MM-SM) → PP_1V2_LDO1_SDR_VDDAM_RX
- XW1112_E → PP_LDO1_SDR_VDDAM_RX0_171
- XW1113_E → PP_LDO1_SDR_VDDAM_RX5_138
- C1105_E 0.1UF, C1112_E 0.1UF

- XW1114_E → PP_LDO1_SDR_VDDAM_BBRX_TOP_97
- XW1115_E → PP_LDO1_SDR_VDDAM_BBRX_BOT_215
- C1106_E 0.1UF, C1107_E 0.1UF

PP_0V8_LDO8 (31 4)
- C1137_E 4UF 20% 6.3V CER-X5R 0201
- C1116_E 0.1UF, C1117_E 0.1UF

XW1117_E (SHORT-8L-0.25MM-SM) → PP_0V875_LDO4 (33 31 6 4) → PP_LDO4_VDD_MX0_PHY_123
- C1118_E 0.1UF

XW1118_E (SHORT-8L-0.1MM-SM) → PP_LDO4_VDD_MX1_96
- C1138_E 4UF 20% 6.3V CER-X5R 0201
- C1119_E 0.1UF

XW1119_E (SHORT-8L-0.1MM-SM) → PP_1V8_LDO6 (33 32 31 9 8 6 5 4) → PP_LDO6_SDR_VDD_PX_20
- C1139_E 4UF 20% 6.3V CER-X5R 0201
- C1120_E 0.1UF

XW1120_E (SHORT-8L-0.1MM-SM) → PP_1V8_LDO6 (33 32 31 9 8 6 5 4) → PP_LDO6_SDR_VDD_PXM_20
- C1142_E 4UF 20% 6.3V CER-X5R 0201
- C1143_E 0.1UF

Right-side rails

- XW1151_E → PP_LDO16_SDR_VDDAH_TP0_35 → XW1184_E → PP_1V7_LDO16 (4 9 31)
- XW1152_E → PP_LDO16_SDR_VDDAH_TP1_35 → XW1184_E → PP_1V7_LDO16_SDR_VDDAH_TP
- C1121_E 0.1UF, C1122_E 0.1UF

XW1153_E → PP_LDO16_SDR_VDDAH_TX0_40 → XW1189_E (SHORT-8L-0.25MM-SM) → PP_1V7_LDO16_SDR_VDDAH_TX
- C1123_E 0.1UF

XW1154_E → PP_LDO16_SDR_VDDAH_TX1_40 → XW1190_E (SHORT-8L-0.25MM-SM) → PP_1V7_LDO16_SDR_VDDAH_TX_1_2
- C1124_E 0.1UF

XW1155_E → PP_LDO16_SDR_VDDAH_TX2_40
- C1125_E 0.1UF

XW1156_E → PP_LDO16_SDR_VDDAH_RP0_5 → XW1183_E (SHORT-8L-0.25MM-SM) → PP_1V7_LDO16_SDR_VDDAH_RP
- XW1157_E → PP_LDO16_SDR_VDDAH_RP1_5
- C1126_E 0.1UF, C1144_E 0.1UF

XW1158_E → PP_LDO16_SDR_VDDAH_RP2_35
- C1127_E 0.1UF

XW1159_E → PP_LDO16_SDR_VDDAH_RP3_35
- C1130_E 0.1UF

XW1160_E → PP_LDO16_SDR_VDDAH_RP4_35
- C1128_E 0.1UF

XW1161_E → PP_LDO16_SDR_VDDAH_RP5_5
XW1162_E → PP_LDO16_SDR_VDDAH_RP5_2_30
- C1131_E 0.1UF, C1145_E 0.1UF

XW1163_E → PP_LDO16_SDR_VDDAH_RX0_10
- C1129_E 0.1UF

XW1164_E → PP_LDO16_SDR_VDDAH_TXDAC0_13 → XW1182_E → PP_1V7_LDO16_SDR_VDDAH_TXDAC
XW1165_E → PP_LDO16_SDR_VDDAH_TXDAC1_26
- C1133_E 0.1UF, C1132_E 0.1UF

XW1166_E (PATH=I226) → PP_LDO16_SDR_VDDAH_LVDS_12
- C1134_E 0.1UF

Bottom-right rails

PP_1V7_LDO16 (4 9 31)
- C1140_E 4UF 20% 6.3V CER-X5R 0201
- C1141_E 4UF 20% 6.3V CER-X5R 0201

STAR ROUTE

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SYNC_DATE=08/01/2019

PAGE TITLE: XCVR POWER_1

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NOTE: 4UF BULK COULD BE FURTHER AWAY AND MAKE SURE THE STAR ROUTING IS FROM 4UF.
NOTE: 1UF SHOULD BE AS CLOSE AS POSSIBLE TO CORRESPONDING PIN ON SDR

PP_0V8_LDO3 4 10 31
PP_0V8_LDO3 31 10 4

C1226_E 4UF 20% 6.3V CER-X5R 0201 ROOM=SUB6_XCVR
C1227_E 4UF 20% 6.3V CER-X5R 0201 ROOM=SUB6_XCVR

XW1202_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1203_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1204_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1205_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1206_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1207_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_RP0 57
PP_LDO3_SDR_VDDAL_RP1 57
PP_LDO3_SDR_VDDAL_RP2 57
PP_LDO3_SDR_VDDAL_RP3 57
PP_LDO3_SDR_VDDAL_RP4 57
PP_LDO3_SDR_VDDAL_RP5 57

C1217_E 1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1215_E 1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1212_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1209_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1205_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1201_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1208_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
PP_LDO3_SDR_VDDAL_RX0 67
C1202_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1209_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1210_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1211_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1212_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1213_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1214_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_RX1 22
PP_LDO3_SDR_VDDAL_RX2 22
PP_LDO3_SDR_VDDAL_RX3 22
PP_LDO3_SDR_VDDAL_RX4 22
PP_LDO3_SDR_VDDAL_RX5 22
PP_LDO3_SDR_VDDAL_RX6 90

C1233_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1206_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1234_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1235_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1210_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1213_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1215_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1216_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1217_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1218_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1201_E SHORT-10L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_RXLO0 27
PP_LDO3_SDR_VDDAL_RXLO4 27
PP_LDO3_SDR_VDDAL_RXLO5 27
PP_LDO3_SDR_VDDAL_RXLO7 27
PP_LDO3_SDR_VDDAL_TP0 30

C1203_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1236_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1237_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1207_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1204_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1237_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1238_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1239_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1240_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_TP1 30
PP_LDO3_SDR_VDDAL_TX0 20
PP_LDO3_SDR_VDDAL_TX1 20
PP_LDO3_SDR_VDDAL_TX2 20

C1208_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1216_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1214_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1211_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
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CRITICAL

D1	VDDAL_RP0
F3	VDDAL_RP1
N2	VDDAL_RP2
W2	VDDAL_RP3
AC2	VDDAL_RP4
AG16	VDDAL_RP5
B13	VDDAL_RX0
C6	VDDAL_RX1
J6	VDDAL_RX2
L6	VDDAL_RX3
W6	VDDAL_RX4
AC6	VDDAL_RX5
AG12	VDDAL_RX6
E12	VDDAL_RXLO0
N12	VDDAL_RXLO4
R12	VDDAL_RXLO5
W12	VDDAL_RXLO7
A26	VDDAL_TP0
AF27	VDDAL_TP1
A28	VDDAL_TX0
AG30	VDDAL_TX1
AE22	VDDAL_TX2
A4	VDDAL_DIG_RP0
K1	VDDAL_DIG_RP1
L2	VDDAL_DIG_RP2
AA2	VDDAL_DIG_RP3
AE2	VDDAL_DIG_RP4
AG14	VDDAL_DIG_RP5
G24	VDDAL_DIG_TP0
AA24	VDDAL_DIG_TP1
B21	VDDAL_DIG1
Y23	VDDAL_DIG2
H21	VDDAL_FBRX
B17	VDDAL_GNSS
A20	VDDAL_ICON6
T19	VDDAL_ICON32
T1	VDDAL_XO

XW1223_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
PP_LDO3_SDR_VDDAL_DIG_RP0 6
C1218_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_DIG_RP1 6
PP_LDO3_SDR_VDDAL_DIG_RP2 6
PP_LDO3_SDR_VDDAL_DIG_RP3 6
PP_LDO3_SDR_VDDAL_DIG_RP4 6
PP_LDO3_SDR_VDDAL_DIG_RP5 6

C1219_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1220_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1222_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1223_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1225_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1224_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1225_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1226_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1227_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1228_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_DIG_TP0 10
C1221_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
XW1229_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_DIG_TP1 10
C1224_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
XW1232_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_DIG1 171
C1231_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
XW1230_E SHORT-8L-0.25MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_DIG2 124
C1232_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
XW1231_E SHORT-8L-0.25MM-SM ROOM=SUB6_XCVR
XW1287_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_FBRX 20
XW1233_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_GNSS 40
C1238_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1230_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
XW1291_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_ICON6 5
XW1235_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_ICON32 25
C1239_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR
C1229_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1236_E SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR PATH=I106

PP_LDO3_SDR_VDDAL_XO 18
C1228_E 0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

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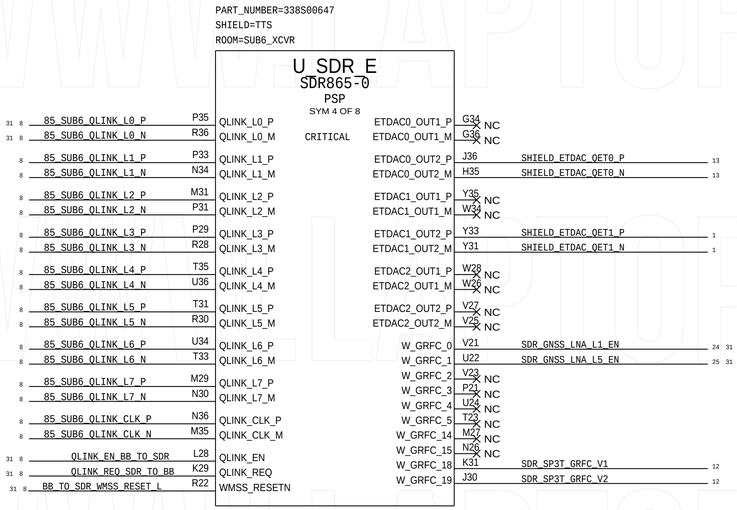

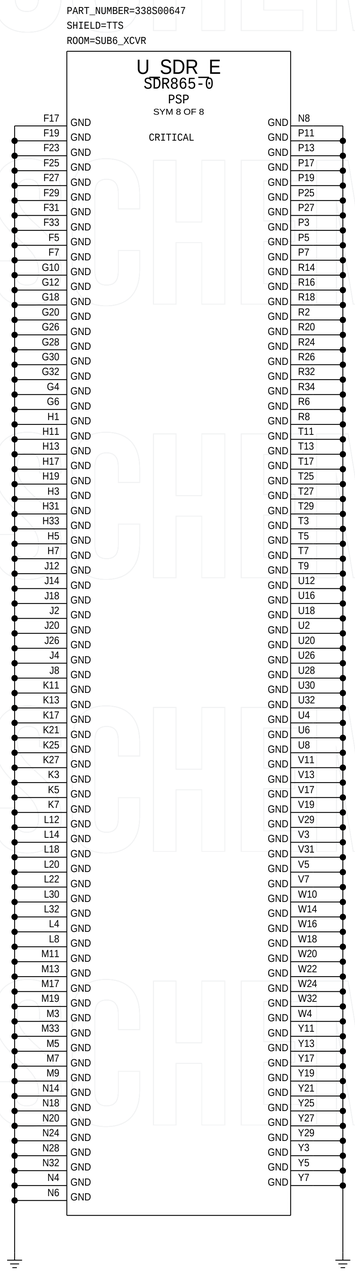

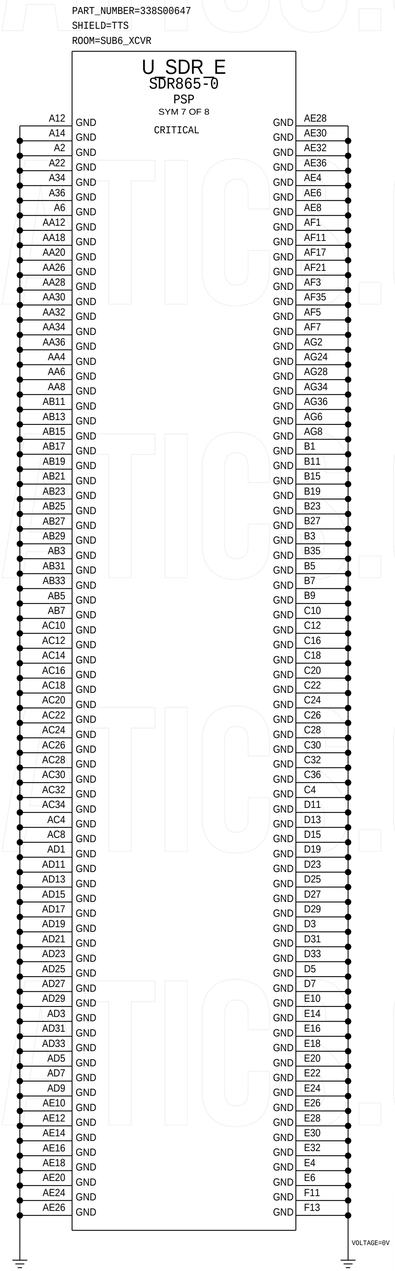

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TRANSCEIVER: TX & RX

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PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 3 OF 8
CRITICAL

QLINK BACKDOOR
SHIELD_RFFE4_SCLK_BB — F21 RFFE0_CLK
SHIELD_RFFE4_SDATA_BB — G22 RFFE0_DATA
SHIELD_RFFE1_SCLK_SDR — K23 RFFE1_CLK
SHIELD_RFFE1_SDATA_SDR — J24 RFFE1_DATA
SHIELD_RFFE2_SCLK_SDR — H25 RFFE2_CLK
SHIELD_RFFE2_SDATA_SDR — H27 RFFE2_DATA
SHIELD_RFFE3_SCLK_SDR — J28 RFFE3_CLK
SHIELD_RFFE3_SDATA_SDR — H29 RFFE3_DATA
SHIELD_RFFE5_SCLK_SDR — L26 RFFE5_CLK
SHIELD_RFFE5_SDATA_SDR — M25 RFFE5_DATA
SHIELD_RFFE7_SCLK_SDR — L24 RFFE7_CLK
SHIELD_RFFE7_SDATA_SDR — M23 RFFE7_DATA
SHIELD_RFFE8_SCLK_SDR — P23 RFFE8_CLK
SHIELD_RFFE8_SDATA_SDR — N22 RFFE8_DATA
NC — J22 RFFE9_CLK
NC — H23 RFFE9_DATA
SHIELD_SDR_38P4M_CLK — R4 XO_IN

基带时钟芯片到射频38.4M时钟

C1400_E 47PF 5% 16V NP0-C0G 01005 NOSTUFF ROOM=SUB6_XCVR

TX0_LB B31 — 50_TX_IN_XCVR_TX0_LB — TO LBPAD_TX
TX0_GSM_LB A32 — 50_TX_IN_XCVR_TX0_LB2G — TO LMB/2G PAD_TX
TX0_JB B33 — 50_TX_IN_XCVR_TX0_LMB — TO LMB/2G PAD_TX
TX0_MB C34 — 50_TX_IN_XCVR_TX0_MB1 — TO HBPAD_TX
TX0_GSM_MB D35 — 50_TX_IN_XCVR_TX0_MB2G — TO LMB/2G PAD_TX
TX0_HB E36 — 50_TX_IN_XCVR_TX0_HB1 — TO HBPAD_TX
TX0_UHB E34 — NC
TX0_LAA_V2X F35 — NC
TX1_LB_JB AG32 — 50_TX_IN_XCVR_TX1_LB_JB — TO LBPAD_TX
TX1_HB2 AE34 — NC
TX1_MB AF33 — NC
TX1_HB1 AD35 — 50_TX_IN_XCVR_TX1_HB1 — TO HBDSM TX
TX1_UHB_5GLM AB35 — NC
TX1_5GH AC36 — NC
TX2_HB_V2X AF19 — NC
TX2_UHB_5GLM AG20 — 50_TX_IN_XCVR_TX2_UHB
TX2_5GH AG18 — 50_TX_IN_XCVR_TX2_N79

R1402_E 0.00 5% 1/32W MF 01005 ROOM=SUB6_XCVR
L1402_E 4.7NH-3%-0.270A 01005 NOSTUFF ROOM=SUB6_XCVR
L1406_E 4.7NH-3%-0.270A 01005 NOSTUFF ROOM=SUB6_XCVR
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 — TO UHBPAD LAT TX
TO UHBPAD LAT TX

R1403_E 0.00 5% 1/32W MF 01005 ROOM=SUB6_XCVR
L1403_E 4.7NH-3%-0.270A 01005 NOSTUFF ROOM=SUB6_XCVR
L1407_E 4.7NH-3%-0.270A 01005 NOSTUFF ROOM=SUB6_XCVR
50_TX_IN_TX2_UHB_PAD_TX_N79_IN

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 1 OF 8
PRX
CRITICAL

FROM HBPAD_RX — 50_RX_XCVR_PRX0_MB_HBT_PRX_OUT4 — K9 PRX0
FROM MIMODSM_L — 50_RX_XCVR_PRX1_MIMO1_RX_OUT_DRX4 — H15 PRX1
FROM HBPAD_RX — 50_RX_XCVR_PRX2_LMB_MBT_HBT_PRX_OUT1 — A10 PRX2
FROM MIMODSM_L — 50_RX_XCVR_PRX3_MIMO1_RX_OUT_DRX3 — V15 PRX3
FROM HBPAD_RX — 50_RX_XCVR_PRX4_MBT_HB_PRX_OUT2 — V9 PRX4
FROM MIMODSM_L — 50_RX_XCVR_PRX5_MIMO1_RX_OUT_DRX1 — U14 PRX5
FROM LBPAD_RX — 50_RX_XCVR_PRX6_LB_A_RX0 — J10 PRX6
FROM MIMODSM_L — 50_RX_XCVR_PRX7_MIMO1_RX_OUT_DRX2 — K15 PRX7
NC — C8 PRX8
50_RX_XCVR_PRX10_LB_PRX_OUT2 — A8 PRX10
NC — J16 PRX11
FROM LAA_RX_L — 50_LAA_RX_XCVR_PRX12 — L10 PRX12
NC — L16 PRX13
FROM UHBPAD_RX — 50_RX_XCVR_PRX14_N79_RX_OUT1 — Y9 PRX14
FROM UHBPAD_RX — 50_RX_XCVR_PRX15_N79_RX_OUT2 — Y15 PRX15
FROM UHBPAD_RX — 50_RX_XCVR_PRX16_UHB_RX_OUT1 — U10 PRX16
FROM UHBPAD_RX — 50_RX_XCVR_PRX17_UHB_RX_OUT2 — T15 PRX17

PRXE W8 — 50_RX_XCVR_PRXE_HB_PRX_OUT3

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 2 OF 8
DRX_GNSS
CRITICAL

FROM_HBDSM_RX — 50_RX_XCVR_DRX0_HB_DSM_RXOUT_DRX4 — G8 DRX0
FROM_MIMODSM_RX_U — 50_RX_XCVR_DRX1_MIMO2_RX_OUT_DRX4 — G16 DRX1
FROM_HBDSM_RX — 50_RX_XCVR_DRX2_HB_DSM_RXOUT_DRX1 — E8 DRX2
FROM_MIMODSM_RX_U — 50_RX_XCVR_DRX3_MIMO2_RX_OUT_DRX3 — AA14 DRX3
FROM_HBDSM_RX — 50_RX_XCVR_DRX4_HB_DSM_RXOUT_DRX2 — P9 DRX4
FROM_MIMODSM_RX_U — 50_RX_XCVR_DRX5_MIMO2_RX_OUT_DRX1 — N16 DRX5
FROM_LBDSM_RX — 50_RX_XCVR_DRX6_LB_DSM_RXOUT1 — H9 DRX6
FROM_MIMODSM_RX_U — 50_RX_XCVR_DRX7_MIMO2_RX_OUT_DRX2 — F15 DRX7
NC — F9 DRX8
NC — G14 DRX9
FROM_LAA_RX_U — 50_LAA_RX_XCVR_DRX10 — N10 DRX10
NC — M15 DRX11
FROM_UHBDSM_RX — 50_RX_XCVR_DRX12_UHB_DSM_N79_RX_OUT1 — AA10 DRX12
FROM_UHBDSM_RX — 50_RX_XCVR_DRX13_UHB_DSM_N79_RX_OUT2 — AA16 DRX13
FROM_UHBDSM_RX — 50_RX_XCVR_DRX14_UHB_DSM_UHB_RX_OUT1 — R10 DRX14
FROM_UHBDSM_RX — 50_RX_XCVR_DRX15_UHB_DSM_UHB_RX_OUT2 — P15 DRX15
NC — M21 DNC

FROM_HBDSM_RX
DRXE AB9 — 50_RX_XCVR_DRXE_HB_DSM_RXOUT_DRX3
DRXF D9 — 50_RX_XCVR_DRXF_LB_DSM_RXOUT2
FBRX_IN K19 — 50_TX_IN_XCVR_FBRX_1
GNSS_IN_L1 C14 — 50_RX_GNSS_L1
GNSS_IN_L5 D17 — 50_RX_GNSS_L5

FL1401_E 10-OHM-1-1A 01005 ROOM=SUB6_XCVR
PP3V0_S2 — PP3V0_S2_SP3T
C1401_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SUB6_XCVR 12S500014

U_SP3T_E
SP3T-MCD
LGA
PART_NUMBER=353S02417
ROOM=SUB6_XCVR
CRITICAL
GND
VDD
SDR_SP3T_GRFC_V1 — CTL1
SDR_SP3T_GRFC_V2 — CTL2
ANT
PORT1 — 50_CPLR_L_CPL1_LAT_OUT
PORT2 — 50_UHB_L_CPLR_OUT
PORT3 — 50_CPLR_U_CPL1_UAT_OUT

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DRAWING NUMBER: 051-05263
SIZE: D
REVISION: 9.0.0
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DISCRETE QET5100 0
HB/LMB-2G

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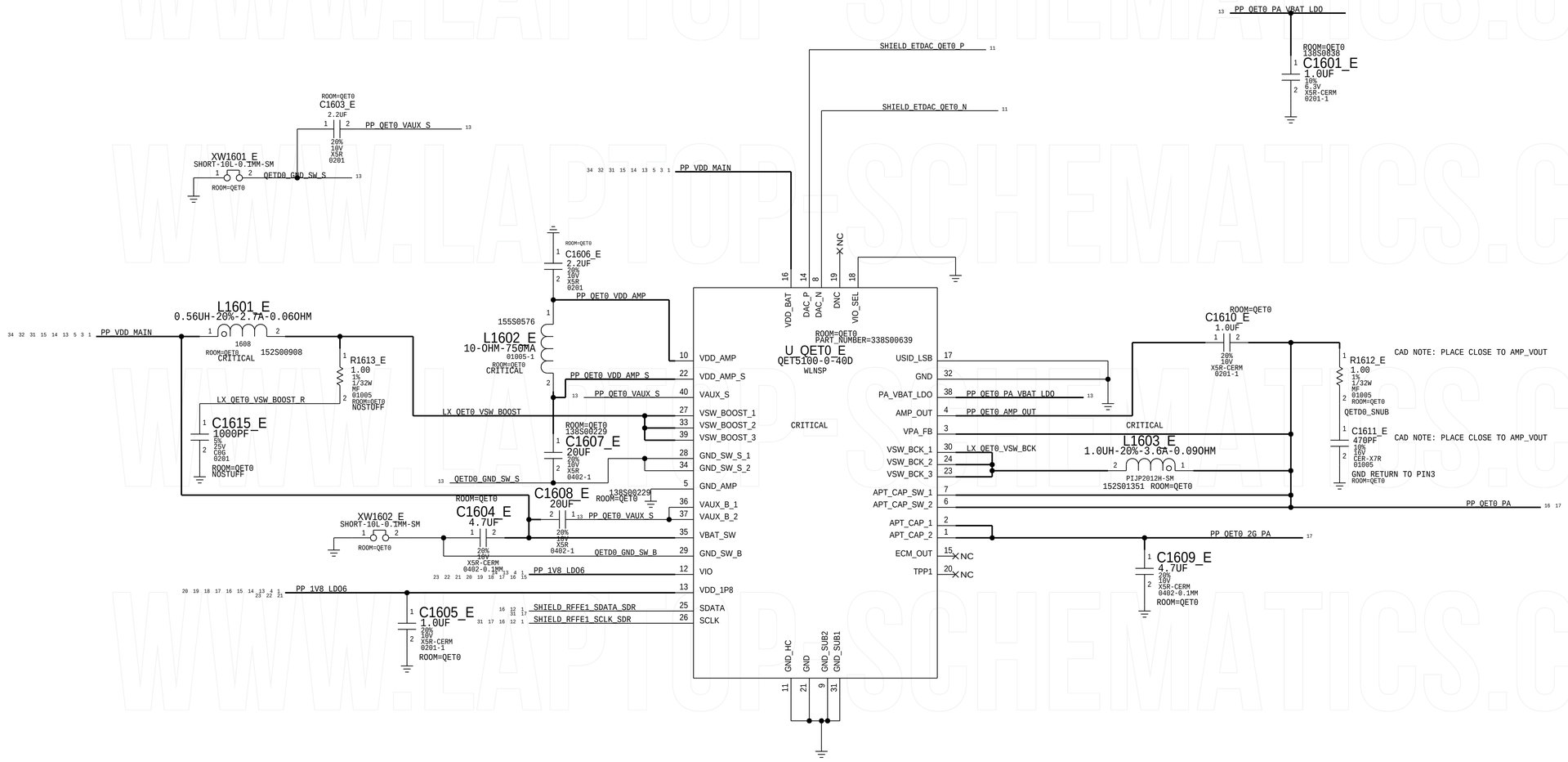

USID = 0X4 WHEN USID PIN IS GND
USID = 0X5 WHEN USID PIN IS HIGH

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PAGE TITLE: QET_DISCRETE_0

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PAGE: 16 OF 60
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APT DCDC 2

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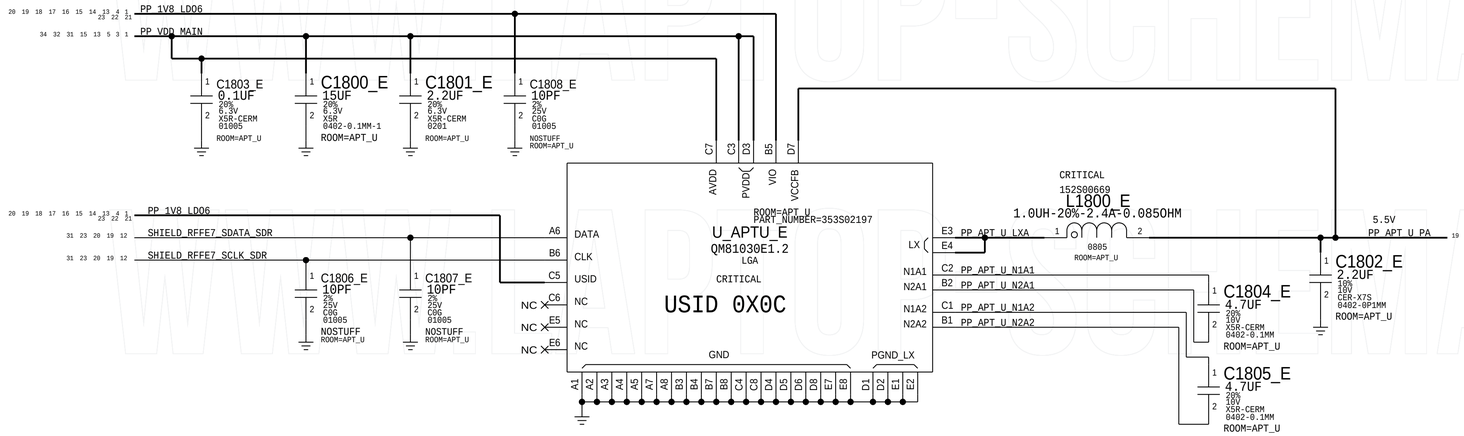

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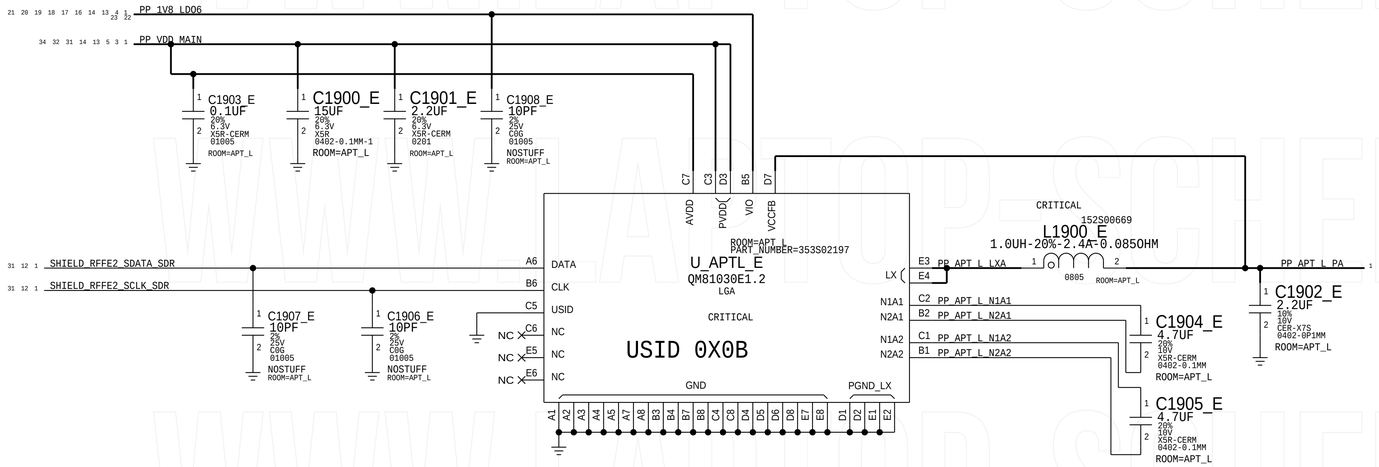

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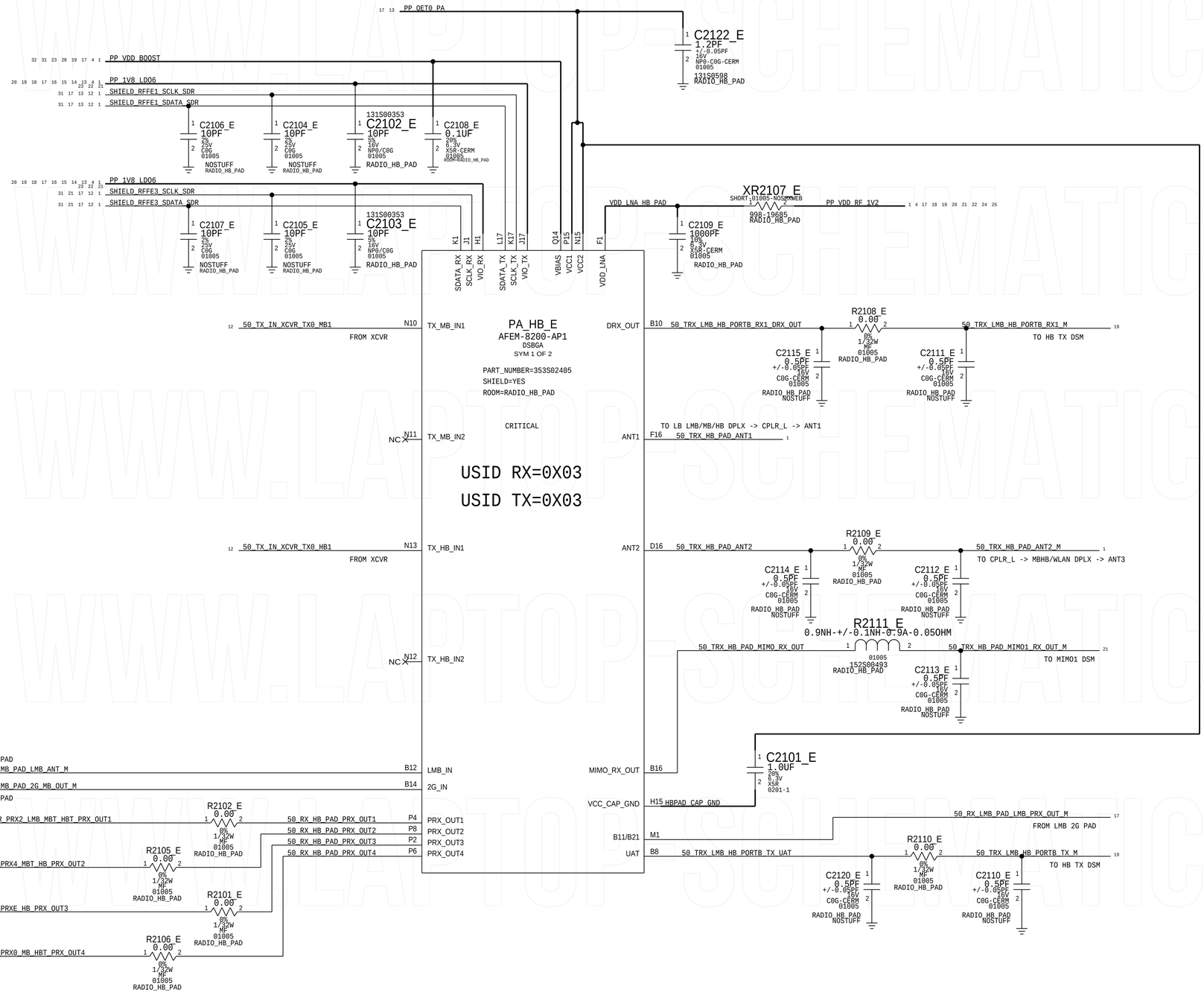

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LMB_2G_PAD

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13 PP_QET0_2G_PA

C2305_E 100PF 5% 16V NP0-C0G 01005-1 LMB_2GPAD

C2304_E 2.2UF 20% 10V X5R 0201 LMB_2GPAD

PP_VDD_BOOST

C2306_E 1.0UF 20% 10V X5R-CERM 0201-1 LMB_2GPAD

20 19 18 17 16 15 14 13 4 3 22 22 21 PP_1V8_LDO6

31 16 13 12 1 SHIELD_RFFE1_SCLK_SDR

31 16 13 12 1 SHIELD_RFFE1_SDATA_SDR

C2311_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD

C2313_E 18PF 5% 16V NP0/C0G 01005 NOSTUFF LMB_2GPAD

C2302_E 10PF 5% 25V C0G 01005 NOSTUFF LMB_2GPAD

20 19 18 17 16 15 14 13 4 3 23 22 21 PP_1V8_LDO6

31 21 16 12 1 SHIELD_RFFE3_SCLK_SDR

31 21 16 12 1 SHIELD_RFFE3_SDATA_SDR

C2312_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD

C2301_E 18PF 5% 16V NP0/C0G 01005 NOSTUFF LMB_2GPAD

C2303_E 10PF 5% 25V C0G 01005 NOSTUFF LMB_2GPAD

PP_QET0_PA 13 16

C2314_E 18PF 5% 16V NP0/C0G 01005 NOSTUFF LMB_2GPAD

XR2304_E SHORT 01005-NOSTUFF 998-19605 LMB_2GPAD

VFE_LO_1V14_LMB_PAD

C2315_E 1000PF 10% 6.3V X5R-CERM 01005 LMB_2GPAD

PP_VDD_RF_1V2 1 4 16 18 19 20 21 22 24 25

A7 SDATA_RX
A6 CLK_RX
A5 VIO_RX
J4 SDATA_TX
J3 SCLK_TX
J2 VIO_TX
F6 Z9_VAPT_1
F7 Z9_VAPT_2
H1 VBIAS
J6 VCC1
J7 VCC2
A9 VDD_LNA

PART_NUMBER=353S02393
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LMB_2GPAD

PA_LMB_E
SKY58232
DSBGA
SYM 1 OF 2

USID RX=0X05
USID TX=0X05

PA_LMB_E
SKY58232
DSBGA
SYM 2 OF 2

PART_NUMBER=353S02393
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LMB_2GPAD

A1 A2 B3 B4 B9 B10 B12 C2 C3 C9 C10 C11 A3 C12 D2 D3 D4 D12 E2 E3 E4 E11 E12 A4 F2 F3 F4 F5 F11 GND F12 G1 G2 G3 G4 A8 G5 G6 G7 G12 H2 H3 H4 H5 H6 H7 A10 H11 H12 J1 J5 J8 J9 J10 J11 J12 A11 A12 B1 B2

12 50_TX_IN_XCVR_TX0_LB2G

R2301_E 0.00 0% 1/32W MF 01005 LMB_2GPAD

FROM XCVR

50_TX_IN_XCVR_TX0_LB2_2G_LB_IN C1 2G_LB_IN

2G_LB_OUT B11 50_TRX_IN_LMB_PAD_2G_LB_OUT

R2305_E 0.9NH-+/-0.1NH-0.9A-0.05OHM 01005 LMB_2GPAD 152S00493

50_TRX_IN_LMB_PAD_2G_LB_OUT_M 1 TO LB PAD

C2307_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

12 50_TX_IN_XCVR_TX0_MB2G

R2302_E 0.00 0% 1/32W MF 01005 LMB_2GPAD

FROM XCVR

50_TX_IN_XCVR_TX0_MB2G_2G_MB_IN D1 2G_MB_IN

2G_MB_OUT D11 50_TRX_IN_LMB_PAD_2G_MB_OUT

R2306_E 0.00 0% 1/32W MF 01005 LMB_2GPAD

50_TRX_IN_LMB_PAD_2G_MB_OUT_M 16 TO HB PAD

C2308_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

NC E1 NC

LMB_ANT G11 50_TRX_IN_LMB_PAD_LMB_ANT

R2307_E 0.00 0% 1/32W MF 01005 LMB_2GPAD

50_TRX_IN_LMB_PAD_LMB_ANT_M 16 TO HB PAD

C2309_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

12 50_TX_IN_XCVR_TX0_LMB

R2303_E 0.00 0% 1/32W MF 01005 LMB_2GPAD

FROM XCVR

50_TX_IN_XCVR_TX0_LMB_TX_LMB_IN_2 F1 TX_LMB_IN

LMB_PRX_OUT C4 50_RX_LMB_PAD_LMB_PRX_OUT

R2308_E 0.00 0% 1/32W MF 01005 LMB_2GPAD

50_RX_LMB_PAD_LMB_PRX_OUT_M 16 TO HB PAD

C2310_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

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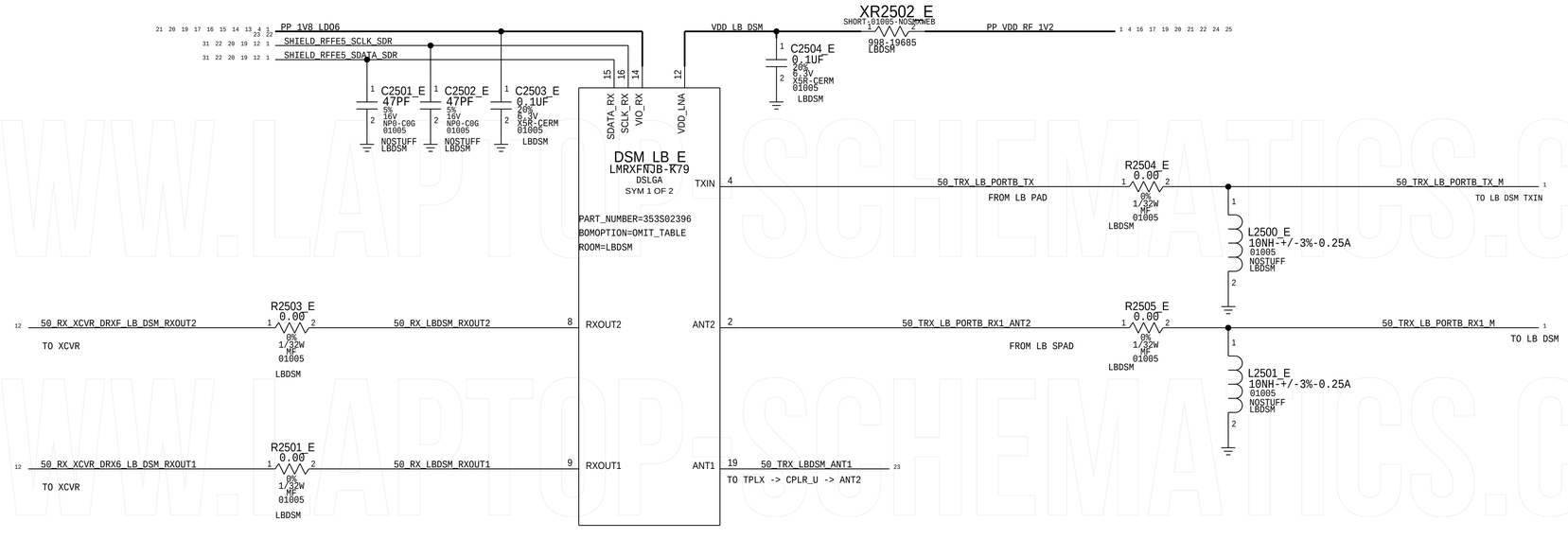
LB DIVERSITY MODULE



USID RX=0X01

PART_NUMBER=353S02396
BOMOPTION=OMIT_TABLE
ROOM=LBDSM

DSM_LB_E
LMRXFNJB-K79
DSLGA
SYM 2 OF 2

1	GND
3	GND
5	GND
6	GND
7	GND
10	GND
11	GND
13	GND
17	GND
18	GND
20	GND

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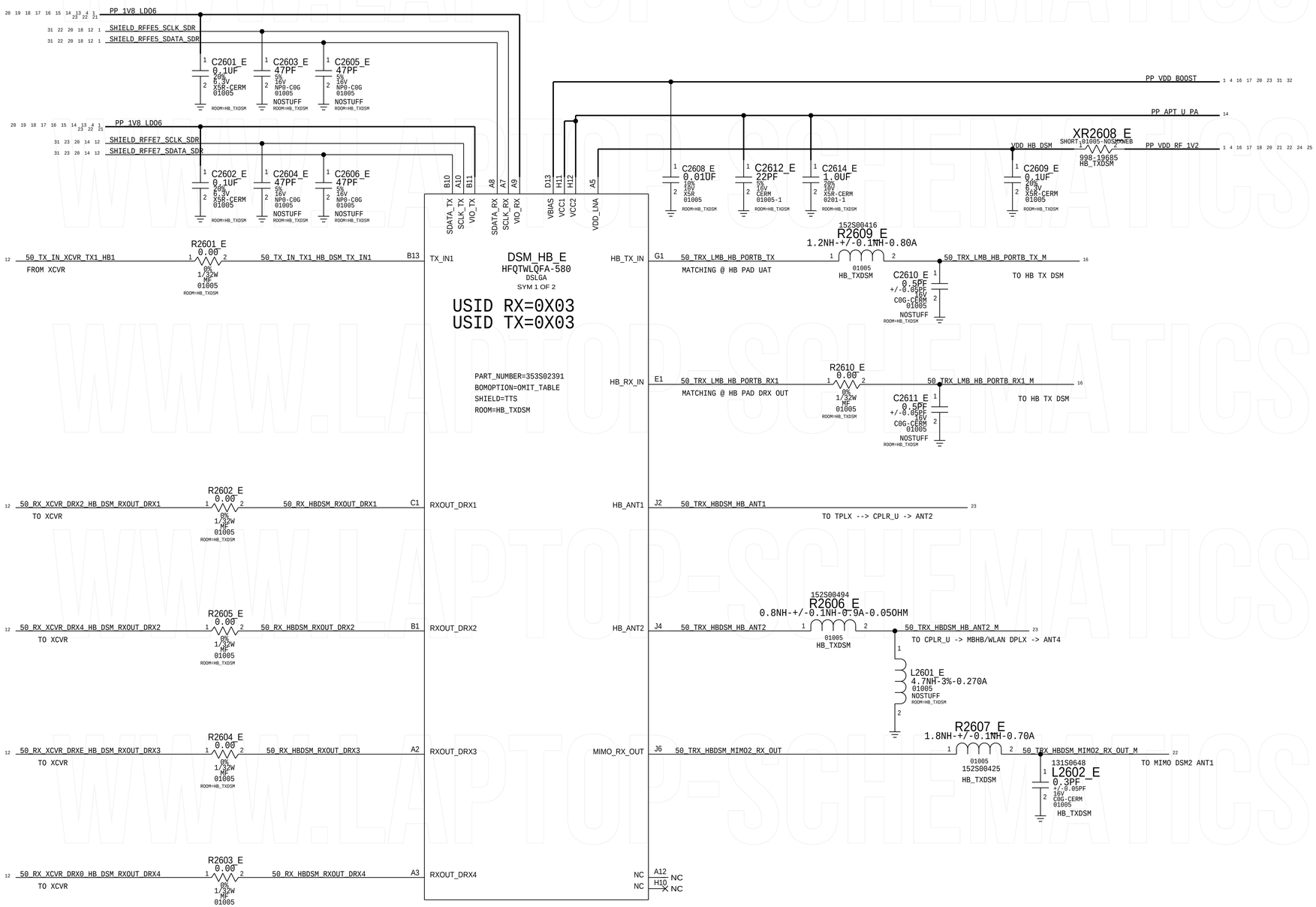
HB RECEIVE DIVERSITY & TX MODULE



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UHB DIVERSITY MODULE

PP_1V8_LDO6
SHIELD_RFFE5_SCLK_SDR
SHIELD_RFFE5_SDATA_SDR
SHIELD_RFFE7_SCLK_SDR
SHIELD_RFFE7_SDATA_SDR

C2701_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2702_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2703_E 0.1UF 20% 6.3V X5R-CERM 01005 UHB_UAT
C2721_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2722_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2723_E 0.1UF 20% 6.3V X5R-CERM 01005 UHB_UAT

DSMUHB_E
SKY53807
DSBGA
SYM 1 OF 2
PART_NUMBER=353S02390
SHIELD=TTS
ROOM=UHB_UAT

USID RX=0X06
USID RX=0X06

CRITICAL

SDATA_RX D4
SCLK_RX E4
VIO_RX C4
SDATA_TX D9
SCLK_TX E9
VIO_TX C9
VBIAS C6
NC F7
NC G7
VDD_LNA C7

NC B1
NC B12
FBRX1 E12

RX_OUT1 A3
RX_OUT2 A4
RX_OUT3 A8
RX_OUT4 A9

R2701_E 0.00 0% 1/32W MF 01005 UHB_UAT
R2703_E 0.00 0% 1/32W MF 01005 UHB_UAT
R2702_E 0.00 0% 1/32W MF 01005 UHB_UAT
R2704_E 0.00 0% 1/32W MF 01005 UHB_UAT

12 50_RX_XCVR_DRX14_UHB_DSM_UHB_RX_OUT1 → TO XCVR
50_RX_UHB_DSM_RX_OUT1
12 50_RX_XCVR_DRX12_UHB_DSM_N79_RX_OUT1 → TO XCVR
50_RX_UHB_DSM_N79_RX_OUT1
12 50_RX_XCVR_DRX15_UHB_DSM_UHB_RX_OUT2 → TO XCVR
50_RX_UHB_DSM_RX_OUT2
12 50_RX_XCVR_DRX13_UHB_DSM_N79_RX_OUT2 → TO XCVR
50_RX_UHB_DSM_N79_RX_OUT2

XR2705_E
SHORT,01005-NOSTUFF,WB 998-19685 UHB_UAT
VDD_UHB_DSM
PP_VDD_RF_1V2

C2704_E 0.1UF 20% 6.3V X5R-CERM 01005 UHB_UAT
PP_VDD_BOOST
C2706_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=UHB_UAT

UHB_ANT1 M2 50_TRX_PAUHBU_UHB_ANT1_TO_ANT4 27
TO UHB/N79 QPLX -> ANT4

UHB_ANT2 M3 50_TRX_PAUHBU_UHB_ANT2_TO_ANT8 26
TO UHB/N79 DPLX -> ANT8

UHB_ANT4 M5 50_TRX_UHB_PAD_PORTB_TX_UHB_ANT4
TO UHB UAT PAD UHB ANT 4
152S00497 R2708_E 0.5NH-+/-0.1NH-1.0A-0.040HM 01005 UHB_UAT
50_TRX_UHB_PAD_PORTB_TX_M 1
131S0370 C2708_E 0.6PF +/-0.1PF 16V NP0-C0G 01005 UHB_UAT

N79_ANT1 M7 50_TRX_PAUHBU_N79_ANT1_TO_ANT4 27
TO UHB/N79 QPLX -> ANT4

N79_ANT2 M8 50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M 1
TO UHB/N79 DPLX -> ANT8

R2709_E 0.00 0% 1/32W MF 01005 UHB_UAT
50_TRX_UHB_PAD_N79_PORTB_TX_M 1
131S00030 C2709_E 0.4PF +/-0.05PF 16V C0G 01005 UHB_UAT

N79_ANT4 M10 50_TRX_UHB_PAD_N79_PORTB_TX_N79_ANT4
TO UHB UAT PAD N79 ANT4

EXT_CPL1
NC
J12
L12
NC
NC

DSMUHB_E
SKY53807
DSBGA
SYM 2 OF 2
PART_NUMBER=353S02390
SHIELD=TTS
ROOM=UHB_UAT

CRITICAL

A1 GND, A2 GND, A5 GND, A6 GND, A7 GND, A10 GND, A11 GND, A12 GND, B2 GND, B3 GND, B4 GND, B5 GND, B6 GND, B7 GND, B8 GND, B9 GND, B10 GND, B11 GND, C1 GND, C2 GND, C3 GND, C5 GND, C8 GND, C10 GND, C11 GND, C12 GND, D1 GND, D2 GND, D3 GND, D5 GND, D6 GND, D7 GND, D8 GND, D10 GND, D11 GND, D12 GND, E1 GND, E2 GND, E3 GND, E5 GND
E6 GND, E7 GND, E8 GND, E10 GND, E11 GND, F1 GND, F2 GND, F3 GND, F4 GND, F5 GND, F6 GND, F8 GND, F9 GND, F10 GND, F11 GND, F12 GND, G1 GND, G2 GND, G3 GND, G4 GND, G5 GND, G6 GND, G8 GND, G9 GND, G10 GND, G11 GND, G12 GND, H1 GND, H12 GND, J1 GND, K1 GND, K12 GND, L1 GND, M1 GND, M4 GND, M6 GND, M9 GND, M11 GND, M12 GND

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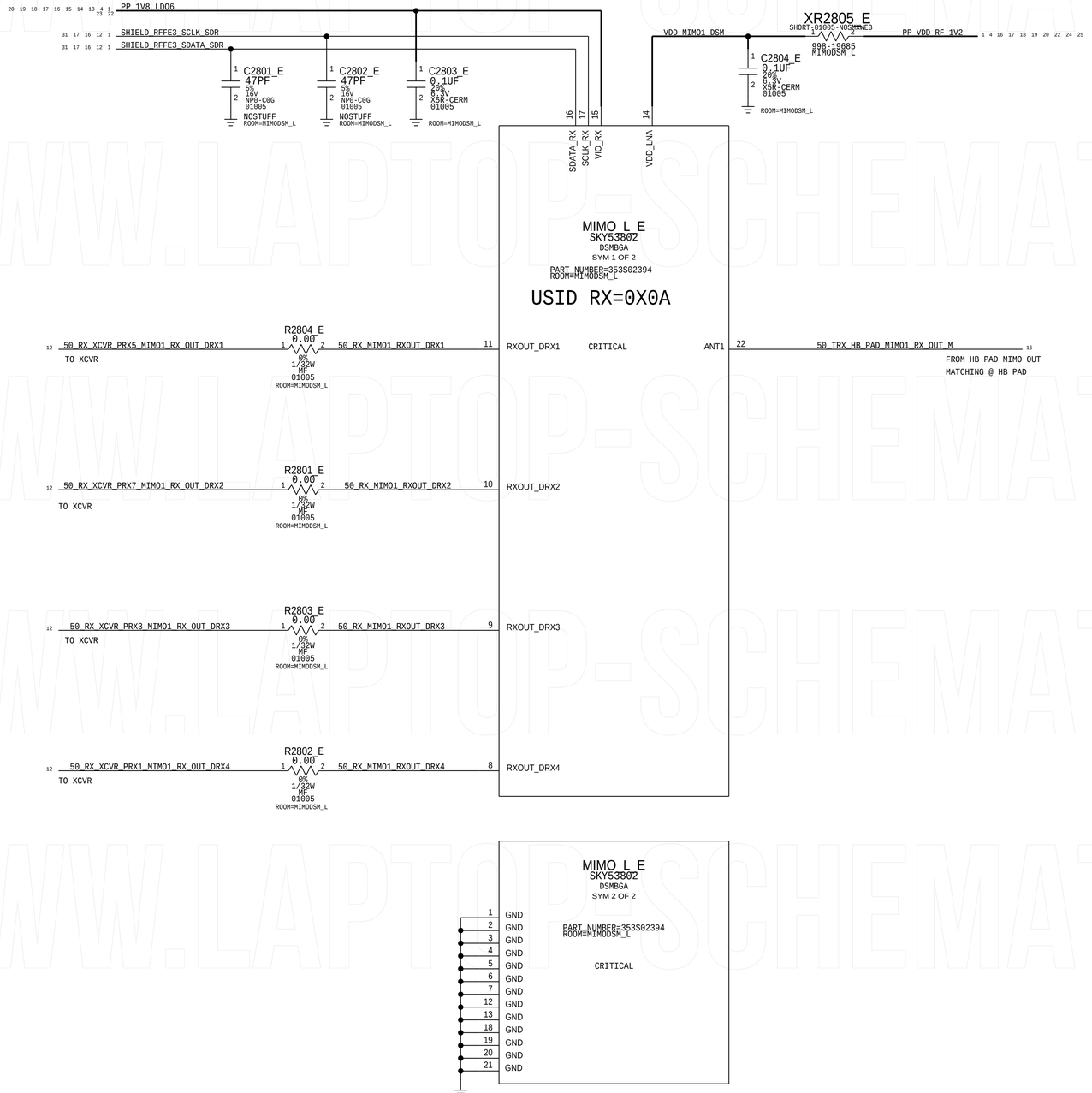

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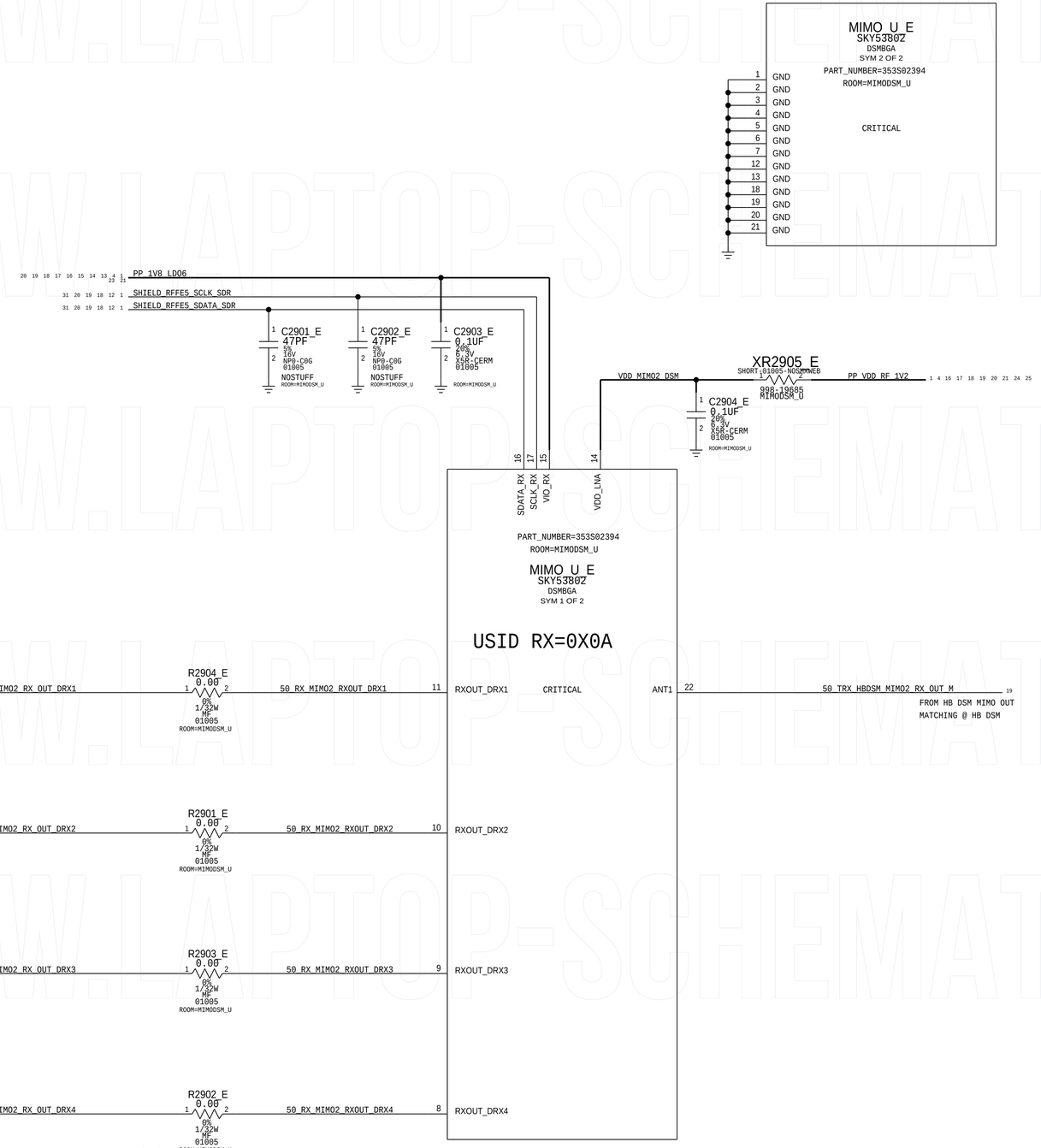
UPPER MIMO DIVERSITY MODULE



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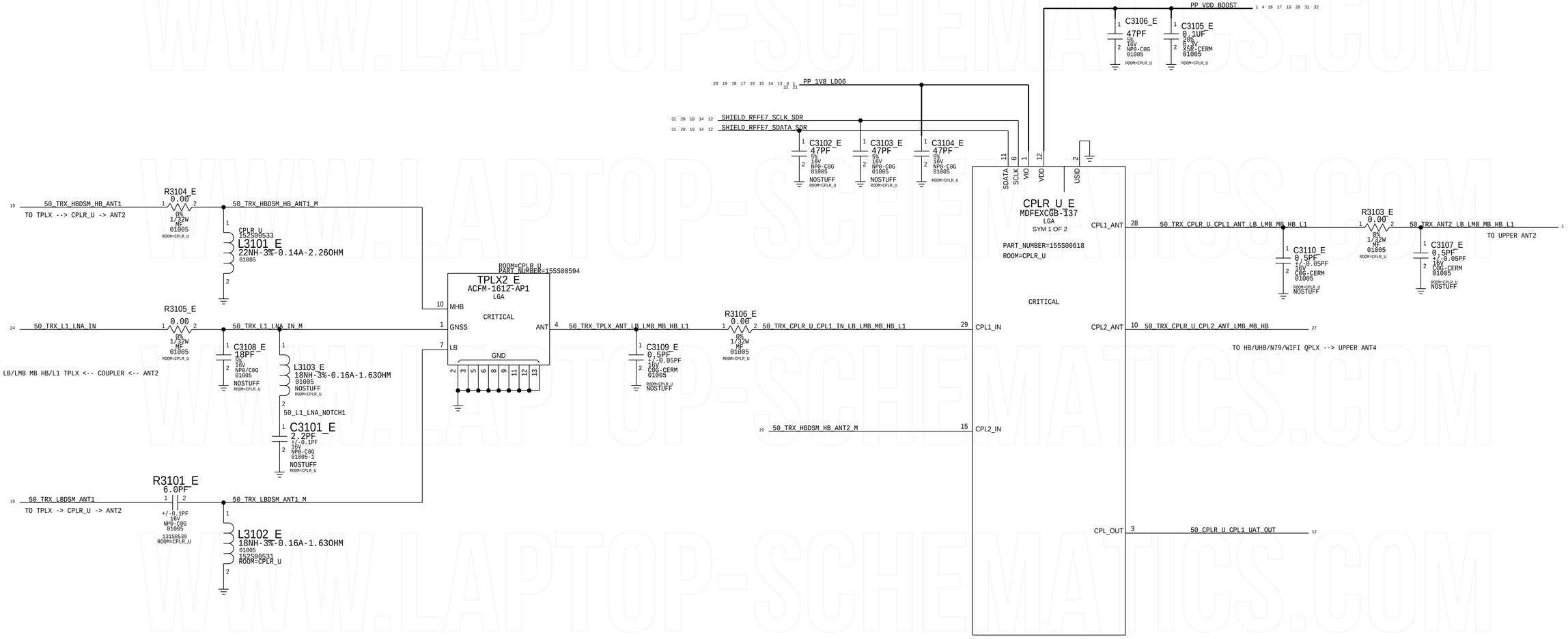
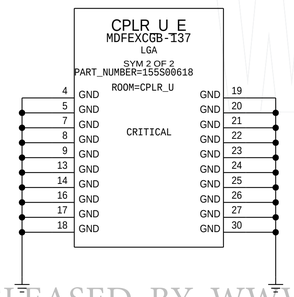
UPPER COUPLER



USID=0X08



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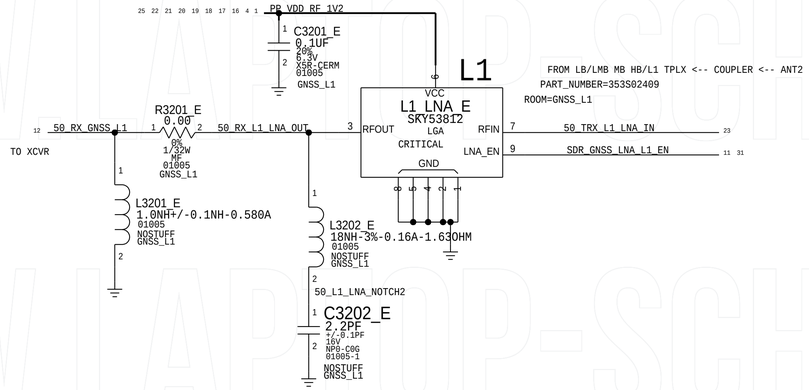
GNSS_L1



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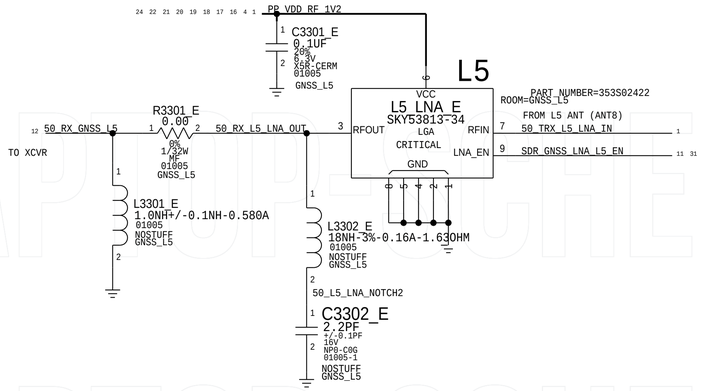
GNSS_L5



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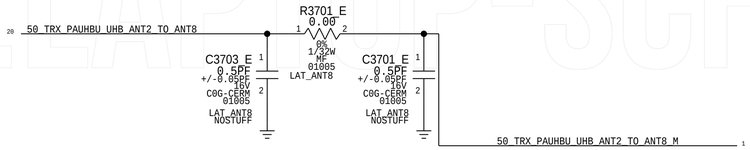
LOWER ANTENNA FEEDS: ANT8

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



ANT8

5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

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PAGE TITLE: LOWER ANTENNA FEEDS_ANT8

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REVISION: 9.0.0

BRANCH: crb-1

PAGE: 37 OF 60

SHEET: 44 OF 60

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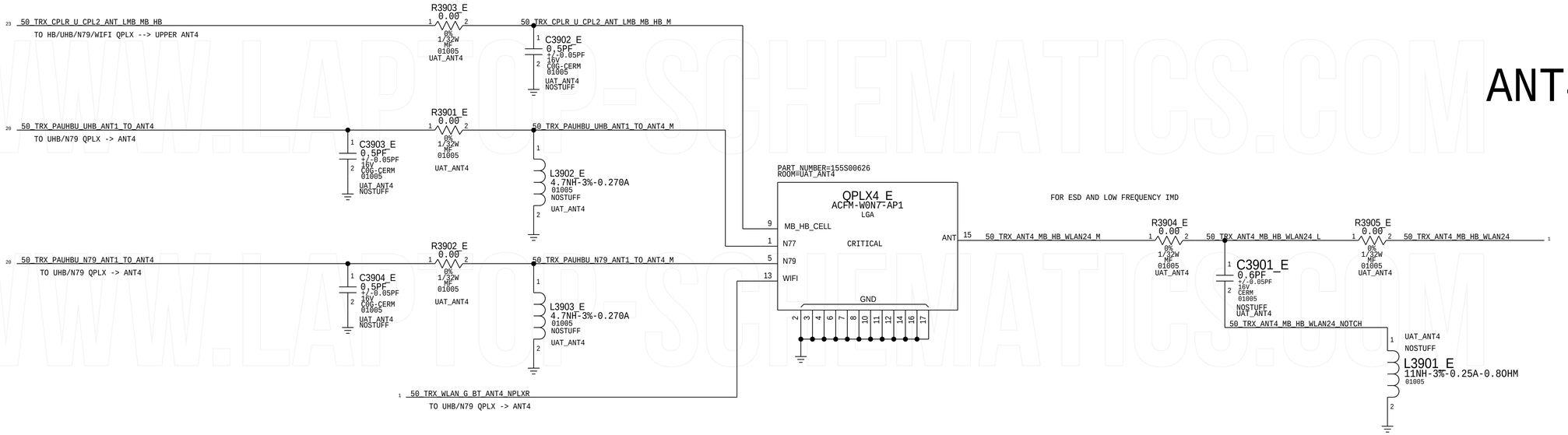
UPPER ANTENNA FEEDS



ANT4

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PHYSICAL SIM
PSIM AND ESIM ARE ON FLEX FOR BOTH D53 AND D54
D53 J_SIM (PLUG.APN:516S00659) ON MLB_BOT_MAV
D54 J_SIM (PLUG.APN:516S00635) ON MLB_TOP

SIM1 IO Filters

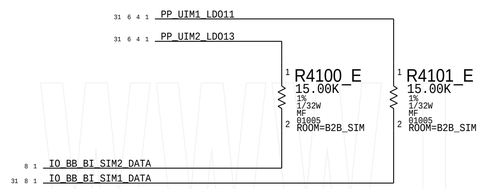
MOVE TO MLB_TOP

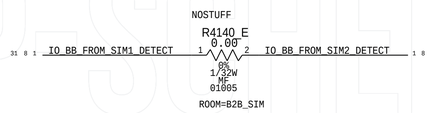
SIM2 IO Filters

MOVE TO MLB_TOP

Power Filters & Pull-ups

MOVE TWO 220PF DESENSE CAPS TO MLB_TOP





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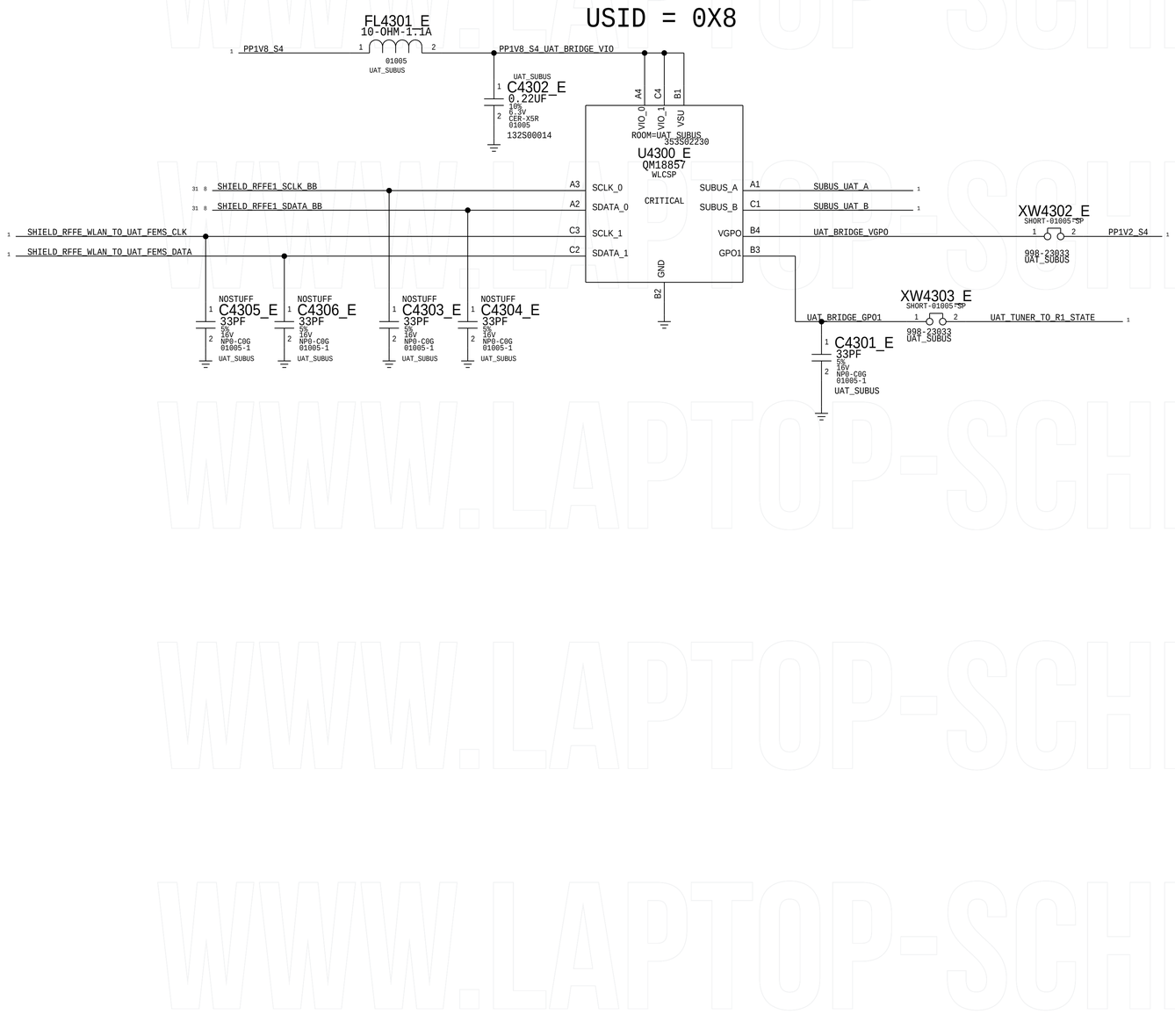
ANTENNA SYSTEM UAT



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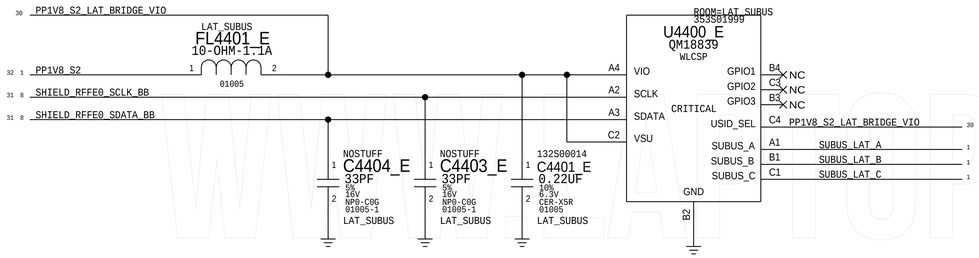
ANTENNA SYSTEM LAT

USID = 0X8 (SEL=VIO)
USID = 0XF (SEL=GND)



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DEBUG & BB PROBE POINTS

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NOSTUFF
PAYM-DEBUG
PART_NUMBER=516S00280

JDEBUG_E
BM29P-24DP-2-0.35V
M-ST-SM

34 32 31 15 14 13 5 3 1	PP_VDD_MAIN	2	1	PP_VDD_MAIN 1 3 5 13 14 15 31 32 34
32 5 1	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	4	3	PP3V0_DEBUG 32
		6	5	BB_JTAG_TDI 8
32 8	90_USB_BB_N	8	7	BB_JTAG_TDO 8
32 8	90_USB_BB_P	10	9	BB_JTAG_TRST_L 8
		12	11	BB_JTAG_RST_L 8
32 5	VBUS_DET_PMIC	14	13	UART_BB_TO_WLAN_TX 1 8
8	BB_JTAG_TCK_SWD_CLK_1V8_R	16	15	UART_BB_TO_WLAN_RX 1 8
8	BB_JTAG_TMS_SWD_IO_1V8_R	18	17	UART1_AOP_TO_BB_TXD 1 8
8 1	IO_BB_TO_SIM1_RESET	20	19	UART1_AOP_FROM_BB_RXD 1 8
28 8 1	IO_BB_FROM_SIM1_DETECT	22	21	IO_BB_TO_SIM1_CLK 1 8
31 28 6 4 1	PP_UIM1_LDO11	24	23	IO_BB_BI_SIM1_DATA 1 8 28
		26	25	
		28	27	

SDR RFFE

PP4620_E	SHIELD_RFFE1_SDATA_SDR	1 12 13 16 17
PP4700_E		
PP4621_E	SHIELD_RFFE1_SCLK_SDR	1 12 13 16 17
PP4701_E		
PP4622_E	SHIELD_RFFE2_SDATA_SDR	1 12 15
PP4702_E		
PP4623_E	SHIELD_RFFE2_SCLK_SDR	1 12 15
PP4703_E		
PP4624_E	SHIELD_RFFE3_SDATA_SDR	1 12 16 17 21
PP4704_E		
PP4625_E	SHIELD_RFFE3_SCLK_SDR	1 12 16 17 21
PP4705_E		
PP4626_E	SHIELD_RFFE5_SDATA_SDR	1 12 18 19 20 22
PP4706_E		
PP4627_E	SHIELD_RFFE5_SCLK_SDR	1 12 18 19 20 22
PP4707_E		
PP4628_E	SHIELD_RFFE7_SDATA_SDR	12 14 19 20 23
PP4708_E		
PP4629_E	SHIELD_RFFE7_SCLK_SDR	12 14 19 20 23
PP4709_E		
PP4642_E	SHIELD_RFFE8_SDATA_SDR	1 12
PP4710_E		
PP4643_E	SHIELD_RFFE8_SCLK_SDR	1 12
PP4711_E		

BB RFFE

PP4712_E	SHIELD_RFFE0_SDATA_BB	8 30
PP4713_E		
PP4714_E	SHIELD_RFFE0_SCLK_BB	8 30
PP4715_E		
PP4716_E	SHIELD_RFFE1_SDATA_BB	8 29
PP4717_E		
PP4718_E	SHIELD_RFFE1_SCLK_BB	8 29
PP4719_E		

QLINK RFFE

PP4640_E	SHIELD_RFFE4_SDATA_BB	8 12 33
PP4641_E	SHIELD_RFFE4_SCLK_BB	8 12 33

AP POWER

PP4720_E	PP_VDD_MAIN	1 3 5 13 14 15 31 32 34
PP4679_E	PP_VDD_BOOST	1 4 16 17 19 20 23 32
PP4698_E	PP3V0_S2	1 12 32

BB POWER

PP4721_E	PP_0V75_SMPS1_6	3 6
PP4722_E	PP_1V22_SMPS2	3 4
PP4723_E	基带电源输出的0.82V S3供电 PP_0V82_SMPS3	3 4 6
PP4724_E	基带电源输出的1.9V S4供电 PP_1V9_SMPS4	3 4 34
PP4725_E	基带电源输出的0.75V S5供电 PP_0V75_SMPS5	3 6
PP4726_E	基带电源输出的0.75V S7供电 PP_0V75_SMPS7	3 4 6
PP4727_E	PP_1V2_LDO1	4 6 9
PP4728_E	PP_1V1_LDO2	4 6
PP4729_E	PP_0V8_LDO3	4 10
PP4730_E	PP_0V875_LDO4	4 6 9 33
PP4731_E	PP_1V8_LDO5	4 6 33
PP4647_E	PP_1V8_LDO6	4 5 6 8 9 32 33
PP4733_E	PP_0V8_LDO7	4 33
PP4734_E	PP_0V8_LDO8	4 9
PP4735_E	PP_0V8_LDO9	4 33
PP4736_E	PP_3V1_LDO10	4 6
PP4737_E	PP_UIM1_LDO11	1 4 6 28 31
PP4738_E	PP_1V2_LDO12	4 33
PP4739_E	PP_UIM2_LDO13	1 4 6 28
PP4740_E	PP_0V6_LDO14	4 6 8
PP4741_E	PP_1V2_LDO15	4 6 32
PP4742_E	PP_1V7_LDO16	4 9

PCIE

PP4634_E	CPU到基带的PCIE总线数据发射P 90_PCIE_GP2_AP_TO_BB_TX_P	1 8
PP4635_E	CPU到基带的PCIE总线数据发射N 90_PCIE_GP2_AP_TO_BB_TX_N	1 8
PP4636_E	CPU到基带的PCIE总线数据接收P 90_PCIE_GP2_AP_FROM_BB_RX_P	1 8
PP4637_E	CPU到基带的PCIE总线数据接收N 90_PCIE_GP2_AP_FROM_BB_RX_N	1 8
PP4638_E	CPU到基带的PCIE总线时钟P 90_PCIE_GP2_AP_TO_BB_REFCLK_P	1 8
PP4639_E	CPU到基带的PCIE总线时钟N 90_PCIE_GP2_AP_TO_BB_REFCLK_N	1 8
PP4684_E	电源到基带的PCIE总线唤醒信号 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	1 8 32
PP4685_E	PCIE_GP2_AP_TO_BB_PERST_L	1 8
PP4686_E	CPU到基带的PCIE总线复位 PCIE_GP2_AP_BI_BB_CLKREQ_L	1 8 32

基带到CPU的PCIE总线时钟请求

CLOCKS

PP4651_E	基带时钟芯片到基带 19.2MHz时钟 SHIELD_MDM_19P2M_CLK	5 8
PP4690_E	基带时钟芯片到射频38.4MHz时钟 SHIELD_SDR_38P4M_CLK	5 12
PP4608_E	SHIELD_SMR_38P4M_CLK	5 33
PP4609_E	基带时钟芯片到无线充电芯片38.4MHz时钟 CLK_BBPMU_TO_DOTARA_38M4_R	1 5
PP4610_E	CLK_BBPMU_TO_NFC_38M	1 5
PP4611_E	SHIELD_PMK_32K_SLEEP_CLK	5
PP4612_E	基带电源到基带的32KHz时钟 SHIELD_SLEEP_CLK_32K	5 8

DOTARA

PP4632_E	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	6

CPU到基带电源时钟开启信号

I2S

PP4693_E	CPU到基带的I2S2总线数据 I2S2_AP_TO_BB_DOUT	1 8
PP4694_E	基带到CPU的I2S1总线串行时钟 I2S2_AP_FROM_BB_BCLK	1 8
PP4695_E	基带到CPU的I2S2总线数据 I2S2_AP_FROM_BB_DIN	1 8
PP4696_E	I2S2_AP_FROM_BB_LRCLK	1 8

基带到CPU的I2S1总线帧时钟

BASEBAND

PP4652_E	CPU到基带的纠错信号 GPIO_AP_TO_BB_COREDUMP	1 8
PP4658_E	CPU到基带时间标记信号 GPIO_AP_TO_BB_TIME_MARK	1 8
PP4655_E	基带到基带电源SPMI总线时钟 BB_BBPMU_SPMI_CLK	5 8
PP4656_E	BB_BBPMU_SPMI_DATA	5 8
PP4671_E	BB_EEPROM_I2C_SCL	8
PP4672_E	BB_EEPROM_I2C_SDA	8
PP4653_E	IO_TOUCH_TO_MANY_SCAN_ACTIVE	1 5
PP4654_E	CPU到基带强制调节信号 GPIO_AOP_TO_BB_FORCE_PWM	1 5
PP4687_E	CPU到基带的复位检测 GPIO_AP_FROM_BB_RESET_DETECT_L	1 8
PP4688_E	PMIC_RESOUT_L	5 8
PP4689_E	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	1 8
PP4600_E	GPIO_AP_TO_BB_PEAK_PWR_IND	1 8
PP4660_E	PS_HOLD	5 8
PP4644_E	PP_PMX_VIO_OUT	5 6
PP4743_E	BOOT_CFG1	8 32
PP4744_E	BOOT_CFG2	8 32
PP4732_E	BB_TO_SDR_WMSS_RESET_L	8 11
PP4745_E	BB_TO_SMR_WMSS_RESET_L	8 33

SWD

PP4691_E	CPU输出的SWD总线时钟 SWD_AP_TO_MANY_SWCLK	1 8
PP4692_E	SWD_AP_BI_BB_SWDIO	1 8

CPU到基带的SWD总线数据

QLINK

PP4681_E	QLINK_REQ_SDR_TO_BB	8 11
PP4682_E	QLINK_EN_BB_TO_SDR	8 11
PP4683_E	QLINK_REQ_SMR_TO_BB	8 33
PP4605_E	QLINK_EN_BB_TO_SMR	8 33
PP4601_E	85_SUB6_QLINK_L0_P	8 11
PP4602_E	85_SUB6_QLINK_L0_N	8 11
PP4603_E	85_MMW_QLINK_L0_P	8 33
PP4604_E	85_MMW_QLINK_L0_N	8 33

R1

PP4661_E	GPIO_BB_TO_R1_COEX	1 8
PP4662_E	GPIO_BB_TO_R1_CH9_REQ	1 8
PP4668_E	GPIO_R1_TO_BB_CH9_COEX	1 8
PP4669_E	GPIO_R1_TO_BB_LAA_SW_CTRL	8

STOCKHOLM

PP4670_E	GPIO_NFC_TO_BBPMU_CLK_EN	1 5

GNSS

PP4645_E	SDR_GNSS_LNA_L1_EN	11 24
PP4646_E	SDR_GNSS_LNA_L5_EN	11 25

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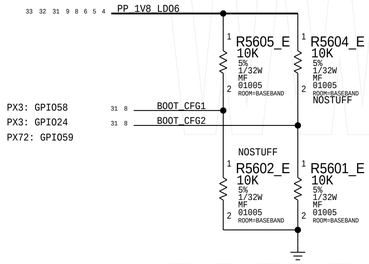
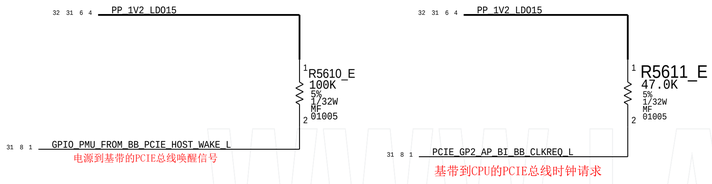
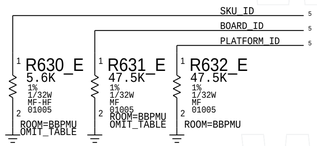


BOOT SEQ	BOOT_CFG3	BOOT_CFG2	BOOT_CFG1	CONFIG
NAND>HSUSB	0	0	0	
PCIE	0	0	1	POR
USB	0	1	0	EUREKA
EMMC>USB	0	1	1	

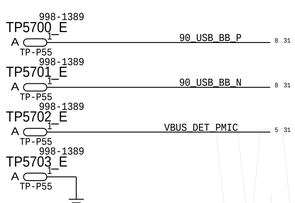
POR PCIE BOOT:
BOOT_CFG2 PD, BOOT_CFG1 PU

EUREKA CONFIG USB BOOT:
BOOT_CFG2 PU, BOOT_CFG1 PD

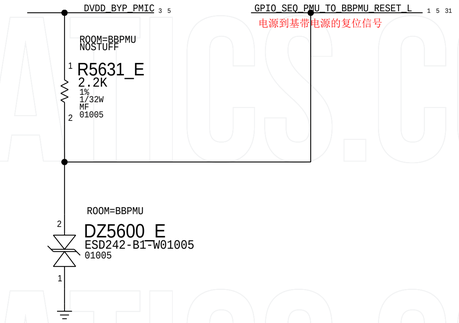




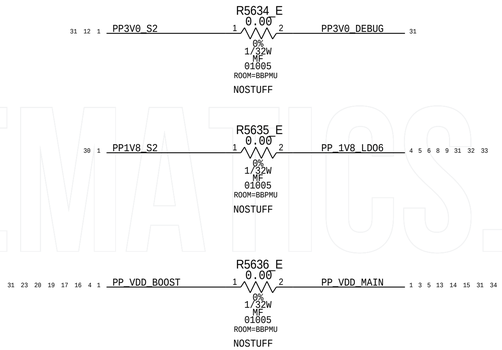
USB TP FOR TEXT FIXTURE



AUTO POWER ON FOR EUREKA CONFIG
+ BB PMU ESD DIODE PROTECTION



STUFF ONLY FOR VENDOR CONFIG



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MMW IF TRANSCEIVER IC

1.2A VDD_CX MAX CURRENT

PP_0V8_LDO7

C5801_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC

BOMOPTION=RF_SKU:NAMM

C5804_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5807_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5809_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5830_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

XW5801_E SHORT-8L-0.1MM-SM

PP_1V8_LDO6

C5802_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

PP_LDO6_SMR_VDD_PX_20

C5805_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC RF_SKU:NAMM

XW5824_E SHORT-8L-0.25MM-SM

PP_0V875_LDO4

C5803_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

PP_LDO4_SMR_MX_115

XW5825_E SHORT-8L-0.25MM-SM

PP_LDO4_SMR_PHY_152

C5806_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC RF_SKU:NAMM

C5808_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC RF_SKU:NAMM

PART_NUMBER=338S00651
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 2 OF 3
CRITICAL

B12	VDD_CX	VDDAH_1	A7
F12	VDD_CX	VDDAH_2	H4
M14	VDD_CX	VDDAH_3	P2
R7	VDD_CX	VDDAH_4	H8
P10	VDD_PX	VDDAL_1	C5
P12	VDD_MX	VDDAL_2	B4
H18	VDDA_PHY	VDDAL_3	F4
		VDDAL_4	R5
		VDDAL_5	B10
		VDDAL_6	E11
		VDDAL_7	R9
		VDDAM_1	B6
		VDDAM_2	G5
		VDDAM_3	P4
		VDDAM_4	A9
		VDDAM_5	P8

XW5802_E SHORT-8L-0.1MM-SM — PP_LDO5_SMR_VDDAH_1_10 — PP_1V8_LDO5

XW5803_E SHORT-8L-0.25MM-SM — PP_LDO5_SMR_VDDAH_2_140

XW5804_E SHORT-8L-0.1MM-SM — PP_LDO5_SMR_VDDAH_3_10

XW5805_E SHORT-8L-0.1MM-SM — PP_LDO5_SMR_VDDAH_4_40

C5823_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

C5812_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5814_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5818_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5820_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

XW5806_E SHORT-8L-0.1MM-SM — PP_LDO9_SMR_VDDAL_1_50 — PP_0V8_LDO9

XW5807_E SHORT-8L-0.1MM-SM — PP_LDO9_SMR_VDDAL_2_10

XW5808_E SHORT-8L-0.25MM-SM — PP_LDO9_SMR_VDDAL_3_140

XW5809_E SHORT-8L-0.1MM-SM — PP_LDO9_SMR_VDDAL_4_90

XW5810_E SHORT-8L-0.1MM-SM — PP_LDO9_SMR_VDDAL_5_10

XW5811_E SHORT-8L-0.1MM-SM — PP_LDO9_SMR_VDDAL_6_10

XW5812_E SHORT-8L-0.1MM-SM — PP_LDO9_SMR_VDDAL_7_10

C5828_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

C5810_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5813_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5816_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5819_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5822_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5825_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5826_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PLACE C5813 CLOSE TO PIN B4

XW5813_E SHORT-8L-0.1MM-SM — PP_LDO12_SMR_VDDAM_1_70 — PP_1V2_LDO12

XW5814_E SHORT-8L-0.25MM-SM — PP_LDO12_SMR_VDDAM_2_120

XW5815_E SHORT-8L-0.1MM-SM — PP_LDO12_SMR_VDDAM_3_70

VDDAM_4:0.24A

VDDAM_5:0.24A

VDD_AM MAX CURRENT 740 MA

C5827_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

C5811_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5815_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5817_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5821_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5824_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PART_NUMBER=338S00651
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 1 OF 3
CRITICAL

	SHIELD_SMR_38P4M_CLK	A3	XO_IN	XO	
		G9	XO_SEL		
		J1	IFH1	IF	
34	50_MMW_SMR526_IFH2	K2	IFH2		
34	50_MMW_SMR526_IFH3	L1	IFH3		
		M2	IFH4		
		F2	IFV1		
34	50_MMW_SMR526_IFV2	E1	IFV2		
34	50_MMW_SMR526_IFV3	D2	IFV3		
		C1	IFV4		
34	SMR_TO_FEZ_PON	P6	GRFC_1_QTM3_PON	GRFC	QLINK PHY
		G7	GRFC_2_QTM0_PON		
		K10	GRFC_3		
		J7	GRFC_4_QTM1_PON		
34	SMR_TO_TANGIER_PON	N5	GRFC_5_QTM2_PON		
		D12	GRFC_6		
		M12	GRFC_7		
		N11	GRFC_8		
		H12	GRFC_9		
		J11	GRFC_10		
31 12 8	SHIELD_RFFE4_SDATA_BB	K12	RFFE0_DATA	RFFE	
31 12 8	SHIELD_RFFE4_SCLK_BB	L11	RFFE0_CLK		
		C11	DNC	DNC	
31 8	QLINK_REQ_SMR_TO_BB	D14	QLINK_REQ		
31 8	QLINK_EN_BB_TO_SMR	G13	QLINK_EN		
31 8	BB_TO_SMR_WMSS_RESET_L	J13	WMSS_RESET*		

QLINK_L0_P	K14	85_MMW_QLINK_L0_P	8 31
QLINK_L0_M	J15	85_MMW_QLINK_L0_N	8 31
QLINK_L1_P	G15	85_MMW_QLINK_L1_P	8
QLINK_L1_M	F14	85_MMW_QLINK_L1_N	8
QLINK_L2_P	E15	85_MMW_QLINK_L2_P	8
QLINK_L2_M	D16	85_MMW_QLINK_L2_N	8
QLINK_L3_P	L15	85_MMW_QLINK_L3_P	8
QLINK_L3_M	M16	85_MMW_QLINK_L3_N	8
QLINK_L4_P	P16	85_MMW_QLINK_L4_P	8
QLINK_L4_M	R15	85_MMW_QLINK_L4_N	8
QLINK_L5_P	D18	85_MMW_QLINK_L5_P	8
QLINK_L5_M	E17	85_MMW_QLINK_L5_N	8
QLINK_L6_P	B16	85_MMW_QLINK_L6_P	8
QLINK_L6_M	A15	85_MMW_QLINK_L6_N	8
QLINK_L7_P	K18	85_MMW_QLINK_L7_P	8
QLINK_L7_M	J17	85_MMW_QLINK_L7_N	8
QLINK_L8_P	L17	85_MMW_QLINK_L8_P	8
QLINK_L8_M	M18	85_MMW_QLINK_L8_N	8
QLINK_L9_P	P18	85_MMW_QLINK_L9_P	8
QLINK_L9_M	R17	85_MMW_QLINK_L9_N	8
QLINK_L10_P	A13	85_MMW_QLINK_L10_P	8
QLINK_L10_M	B14	85_MMW_QLINK_L10_N	8
QLINK_L11_P	B18	85_MMW_QLINK_L11_P	8
QLINK_L11_M	A17	85_MMW_QLINK_L11_N	8
QLINK_L12_P	R13	85_MMW_QLINK_L12_P	8
QLINK_L12_M	P14	85_MMW_QLINK_L12_N	8
QLINK_CLK_P	G17	85_MMW_QLINK_CLK_P	8
QLINK_CLK_M	F18	85_MMW_QLINK_CLK_N	8

PART_NUMBER=338S00651
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 3 OF 3
CRITICAL

A1	GND	GND	H10
A5	GND	GND	H14
A11	GND	GND	H16
B2	GND	GND	J3
B8	GND	GND	J5
C3	GND	GND	J9
C7	GND	GND	K4
C9	GND	GND	K6
C13	GND	GND	K8
C15	GND	GND	K16
C17	GND	GND	L3
D4	GND	GND	L5
D6	GND	GND	L7
D8	GND	GND	L9
D10	GND	GND	L13
E3	GND	GND	M4
E5	GND	GND	M6
E7	GND	GND	M8
E9	GND	GND	M10
E13	GND	GND	N1
F6	GND	GND	N3
F8	GND	GND	N7
F10	GND	GND	N9
F16	GND	GND	N13
G1	GND	GND	N15
G3	GND	GND	N17
G11	GND	GND	R1
H2	GND	GND	R3
H6	GND	GND	R11

SYNC_DATE=08/01/2019

PAGE TITLE: MMW

DRAWING NUMBER: 051-05263 SIZE: D
REVISION: 9.0.0
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TANGIER SIP

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 1 OF 4
CRITICAL

33 SMR_TO_TANGIER_PON
117S0158
R5932_E 100K 5% 1/32W MF 01005
ROOM=MMW_SIP
BOMOPTION=RF_SKU:NAMM

PP5901_E TANGIER_TP1	386	TP1	50_RFH_Q1_39G_S1 209 50_MMW_SMR525_S1H_HPOL 35
PP5902_E TANGIER_TP2	379	TP2	50_RFH_Q1_28G_S1 208 50_MMW_SMR525_S1L_HPOL 35
PP5903_E TANGIER_TP3	380	TP3	50_RFH_Q1_39G_S2 210 50_MMW_SMR525_S2H_HPOL 35
PP5904_E TANGIER_TP4	319	TP4	50_RFH_Q1_28G_S2 211 50_MMW_SMR525_S2L_HPOL 35
PP5905_E TANGIER_TP5	378	TP5	50_RFH_Q1_39G_S3 335
PP5906_E TANGIER_TP6	375	TP6	50_RFH_Q1_28G_S3 334
PP5907_E TANGIER_TP7	376	TP7	50_RFH_Q1_39G_S4 336
PP5908_E TANGIER_RFFE_CLK	358	RFFE_CLK	50_RFH_Q1_28G_S4 337
PP5909_E TANGIER_RFFE_DATA	377	RFFE_DATA	
PP5910_E 50_TANGIER_TP11	298	TP11	
33 50_MMW_SMR526_IFH2	373	50_IF1_H	50_RFH_Q2_39G_S5 206 50_MMW_SMR525_S5H_HPOL 35
33 50_MMW_SMR526_IFV3	382	50_IF2_V	50_RFH_Q2_28G_S5 207 50_MMW_SMR525_S5L_HPOL 35
			50_RFH_Q2_39G_S6 205 50_MMW_SMR525_S6H_HPOL 35
			50_RFH_Q2_28G_S6 204 50_MMW_SMR525_S6L_HPOL 35
			50_RFH_Q2_39G_S7 332 50_MMW_SMR525_S7H_HPOL 34
			50_RFH_Q2_28G_S7 333 50_MMW_SMR525_S7L_HPOL 34
			50_RFH_Q2_39G_S8 331 50_MMW_SMR525_S8H_HPOL 34
			50_RFH_Q2_28G_S8 330 50_MMW_SMR525_S8L_HPOL 34
PP_VDD_MAIN	68	VBATT	50_RFV_Q3_39G_S9 216 50_MMW_SMR525_S9H_VPOL 35
	69	VBATT	50_RFV_Q3_28G_S9 217 50_MMW_SMR525_S9L_VPOL 35
	90	VBATT	50_RFV_Q3_39G_S10 215 50_MMW_SMR525_S10H_VPOL 35
	91	VBATT	50_RFV_Q3_28G_S10 214 50_MMW_SMR525_S10L_VPOL 35
	92	VBATT	50_RFV_Q3_39G_S11 342 50_MMW_SMR525_S11H_VPOL 34
PP_1V9_SMPS4 MAKE_BASE=TRUE	42	VDD_IO_1V85	50_RFV_Q3_28G_S11 343 50_MMW_SMR525_S11L_VPOL 34
			50_RFV_Q3_39G_S12 341 50_MMW_SMR525_S12H_VPOL 34
			50_RFV_Q3_28G_S12 340 50_MMW_SMR525_S12L_VPOL 34
			50_RFV_Q4_39G_S13 219 50_MMW_SMR525_S13H_VPOL 35
			50_RFV_Q4_28G_S13 218 50_MMW_SMR525_S13L_VPOL 35
			50_RFV_Q4_39G_S14 220 50_MMW_SMR525_S14H_VPOL 35
			50_RFV_Q4_28G_S14 221 50_MMW_SMR525_S14L_VPOL 35
			50_RFV_Q4_39G_S15 345
			50_RFV_Q4_28G_S15 344
			50_RFV_Q4_39G_S16 346
			50_RFV_Q4_28G_S16 347

C5901_E 100PPF 5% 16V NP0-C0G 01005-1 131S00303 BOMOPTION=RF_SKU:NAMM ROOM=MMW_SIP

C5902_E 100PF 5% 16V NP0-C0G 01005-1 131S00303 ROOM=MMW_SIP

基带电源输出的1.9V S4供电

BOMOPTION=RF_SKU:NAMM

SMYRNA

PART_NUMBER=518S00234
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

J_SMYR_E
MM3631-2703A16
F-ST-SM

34 50_MMW_SMR525_S11L_VPOL	2	9	50_MMW_SMR525_S11H_VPOL 34
34 50_MMW_SMR525_S7L_HPOL	4	11	50_MMW_SMR525_S7H_HPOL 34
34 50_MMW_SMR525_S12H_VPOL	6	13	50_MMW_SMR525_S8L_HPOL 34
34 50_MMW_SMR525_S8H_HPOL	8	15	50_MMW_SMR525_S12L_VPOL 34

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 2 OF 4
CRITICAL

1 GND	GND	66	136 GND	GND	200
2 GND	GND	67	137 GND	GND	201
3 GND	GND	70	138 GND	GND	202
4 GND	GND	71	139 GND	GND	203
5 GND	GND	72	140 GND	GND	212
6 GND	GND	73	141 GND	GND	213
7 GND	GND	74	142 GND	GND	222
8 GND	GND	75	143 GND	GND	223
9 GND	GND	76	144 GND	GND	224
10 GND	GND	77	145 GND	GND	225
11 GND	GND	78	146 GND	GND	226
12 GND	GND	80	147 GND	GND	227
13 GND	GND	81	148 GND	GND	228
14 GND	GND	82	149 GND	GND	229
15 GND	GND	83	150 GND	GND	230
16 GND	GND	84	151 GND	GND	231
17 GND	GND	85	152 GND	GND	232
18 GND	GND	86	153 GND	GND	233
19 GND	GND	87	154 GND	GND	234
20 GND	GND	88	155 GND	GND	235
21 GND	GND	89	156 GND	GND	236
22 GND	GND	93	157 GND	GND	237
23 GND	GND	94	158 GND	GND	238
24 GND	GND	95	159 GND	GND	239
25 GND	GND	96	160 GND	GND	240
26 GND	GND	97	161 GND	GND	241
27 GND	GND	98	162 GND	GND	242
28 GND	GND	99	163 GND	GND	243
29 GND	GND	100	164 GND	GND	244
30 GND	GND	101	165 GND	GND	245
31 GND	GND	102	166 GND	GND	246
32 GND	GND	103	167 GND	GND	247
33 GND	GND	104	168 GND	GND	248
34 GND	GND	105	169 GND	GND	249
35 GND	GND	106	170 GND	GND	250
36 GND	GND	107	171 GND	GND	251
37 GND	GND	108	172 GND	GND	252
38 GND	GND	109	173 GND	GND	253
39 GND	GND	110	174 GND	GND	254
40 GND	GND	111	175 GND	GND	255
41 GND	GND	112	176 GND	GND	256
43 GND	GND	113	177 GND	GND	257
44 GND	GND	114	178 GND	GND	258
45 GND	GND	115	179 GND	GND	259
46 GND	GND	116	180 GND	GND	260
47 GND	GND	117	181 GND	GND	261
48 GND	GND	118	182 GND	GND	262
49 GND	GND	119	183 GND	GND	263
50 GND	GND	120	184 GND	GND	264
51 GND	GND	121	185 GND	GND	265
52 GND	GND	122	186 GND	GND	266
53 GND	GND	123	187 GND	GND	267
54 GND	GND	124	188 GND	GND	268
55 GND	GND	125	189 GND	GND	269
56 GND	GND	126	190 GND	GND	270
57 GND	GND	127	191 GND	GND	271
58 GND	GND	128	192 GND	GND	272
59 GND	GND	129	193 GND	GND	273
60 GND	GND	130	194 GND	GND	274
61 GND	GND	131	195 GND	GND	275
62 GND	GND	132	196 GND	GND	276
63 GND	GND	133	197 GND	GND	277
64 GND	GND	134	198 GND	GND	278
65 GND	GND	135	199 GND	GND	279

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 3 OF 4
CRITICAL

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 4 OF 4
CRITICAL

GND	GND	280	323 GND
GND	GND	281	324 GND
GND	GND	282	325 GND
GND	GND	283	326 GND
GND	GND	284	327 GND
GND	GND	285	328 GND
GND	GND	286	329 GND
GND	GND	287	338 GND
GND	GND	288	339 GND
GND	GND	289	348 GND
GND	GND	290	349 GND
GND	GND	291	350 GND
GND	GND	292	351 GND
GND	GND	293	352 GND
GND	GND	294	353 GND
GND	GND	295	354 GND
GND	GND	296	355 GND
GND	GND	297	356 GND
GND	GND	299	357 GND
GND	GND	300	359 GND
GND	GND	301	360 GND
GND	GND	302	361 GND
GND	GND	303	362 GND
GND	GND	304	363 GND
GND	GND	305	364 GND
GND	GND	306	365 GND
GND	GND	307	366 GND
GND	GND	308	367 GND
GND	GND	309	368 GND
GND	GND	310	369 GND
GND	GND	311	370 GND
GND	GND	312	371 GND
GND	GND	313	372 GND
GND	GND	314	374 GND
GND	GND	315	381 GND
GND	GND	316	383 GND
GND	GND	317	384 GND
GND	GND	318	385 GND
GND	GND	320	387 GND
GND	GND	321	388 GND
GND	GND	322	

SIDE FIRE

PP_VDD_MAIN

ROOM=MMW_SIP
BOMOPTION=RF_SKU:NAMM
155S00373
FL5911_E FERR-33-OHM-25%-3.5A 0402
PP_VBAT_FEZ

C5911_E 100PF 5% 16V NP0-C0G 01005-1 131S00303 BOMOPTION=RF_SKU:NAMM ROOM=MMW_SIP

C5912_E 220PF 5% 25V C0G 01005 NOSTUFF ROOM=MMW_SIP

BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

J_FEZ_E
SMT-FLEX-FEZ-3L-X1804
SMT-PAD

1	GND0	
2	GND1	
3	GND2	
4	PON	
5	GND3	
6	IFV	
7	GND4	
8	1P85V	
9	GND5	
10	GND6	
11	GND7	
12	VBAT0	
13	GND8	
14	GND9	
15	GND10	
16	VBAT1	
17	GND11	
18	IFH	
19	GND12	
20	VBAT2	
21	GND13	
22	GND14	
23	GND15	
24	VBAT3	

0R HOLDERS

33 50_MMW_SMR526_IFV2
33 50_MMW_SMR526_IFH3

50_MMW_SMR526_IFH3 NET CONNECTS TO 50_IF1_H AND
50_MMW_SMR526_IFV2 NET CONNECTS TO 50_IF2_V IN FEZ FLEX

ROOM=MMW_SIP
BOMOPTION=RF_SKU:NAMM
155S00402
FL5921_E FERR-33OHM-25%-1.5A 0201
PP_1V9_SMPS4

1.85V
PP_1V85_FEZ

C5921_E 68PF 5% 16V NP0/C0G 01005 131S00385 ROOM=MMW_SIP

C5922_E 220PF 5% 25V C0G 01005 NOSTUFF ROOM=MMW_SIP

基带电源输出的1.9V S4供电

BOMOPTION=RF_SKU:NAMM

ROOM=MMW_SIP
FL5931_E 0.00 0% 1/32W MF 01005
33 SMR_TO_FEZ_PON
V_PON_FEZ

117S0158
R5931_E 100K 5% 1/32W MF 01005
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP
BOMOPTION=RF_SKU:NAMM

SAISS FLEX SHOULD BE ASSEMBLED WITH APN:632-03619

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PAGE TITLE: TANGIER SIP

DRAWING NUMBER: 051-05263
SIZE: D
REVISION: 9.0.0
BRANCH: crb-1
PAGE: 59 OF 60
SHEET: 52 OF 60

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BG1 ARRAY

PART_NUMBER=339M00116
BOMOPTION=RF_SKU:NAMM
ROOM=BG1

U_BG1_E
MWNP01SEMA01
LGA
SYM 1 OF 3
CRITICAL

34	50_MMW_SMR525_S6L_HPOL	244	50_LB1_H	50_HB1_H	235	50_MMW_SMR525_S6H_HPOL	34
34	50_MMW_SMR525_S14L_VPOL	236	50_LB1_V	50_HB1_V	243	50_MMW_SMR525_S14H_VPOL	34
34	50_MMW_SMR525_S1L_HPOL	309	50_LB2_H	50_HB2_H	298	50_MMW_SMR525_S1H_HPOL	34
34	50_MMW_SMR525_S9L_VPOL	299	50_LB2_V	50_HB2_V	307	50_MMW_SMR525_S9H_VPOL	34
34	50_MMW_SMR525_S5L_HPOL	278	50_LB3_H	50_HB3_H	266	50_MMW_SMR525_S5H_HPOL	34
34	50_MMW_SMR525_S13L_VPOL	267	50_LB3_V	50_HB3_V	277	50_MMW_SMR525_S13H_VPOL	34
34	50_MMW_SMR525_S2L_HPOL	338	50_LB4_H	50_HB4_H	328	50_MMW_SMR525_S2H_HPOL	34
34	50_MMW_SMR525_S10L_VPOL	300	50_LB4_V	50_HB4_V	308	50_MMW_SMR525_S10H_VPOL	34

PART_NUMBER=339M00116
BOMOPTION=RF_SKU:NAMM
ROOM=BG1

U_BG1_E
MWNP01SEMA01
LGA
SYM 2 OF 3
CRITICAL

1	GND	GND	97
2	GND	GND	98
3	GND	GND	99
4	GND	GND	100
5	GND	GND	101
6	GND	GND	102
7	GND	GND	103
8	GND	GND	104
9	GND	GND	105
10	GND	GND	106
11	GND	GND	107
12	GND	GND	108
13	GND	GND	109
14	GND	GND	110
15	GND	GND	111
16	GND	GND	112
17	GND	GND	113
18	GND	GND	114
19	GND	GND	115
20	GND	GND	116
21	GND	GND	117
22	GND	GND	118
23	GND	GND	119
24	GND	GND	120
25	GND	GND	121
26	GND	GND	122
27	GND	GND	123
28	GND	GND	124
29	GND	GND	125
30	GND	GND	126
31	GND	GND	127
32	GND	GND	128
33	GND	GND	129
34	GND	GND	130
35	GND	GND	131
36	GND	GND	132
37	GND	GND	133
38	GND	GND	134
39	GND	GND	135
40	GND	GND	136
41	GND	GND	137
42	GND	GND	138
43	GND	GND	139
44	GND	GND	140
45	GND	GND	141
46	GND	GND	142
47	GND	GND	143
48	GND	GND	144
49	GND	GND	145
50	GND	GND	146
51	GND	GND	147
52	GND	GND	148
53	GND	GND	149
54	GND	GND	150
55	GND	GND	151
56	GND	GND	152
57	GND	GND	153
58	GND	GND	154
59	GND	GND	155
60	GND	GND	156
61	GND	GND	157
62	GND	GND	158
63	GND	GND	159
64	GND	GND	160
65	GND	GND	161
66	GND	GND	162
67	GND	GND	163
68	GND	GND	164
69	GND	GND	165
70	GND	GND	166
71	GND	GND	167
72	GND	GND	168
73	GND	GND	169
74	GND	GND	170
75	GND	GND	171
76	GND	GND	172
77	GND	GND	173
78	GND	GND	174
79	GND	GND	175
80	GND	GND	176
81	GND	GND	177
82	GND	GND	178
83	GND	GND	179
84	GND	GND	180
85	GND	GND	181
86	GND	GND	182
87	GND	GND	183
88	GND	GND	184
89	GND	GND	185
90	GND	GND	186
91	GND	GND	187
92	GND	GND	188
93	GND	GND	189
94	GND	GND	190
95	GND	GND	191
96	GND	GND	192

PART_NUMBER=339M00116
BOMOPTION=RF_SKU:NAMM
ROOM=BG1

U_BG1_E
MWNP01SEMA01
LGA
SYM 3 OF 3
CRITICAL

193	GND	GND	293
194	GND	GND	294
195	GND	GND	295
196	GND	GND	296
197	GND	GND	297
198	GND	GND	301
199	GND	GND	302
200	GND	GND	303
201	GND	GND	304
202	GND	GND	305
203	GND	GND	306
204	GND	GND	310
205	GND	GND	311
206	GND	GND	312
207	GND	GND	313
208	GND	GND	314
209	GND	GND	315
210	GND	GND	316
211	GND	GND	317
212	GND	GND	318
213	GND	GND	319
214	GND	GND	320
215	GND	GND	321
216	GND	GND	322
217	GND	GND	323
218	GND	GND	324
219	GND	GND	325
220	GND	GND	326
221	GND	GND	327
222	GND	GND	329
223	GND	GND	330
224	GND	GND	331
225	GND	GND	332
226	GND	GND	333
227	GND	GND	334
228	GND	GND	335
229	GND	GND	336
230	GND	GND	337
231	GND	GND	339
232	GND	GND	340
233	GND	GND	341
234	GND	GND	342
237	GND	GND	343
238	GND	GND	344
239	GND	GND	345
240	GND	GND	346
241	GND	GND	347
242	GND	GND	348
245	GND	GND	349
246	GND	GND	350
247	GND	GND	351
248	GND	GND	352
249	GND	GND	353
250	GND	GND	354
251	GND	GND	355
252	GND	GND	356
253	GND	GND	357
254	GND	GND	358
255	GND	GND	359
256	GND	GND	360
257	GND	GND	361
258	GND	GND	362
259	GND	GND	363
260	GND	GND	364
261	GND	GND	365
262	GND	GND	366
263	GND	GND	367
264	GND	GND	368
265	GND	GND	369
268	GND	GND	370
269	GND	GND	371
270	GND	GND	372
271	GND	GND	373
272	GND	GND	374
273	GND	GND	375
274	GND	GND	376
275	GND		
276	GND		
279	GND		
280	GND		
281	GND		
282	GND		
283	GND		
284	GND		
285	GND		
286	GND		
287	GND		
288	GND		
289	GND		
290	GND		
291	GND		
292	GND		

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DRAWING NUMBER 051-05263
SIZE D
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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

HIER_NFC

LAST_MODIFICATION=Wed Jul 1 15:22:42 2020

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56	3	NFC_P_FE		

PRIMARY CHIP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00629	338S00630	?	NFC_P	SN210V PROD VS DEV

D54 PRIMARY MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00026	2	CAP,CER,C0G,820PF,2%25V,0201	C7510_S,C7513_S	?
131S00016	2	CAP,CER,C0G,470PF,2%25V,0201	C7550_S,C7551_S	?
152S01116	2	IND,82NH,2.5%,0.55A,0402	L7500_S,L7501_S	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7514_S,C7542_S	?
131S0825	2	CAP,CER,C0G,560PF,2%,25V,0201	C7512_S,C7541_S	?
131S00025	1	CAP,CER,C0G,1000PF,2%,50V,0201	C7546_S	?
131S00209	1	CAP,CER,C0G,68PF,2%,25V,0201	C7547_S	?
131S00016	1	CAP,CER,C0G,470PF,2%,50V,0201	C7548_S	?
131S0731	1	CAP,CER,C0G,100PF,2%,25V,0201	C7558_S	NOSTUFF

XTAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00077	197S00206	?	Y7500_S	XTAL,27P12 MHZ
197S00076	197S00206	?	Y7500_S	XTAL,27P12 MHZ

2 IN PP_VDD_MAIN VOLTAGE=3.8
2 IN PP1V2_NFC_S2 VOLTAGE=1.2
2 IN PP1V8_S4 VOLTAGE=1.8V
2 IN PP1V2_S4 VOLTAGE=1.2

2 IO I2C_R1_TO_NFC_SCL
2 IO I2C_R1_TO_NFC_SDA
2 IO I2C_BT_TO_NFC_SCL
2 IO I2C_BT_TO_NFC_SDA

2 IO SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
2 IO SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R

2 IN GPIO_SEQ_PMU_TO_NFC_EN

2 IN NFC_P_THERMISTOR_UAT4
2 IN NTC_STOCKHOLM

2 OUT GPIO_SE_TO_BT_PKT_RDY
2 OUT GPIO_NFC_TO_ARCAMP_RESET_L
2 OUT GPIO_NFC_TO_ARCAMP_TRIG
2 IO NFC_P_ANT_POS
2 IO NFC_P_ANT_NEG
IO 2 NFC_P_TEST_OUT

2 IN GPIO_NFC_F_NFC_P_SYNC2
2 IN GPIO_NFC_F_NFC_P_SYNC1
2 IN IO_TOUCH_TO_MANY_SCAN_ACTIVE_U

NFC: TABLE OF CONTENTS

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STOCKHOLM

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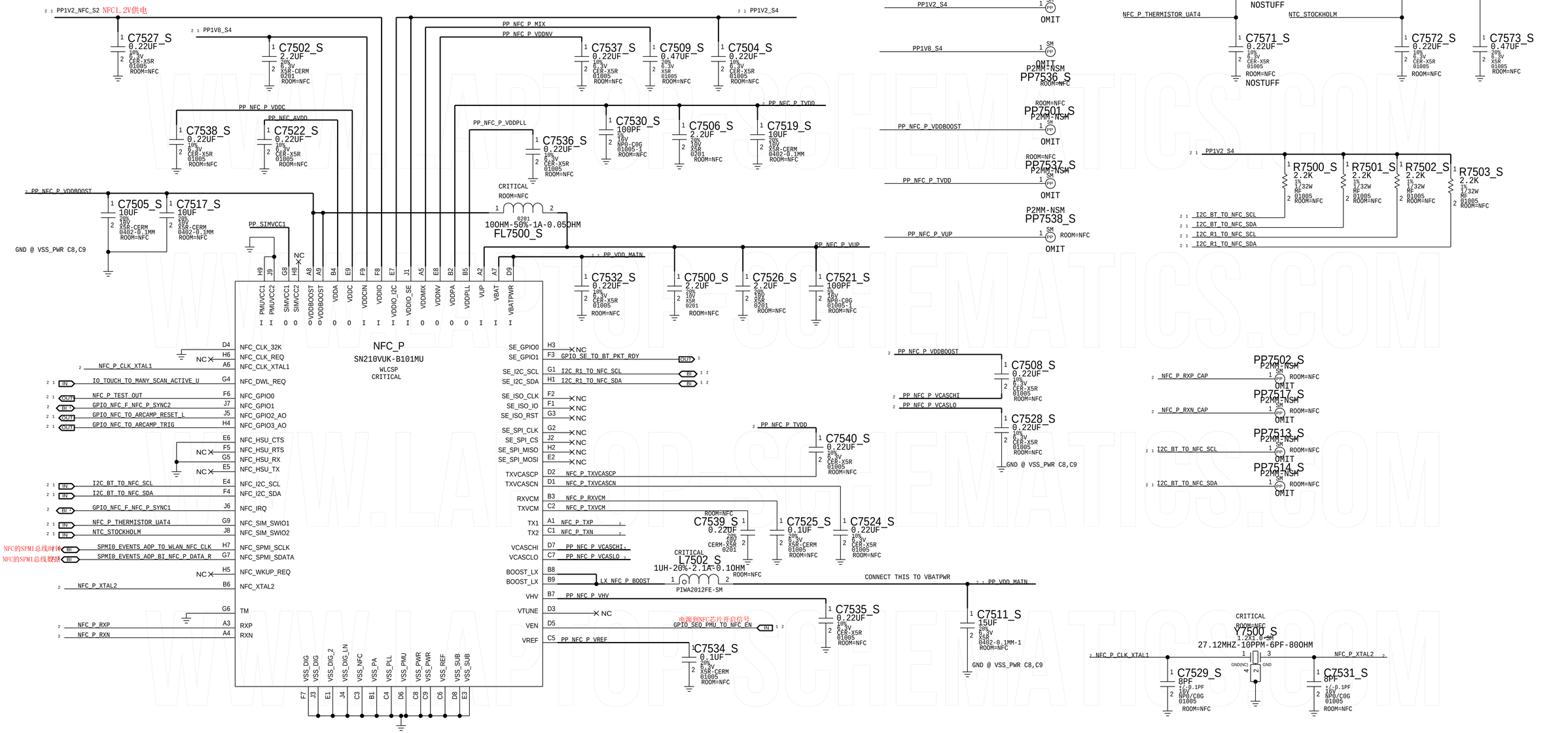

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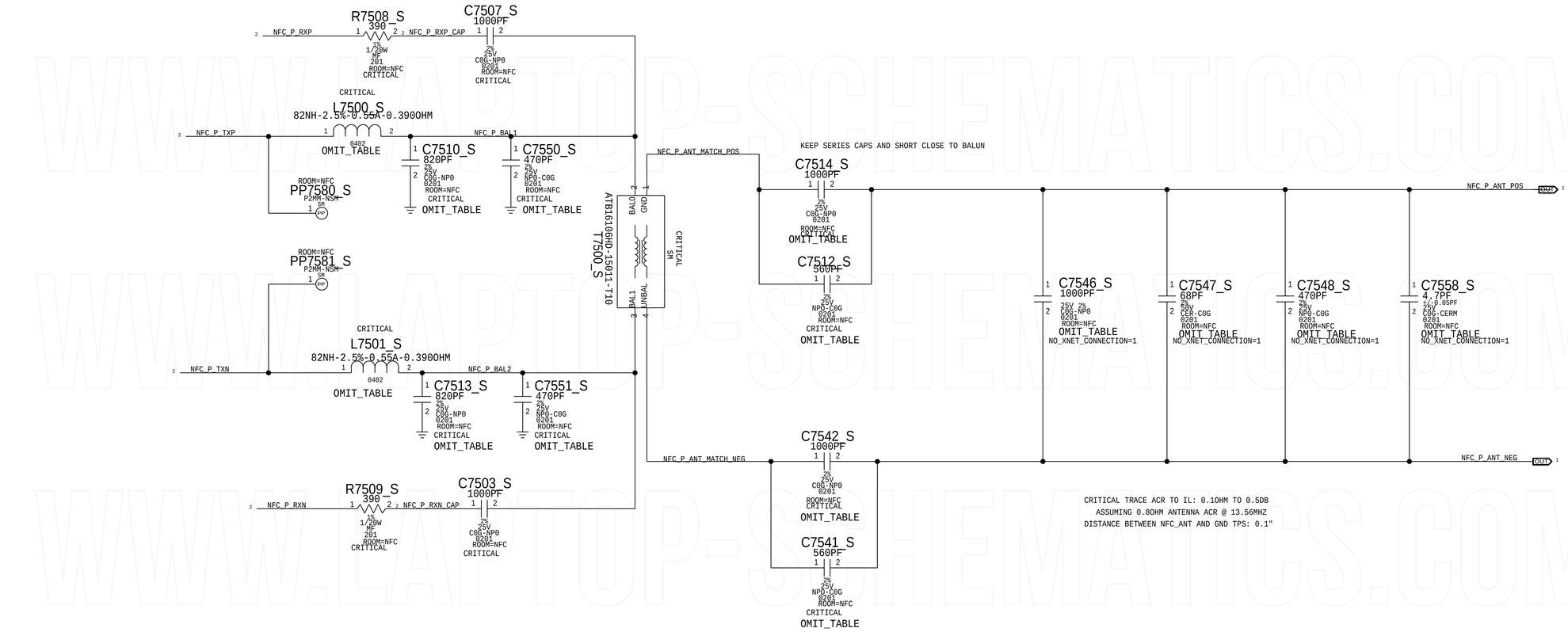

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

D54 HIER_WIFI_BOT

LAST_MODIFICATION=Wed Jul 1 15:22:37 2020

PAGE	CSA	CONTENTS	SYNC	DATE
57	1	Table of Contents_D52		
58	2	THELONIOUS	D52_WIFI_MASTER_0.21.0	
59	7	2G4 rFEM (UAT)	D52_WIFI_MASTER_0.17.0	
60	8	2G4 rFEM (LAT)	D52_WIFI_MASTER_0.17.0	

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	WIFI_MASTER	2	0.21.0	S	2019_12_09_16:30:41

SYMBOL IO PORTS

POWER

MAKE_BASE=TRUE
PP_VDD_MAIN VOLTAGE=3.8 — PP_VDD_MAIN
PP_VDD_MAIN VOLTAGE=3.8
PP_VDD_MAIN VOLTAGE=3.8
PP1V8_S2 VOLTAGE=1.8V
PP1V8_S4 VOLTAGE=1.8V
PP1V2_S4 VOLTAGE=1.2

ANTENNA

50_TRX_WLAN_G_BT_ANT4_NPLXR
50_TRX_WLAN_G_BT_ANT3_NPLXR

RFEM CONNECTIONS

RF
50_WLAN_A_C0_TXRX_FEM_M
50_WLAN_A_C1_TXRX_FEM_M

ANALOG
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
ANALOG_LAT_5G_FEM_TO_WLAN_PDTS

GPIO
GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN

RFFE
RFFE_WLAN_TO_UAT_5G_FEM_RST_L
RFFE_WLAN_TO_LAT_5G_FEM_RST_L
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA

CELLULAR CONNECTIONS

UART_BB_TO_WLAN_TX
UART_BB_TO_WLAN_RX

AP CONNECTIONS

GPIO_AP_FROM_WLAN_TIME_SYNC
GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG
GPIO_AP_FROM_BT_AUDIO_SYNC

PCIE
PCIE_GP1_AP_TO_WLAN_PERST_L
PCIE_GP1_AP_BI_WLAN_CLKREQ_L
90_PCIE_GP1_AP_TO_WLAN_TX_P
90_PCIE_GP1_AP_TO_WLAN_TX_N
90_PCIE_GP1_AP_FROM_WLAN_RX_P
90_PCIE_GP1_AP_FROM_WLAN_RX_N
90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
90_PCIE_GP1_AP_TO_WLAN_REFCLK_N

AOP CONNECTIONS

SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
SPMI0_EVENTS_AOP_BI_WLAN_DATA_R
GPIO_AOP_TO_WLAN_CONTEXT_A
GPIO_AOP_TO_WLAN_CONTEXT_B

PMU CONNECTIONS

GPIO_S4_PMU_TO_WLAN_REG_ON
GPIO_PMU_FROM_WLAN_HOST_WAKE
CLK_GPIO_S4_PMU_TO_WLAN_R1_32K

SE CONNECTIONS

I2C_BT_TO_NFC_SCL
I2C_BT_TO_NFC_SDA
GPIO_SE_TO_BT_PKT_RDY

R1 CONNECTIONS

GPIO_R1_TO_WLAN_COEX
GPIO_WLAN_TO_R1_COEX
IO_BT_TO_R1_TIME_SYNC
IO_BT_TO_R1_WAKE

SPKR CONNECTIONS

GPIO_BT_TO_BOT_SPKR_TRIG

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5G INTERSTATE BPFS

R201_W 0.8NH-+/-0.05NH-0.9A — 50_WLAN_A_C0_TXRX_FEM_M — 01005 — 50_WLAN_A_C0_TXRX_BPF
C203_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
C204_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
FL_ISG_U_W ACPF-7350-AP1 LGA CRITICAL — TX/RX — GND — ANT — ROOM=WLAN
50_WLAN_A_C0_TXRX_BPF_R — R233_W 0.0D 0% 1/32W MF 01005 ROOM=WLAN — 50_WLAN_A_C0_TXRX
C201_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
C202_W 0.2PF +/-0.05PF 16V C0G-CERM 01005

R202_W 0.6NH-+/-0.05NH-0.95A — 50_WLAN_A_C1_TXRX_FEM_M — 01005 — 50_WLAN_A_C1_TXRX_BPF
C205_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
C206_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
FL_ISG_L_W ACPF-7350-AP1 LGA CRITICAL — TX/RX — GND — ANT — ROOM=WLAN
50_WLAN_A_C1_TXRX_BPF_R — R235_W 0.6NH-+/-0.05NH-0.95A — 01005 — 50_WLAN_A_C1_TXRX
C228_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
C241_W 0.2PF +/-0.05PF 16V C0G-CERM 01005

R237_W 0.0D 0% 1/32W MF 01005 ROOM=WLAN — 50_WLAN_G_C0_TXRX_FEM_M — 50_WLAN_G_C0_TXRX_R
C230_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
C243_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN

R238_W 0.0D 0% 1/32W MF 01005 ROOM=WLAN — 50_WLAN_G_C1_TXRX_FEM_M — 50_WLAN_G_C1_TXRX_R
C231_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN
C244_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 — NOSTUFF ROOM=WLAN

PP1V2_S4 VOLTAGE=1.2
C250_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN
PP1V8_S4
C252_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN
C257_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN
PP_VDD_MAIN VOLTAGE=3.8
C232_W 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=WLAN
C233_W 4.7PF +/-0.1PF 16V NP0/C0G 01005 ROOM=WLAN
PP_VDD_MAIN
C245_W 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=WLAN
C247_W 2.2UF 20% 6.3V X5R-CERM 0201
C246_W 27PF 5% 16V NP0-C0G 01005-1 ROOM=WLAN

L253_W 2.2UH-20%-1.1A-0.293OHM 0603 ROOM=WLAN — PP1V02_ABUCK_L VOLTAGE=1.02
C254_W 7.5UF 20% 4V CERM 0402 ROOM=WLAN
PP1V02_ABUCK VOLTAGE=1.02
L255_W 2.2UH-20%-1.1A-0.293OHM 0603 ROOM=WLAN — PP0V72_CBUCK_L VOLTAGE=0.72
C256_W 7.5UF 20% 4V CERM 0402 ROOM=WLAN
PP0V72_CBUCK VOLTAGE=0.72
PP3V3_BTLDO VOLTAGE=3.3
C270_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN

VBAT 169 VBAT 183 VBAT_RF 205 — VDDIO_RF 5 — VDDIO1P2 204 — VDDIO1P8 6
ASR_VLX 186 — ASR_VLX 200 — ABUCK_1P02 202
ABUCK_WL2G_BT_1P02 206 — ABUCK_WL2G_BT_1P02 207 — ABUCK_WL5G_1P02 179 — ABUCK_WL5G_1P02 165
CSR_VLX 184 — CSR_VLX 198 — CBUCK_0P72 3 — CBUCK_0P72 17 — CBUCK_0P72 141 — BTLDO3V3 194

ANALOG_UAT_5G_FEM_TO_WLAN_PDTS — 5G_C0_ANT 28 — 5GTSSI_C0 56 — 5G_C1_ANT 12 — 5GTSSI_C1 10
ANALOG_UAT_LAT_5G_FEM_TO_WLAN_PDTS — 2G_C0_ANT 196 — 2GTSSI_C0 168 — 2G_C1_ANT 112 — 2GTSSI_C1 140
ANALOG_UAT_2G_FEM_TO_WLAN_PDTS

GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN — LNA_EN_5GC0 61
GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN — LNA_EN_5GC1 46
GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN — LNA_EN_2GC0 62
GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN — LNA_EN_2GC1 20

RFFE_WLAN_TO_UAT_5G_FEM_RST_L — 5G_C0_RESET 48
RFFE_WLAN_TO_UAT_2G_FEM_RST_L — 2G_C0_RESET 33
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK — C0_MIPI_CLK 50
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA — C0_MIPI_DATA 49
RFFE_WLAN_TO_LAT_5G_FEM_RST_L — 5G_C1_RESET 19
RFFE_WLAN_TO_LAT_2G_FEM_RST_L — 2G_C1_RESET 34
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK — C1_MIPI_CLK 36
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA — C1_MIPI_DATA 35

NC — WL_GPIO_7/DAP_SEL 63
PLACE_SIDE=BOTTOM
SM PP207_W P2MM-NSM ROOM=WLAN OMIT — WL_GPIO_18 1 — WL_GPIO_18 120
UART_BB_TO_WLAN_TX — WLBT_SECI_IN 105
UART_BB_TO_WLAN_RX — WLBT_SECI_OUT 119
SM PP242_W P2MM-NSM ROOM=WLAN OMIT — GPIO_AP_FROM_WLAN_TIME_SYNC 1 — WLAN_TIME_SYNC 147
CPU到WIFI的时间同步信号
NC — LHL_GPIO2 130
NC — SPMI_IDC_CLK 157
NC — SPMI_IDC_DAT 144

CPU到WIFI PCIE总线复位 — PCIE_GP1_AP_TO_WLAN_PERST_L — WLBT_WL_PCIE_PERST_L 44
WIFI到CPU的 PCIE总线时钟请求 — PCIE_GP1_AP_BI_WLAN_CLKREQ_L — WLBT_WL_PCIE_CLKREQ_L 86
CPU到WIFI PCIE总线发射P — 90_PCIE_GP1_AP_TO_WLAN_TX_P — 90_WLBT_WL_PCIE_RD_P 29
CPU到WIFI PCIE总线发射N — 90_PCIE_GP1_AP_TO_WLAN_TX_N — 90_WLBT_WL_PCIE_RD_N 15
CPU到WIFI PCIE总线接收P — 90_PCIE_GP1_AP_FROM_WLAN_RX_P — 90_WLBT_WL_PCIE_TD_P 71
CPU到WIFI PCIE总线接收N — 90_PCIE_GP1_AP_FROM_WLAN_RX_N — 90_WLBT_WL_PCIE_TD_N 57
CPU到WIFI PCIE总线时钟P — 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P — 90_WLBT_WL_PCIE_REFCLK_P 113
CPU到WIFI的PCIE总线时钟N — 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N — 90_WLBT_WL_PCIE_REFCLK_N 99
C226_W 100PF 10% 16V X5R 01005-1 NOSTUFF

SM PP243_W P2MM-NSM ROOM=WLAN OMIT — RF_SW_CTRL_3 1 — RF_SW_CTRL_3 47
NC — CLK_REQ 172

U_WLAN_W THELONIOUS-U-ES4.3 LGA 2103-601901-80 SYM 1 OF 2 CRITICAL

WLBT_WL_FAST_UART_RX 104 — NC
WLBT_WL_FAST_UART_RTS_OUT 75 — NC
WLBT_WL_FAST_UART_CTS_IN 89 — NC
WLBT_WL_FAST_UART_TX 90 — NC
WLBT_WL_HOST_WAKE 91 — GPIO_PMU_FROM_WLAN_HOST_WAKE 1 — 电源到WIFI的唤醒信号 — PP244_W SM P2MM-NSM OMIT ROOM=WLAN
WLBT_WL_REG_ON 174 — GPIO_AP_TO_WLAN_REG_ON 1 — 电源到WIFI的开启信号 GPIO_S4_PMU_TO_WLAN_REG_ON — PP206_W SM P2MM-NSM OMIT ROOM=WLAN

WLAN_TDI/CXT_A 74 — GPIO_AOP_TO_WLAN_CONTEXT_A 1 — PP201_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TDO/CXT_B 60 — GPIO_AOP_TO_WLAN_CONTEXT_B 1 — PP202_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TRST_L 64 — JTAG_WLAN_TRST_L 1 — PP203_W SM P2MM-NSM OMIT ROOM=WLAN
JTAG_SEL 171 — JTAG_WLAN_SEL 1 — PP232_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_SCT/SWD_CLK 103 — JTAG_WLAN_TCK 1 — PP204_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TMS/SWD_DAT 78 — JTAG_WLAN_TMS 1 — PP205_W SM P2MM-NSM OMIT ROOM=WLAN

WL_GPIO_21/BT_OVER_UART 146 — NC
WLBT_BT_UART_RXD 172 — NC
WLBT_BT_UART_RTS_L 178 — NC
WLBT_BT_UART_CTS_L 176 — NC
WLBT_BT_UART_TXD 175 — NC
WLBT_BT_DEV_WAKE 189 — GPIO_BT_TO_BOT_SPKR_TRIG 1 — PP210_W SM P2MM-NSM OMIT ROOM=WLAN
WLBT_BT_REG_ON 173 — NC

1V2_WIFI_TO_SENSORA_COEX 116 — NC
1V2_BT_TO_SENSORA_COEX 134 — NC
1V8_WIFI_TO_SENSORA_COEX 77 — NC
1V8_BT_TO_SENSORA_COEX 76 — NC
GPIO_SENSORB_TO_BT_SYNC 161 — GPIO_SE_TO_BT_PKT_RDY 1 — PP211_W SM P2MM-NSM OMIT ROOM=WLAN
SENSORC_TO_WIFI_COEX 118 — GPIO_R1_TO_WLAN_COEX 1 — PP233_W SM P2MM-NSM OMIT ROOM=WLAN
WIFI_TO_SENSORC_COEX 117 — GPIO_WLAN_TO_R1_COEX 1 — PP234_W SM P2MM-NSM OMIT ROOM=WLAN
BT_TO_SENSORC_TIME_SYNC 160 — TO_BT_TO_R1_TIME_SYNC 1 — PP235_W SM P2MM-NSM OMIT ROOM=WLAN
BT_TO_SENSORC_WAKE 133 — TO_BT_TO_R1_WAKE 1 — PP212_W SM P2MM-NSM OMIT ROOM=WLAN
SOC_TO_BT_TIME_SYNC 162 — CPU输出的同步信号 GPIO_ISP_RCAM_TO_STROBE_KRAKEN 1 — PP238_W SM P2MM-NSM OMIT ROOM=WLAN
BT_TO_AP_TIME_SYNC 191 — CPU到蓝牙声音同步信号 GPIO_AP_FROM_BT_AUDIO_SYNC 1 — PP236_W SM P2MM-NSM OMIT ROOM=WLAN
CKPLUS_WAIVE=I2C_PULLUP
SE_I2C_CLK 158 — I2C_BT_TO_NFC_SCL
SE_I2C_DAT 159 — I2C_BT_TO_NFC_SDA
CKPLUS_WAIVE=I2C_PULLUP
SPMI_HEB_CLK 132 — SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK 1 — CPU到蓝牙WIFI NFC的SPMI总线时钟 — PP214_W SM P2MM-NSM OMIT ROOM=WLAN
SPMI_HEB_DAT 131 — SPMI0_EVENTS_AOP_BI_WLAN_DATA_R 1 — CPU到蓝牙WIFI NFC的SPMI总线数据 — PP215_W SM P2MM-NSM OMIT ROOM=WLAN
WLBT_CLK_32K 145 — CLK_GPIO_S4_PMU_TO_WLAN_R1_32K 1 — 电源到WIFI 超带宽芯片的时钟 — PP239_W SM P2MM-NSM OMIT ROOM=WLAN
TCXO_IN 8 — NC

U_WLAN_W THELONIOUS-U-ES4.3 LGA 2103-601901-80 SYM 2 OF 2 CRITICAL — ROOM=WLAN

GND 1	GND 98	GND 2	GND 100	GND 4	GND 101	GND 7	GND 102	GND 9	GND 106	GND 11	GND 107	GND 13	GND 108	GND 14	GND 109	GND 16	GND 110	GND 18	GND 111	GND 21	GND 114	GND 22	GND 115	GND 23	GND 121	GND 24	GND 122	GND 25	GND 123	GND 26	GND 124	GND 27	GND 125	GND 30	GND 126	GND 31	GND 127	GND 32	GND 128	GND 37	GND 129	GND 38	GND 135	GND 39	GND 136	GND 40	GND 137	GND 41	GND 138	GND 42	GND 139	GND 43	GND 142	GND 45	GND 143	GND 51	GND 148	GND 52	GND 149	GND 53	GND 150	GND 54	GND 151	GND 55	GND 152	GND 58	GND 153	GND 59	GND 154	GND 65	GND 155	GND 66	GND 156	GND 67	GND 163	GND 68	GND 164	GND 69	GND 166	GND 70	GND 167	GND 72	GND 170	GND 73	GND 192	GND 79	GND 193	GND 80	GND 180	GND 81	GND 181	GND 82	GND 182	GND 83	GND 185	GND 84	GND 187	GND 85	GND 188	GND 87	GND 190	GND 88	GND 195	GND 92	GND 197	GND 93	GND 199	GND 94	GND 201	GND 95	GND 203	GND 96	GND 208	GND 97	GND 209	GND 210

CPU到WIFI PCIE总线复位 — OMIT SM PP222_W P2MM-NSM ROOM=WLAN — PCIE_GP1_AP_TO_WLAN_PERST_L
WIFI到CPU的 PCIE总线时钟请求 — OMIT SM PP223_W P2MM-NSM ROOM=WLAN — PCIE_GP1_AP_BI_WLAN_CLKREQ_L
CPU到WIFI PCIE总线发射P — OMIT SM PP224_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_TX_P
CPU到WIFI PCIE总线发射N — OMIT SM PP225_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_TX_N
CPU到WIFI PCIE总线接收P — OMIT SM PP226_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_FROM_WLAN_RX_P
OMIT SM PP227_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_FROM_WLAN_RX_N
CPU到WIFI的PCIE总线时钟P — OMIT SM PP228_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
OMIT SM PP229_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N — CPU到WIFI的PCIE总线时钟N

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00773	339S00761	?	U_WLAN_W	BOMOPTION FOR STATS

SENSOR A = DOTARA
SENSOR B = SE
SENSOR C = R1

GPIO_PMU_FROM_WLAN_HOST_WAKE — R259_W 100K 5% 1/32W MF 01005 ROOM=WLAN
PP1V2_S4 — R257_W 10K 5% 1/32W MF 01005 ROOM=WLAN NOSTUFF
JTAG_WLAN_SEL — NOSTUFF= JTAG DISABLED

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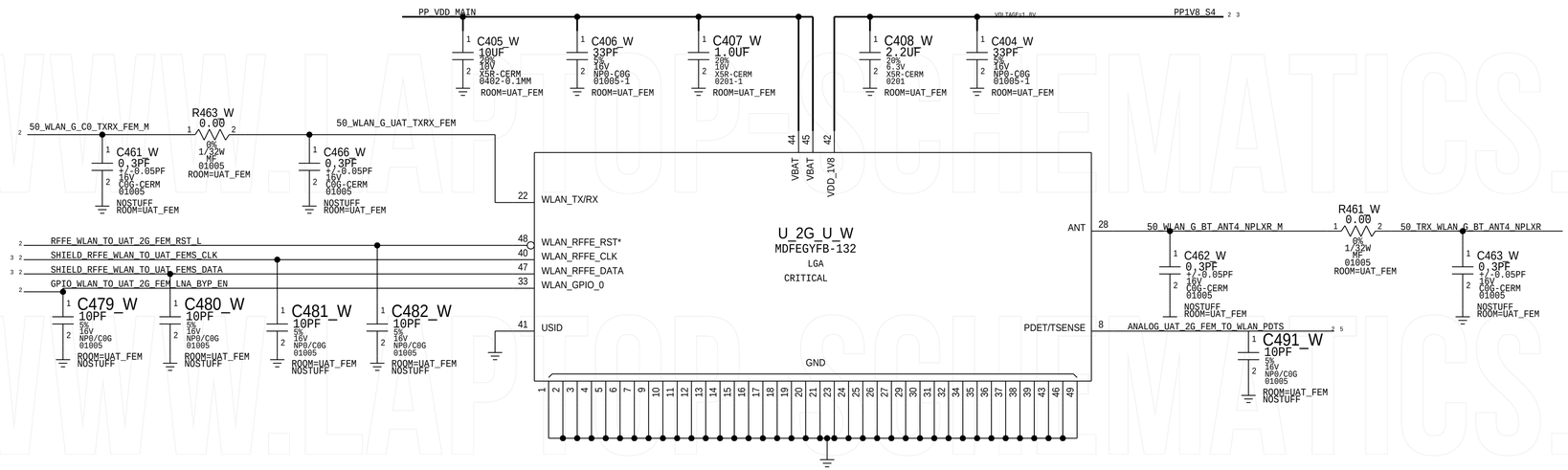

OMIT_SM PP216_W P2MM-NSM ROOM=WLAN — ANALOG_UAT_2G_FEM_TO_WLAN_PDTS

OMIT_SM PP250_W P2MM-NSM ROOM=UAT_FEM — SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK

OMIT_SM PP251_W P2MM-NSM ROOM=UAT_FEM — SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA

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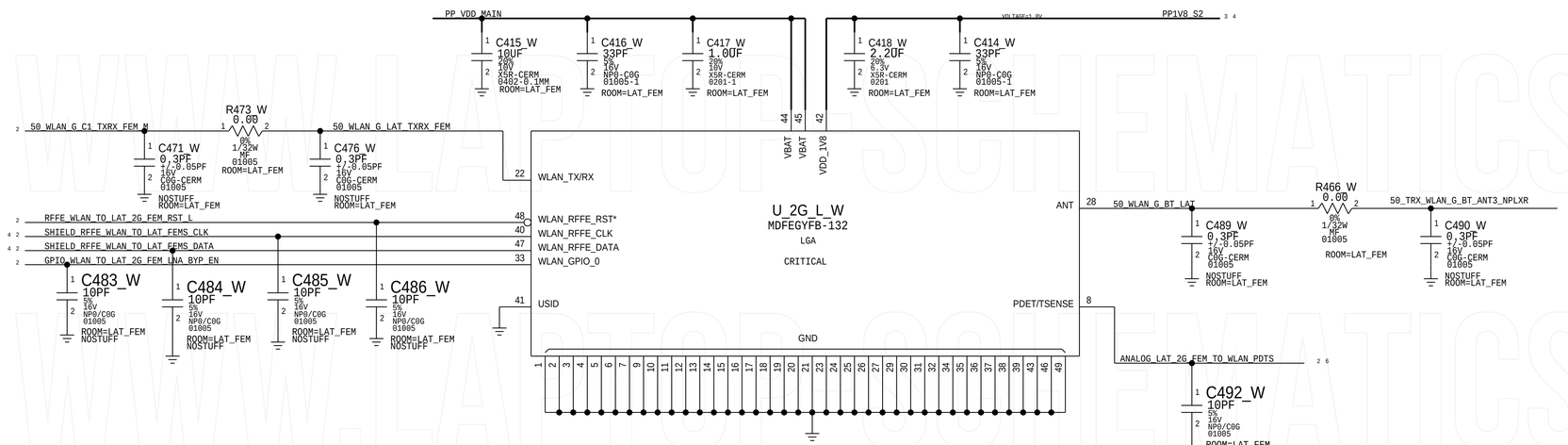

OMIT SM PP217_W P2MM-NSM ROOM=WLAN — ANALOG_LAT_2G_FEM_TO_WLAN_PDTS

OMIT SM PP252_W P2MM-NSM ROOM=LAT_FEM — SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK

OMIT SM PP253_W P2MM-NSM ROOM=LAT_FEM — SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA

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